

SSDM 2000 Advance Program

GENERAL INFORMATION

DATE

The 2000 International Conference on Solid State Devices and Materials (SSDM 2000) will be held from Tuesday, August 29 through Thursday, 31, 2000.

A half-day short course will be held on Monday evening, August 28.

LOCATION

SENDAI INTERNATIONAL CENTER

Aobayama, Aoba-ku, Sendai-shi 980-0856

Phone: +81-22-265-2211

Fax: +81-22-265-2485

REGISTRATION

The registration desk will be open from Monday to Thursday.

The registration hours are as follows.

August 28 11:00-17:00 (Short Course) 2F Lobby

August 28 18:00-20:00 (Conference) 2F Lobby

August 29 8:00-18:00 2F Lobby

August 30 8:30-18:00 2F Lobby

August 31 8:30-15:00 2F Lobby

Pre-registration is recommended due to the expected large number of participants. In order to pre-register for SSDM 2000, the enclosed Registration Form should be returned with your payment by July 31 to the SSDM 2000 Secretariat. Payment should be made in Japanese yen by bank transfer or bank draft payable to the SSDM 2000 Secretariat. Credit cards are acceptable from overseas attendees only: Diners, Master Card, VISA and AMEX. No personal checks will be accepted. After your remittance has been received, the receipt and a voucher for the participant's kit will be sent by the secretariat in middle of August.

*Bank transfer to SSDM

A/C No. 075-1229143

Daiichi Kangyo Bank, Hongo Branch, Tokyo

	Registration Fee			Banquet
	by July 10, 2000	after August 1, 2000	Short Course	
Regular	JPY35,000	JPY40,000	JPY10,000	JPY6,000
Student	JPY18,000		JPY1,000	JPY3,000
Accompanying Person				JPY3,000

1. The conference registration fee covers the conference attendance and includes a copy of the Extended Abstracts.
2. **Student fee of Short Course has been discounted from JPY5,000 to JPY1,000.**
3. Most lectures of the short course are given in Japanese (No Translation), while their texts are prepared in English.

CANCELLATION

Conference:

Cancellation fee of JPY3,000 will be deducted from the refund. Cancellations should be made in writing to the SSDM 2000 Secretariat. No cancellation will be allowed after August 10, 2000. Extended Abstracts will be sent to absent registrants after the Conference.

Short Course:

Regular: JPY2,000 will be deducted.

Student: No Cancellation

Cancellations should be made in writing to the SSDM 2000 Secretariat. No cancellation will be allowed after August 10, 2000. A text will be sent to absent registrants after the Conference

BANQUET

A buffet dinner will be held at "RECEPTION HALL" of the conference site (2F) on August 29 from 18:30-20:30. Tickets (JPY6,000 each) can be purchased at the registration desk.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted. A two-page description must be sent in the camera-ready format as required for the regular papers. The accepted papers will be included in the Extended Abstracts.

Original 2-page manuscript, 15 copies of printed or photocopied on both sides of a sheet with Author's Application Form and Copyright Form should be sent to SSDM 2000 Secretariat.

Author's Application Form and Copyright Form are available in Web Page.
(<http://ssdm.bcasj.or.jp/>)

<p>Deadline for receipt of Late News papers is July 7, 2000.</p>
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Notice of acceptance will be mailed by the early in August.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed without opportunity for further change in the extended abstracts, which will be distributed on the opening day of the Conference.

Authors of accepted papers are encouraged to submit an extended version for a special issue of the Japanese Journal of Applied Physics. This special issue will be published in 2001. Details will be provided with the notice of acceptance.

INSTRUCTIONS FOR SPEAKERS

Session Registration

In order to run the program smoothly, speakers are requested to visit the session registration desk no later than 15 minutes before their session starts.

Presentation Time

The time assigned to a contributed paper is 15 minutes for each session, including 3 minutes for discussion. The time assigned to an invited paper (except Plenary Talks) is 30 minutes, including 5 minutes for discussion.

AWARDS

"SSDM Awards" will be given to excellent papers presented in the previous conferences.

SSDM Award

For the paper outstandingly contributed to the field of solid state devices and materials, among the papers presented prior to 1989.

SSDM Paper Award

For the best paper presented at the last conference.

SSDM Young Researcher Award

For a few excellent papers by young researchers presented at the last conference.

FINANCIAL SUPPORT

Limited financial support for presentations by students and by researchers from newly industrializing countries is available. The amount will be JPY40,000. Those who are interested in the support should directly contact to the Steering Committee, c/o Business Center for Academic Societies Japan

VISA REQUIREMENT

All foreign participants must have valid passport. Participants from countries where a visa is required to enter Japan are recommended to apply at the nearest Japanese embassy in their countries as soon as possible.

OFFICIAL TRAVEL AGENT

Japan Travel Bureau (JTB) has been appointed as the official travel agent for the Conference and will handle hotel accommodations.

Japan Travel Bureau (JTB)

Tohoku Communications Inc.

Kotsukosha Bldg 3F, 3-6-8 Chuo, Aoba-ku, Sendai 980-0021, Japan

Phone: +81-22-262-5055

FAX: +81-22-262-5002

E-mail: tcs02@thk.jtb.co.jp

HOTEL ACCOMMODATIONS

The Organizing Committee of SSDM 2000 has a block of sufficient rooms at discount convention rates to accommodate participants and accompanying persons. The Accommodation Reservation Form should be sent by postal mail or fax to Japan Travel Bureau, Inc. (JTB) **before July 19**. If a room at your first choice hotel is unavailable, the second choice (or third choice) hotel will be assigned. Reservation confirmation will be sent to you by E-mail or by fax.

No	Hotels	Single	Twin	From the Conference site
1	Sendai Tokyu Hotel	JPY9,500	JPY16,000	15 min on foot
2	Sendai Daini Washington Hotel	JPY8,700	JPY15,400	10 min on foot
3	Sendai Daiichi Washington Hotel	JPY7,700	Not available	10 min on foot

4	Hotel Bel Air Sendai	JPY8,000	JPY15,000	20 min on foot
5	Sendai Fuji Hotel	JPY7,350	JPY12,600	20 min on foot
6	Chisan Hotel Sendai	JPY7,600	JPY13,600	30 min on foot
7	Hotel Richfield Sendai	JPY6,825	JPY14,806	20 min on foot
8	Hotel Sendai Golden Palace	JPY6,800	JPY13,600	25 min on foot

*The amount of charges is per room for one night.

*Above room rate includes government tax and service charge but no meal.

*Please pay all charges directly to the hotel in cash or by credit card when checking out.

*Inform JTB of any changes in your dates of arrival and/or departure or of cancellation.

*You MUST give notice to JTB if you intend to check in at the hotel later than 21:00 on the intended arrival date, or your reservation may be canceled.

RUMP SESSIONS

Rump A (18:00-20:00, August 30, 2000)

Title: Key technology for future wireless systems

--- Can Si Overcome GaAs ? ---

Moderators: K. Honjo (NEC)

Panelists: N. Suematsu (Mitsubishi)

K. Masu(Tokyo Inst. of Technol.)

N. Iwata (NEC)

K. Washio(Hitachi)

S. Ohara (Fujitsu)

Y. Ohta (Matsushita)

Recent significant growth for mobile communications is indebted to the progress of microwave transistor technologies. Since a suitable frequency range for mobile communications is a 1 GHz to 2 GHz range, considering electromagnetic wave propagation characteristics, device technologies are very competitive. Both GaAs and Si device technologies can provide required specifications for the present mobile systems. Future mobile communication systems will require much higher linearity with higher power efficiency for RF amplifiers and higher complexities with lower dc power dissipation for digital signal processors. In this rump session, we would like to discuss key technology for future wireless systems. This session mainly covers topics for transistor technologies, MMIC technologies including planar waveguides both for Si and GaAs.

Rump B (18:00-20:00, August 30, 2000)

Title: Carbon Nanotube: Fundamental Physics , Application and Future Prospects

Moderators: K. Matsumoto (ETL)
N. Yokoyama (Fujitsu Labs.)

Panelists: S. Iijima (NEC) T. Ando (Univ. of Tokyo)
K. Tsukagoshi (Riken) T. Kuzumaki (Univ. of Tokyo)
Y. Saito (Mie Univ.) H. Tokumoto (NAIR)

The carbon nanotube has a self-organising one-dimensional structure with a specific transportation characteristics and is expected to be an important material for the electronics in the next generation. The purpose of this rump session is to overview the features of the carbon nanotube from variety of theoretical, experimental, and application aspects and is to consider the future prospects of the carbon nanotube. From the theoretical aspect, the specific electron transport characteristics, quantum mechanical transport, and contact problems are discussed. In the fundamental physical experiment, the fabrication of the new carbon nanotube structure, the electron spin injection and transport in the nanotube, and a single electron characteristics are discussed. One of the most expected application of the nanotube is the field emitter. At the high applied electric field, the structure of the nanotube is deformed thereby emitting the electron. This feature is applicable to the field emitter flat panel display. Another important application of the nanotube is the ultra-sharp cantilever for the atomic force microscope (AFM). Owing to the small size of the nanotube, the resolution of the AFM could be greatly enhanced. From these theoretical and experimental results, we would like to discuss the usefulness, problems, and future prospects of the carbon nanotube.

SHORT COURSES

Two short courses will be held on August 28, 2000 for young engineers and students. The courses consist of five lectures relating to the following topics. Most lectures are given in Japanese.

Short Course I

"Quantum Communication and Quantum Computing in the Internet Era in the 21st Century"

Organizer: N. Yokoyama (Fujitsu Labs.)

The arrival of the Internet era has made E-Life and E-Commerce commonplace realities, increasing the demand for even higher degrees of secure communications. As the recent cracking into Japan's governmental offices signifies, the security level of the current internet can be very low. Against this background, quantum encryption and quantum communication have earned increased attention as communication means that ensure complete privacy of communications. The progress of computer technologies facilitated factorization into prime factors. Some experts pointed out that encryption codes, which were regarded as being practically impossible to decipher, might be deciphered at a fraction of the time. In an effort to overcome such problems, research and development activities related to quantum computing are on the increase, mainly in the United States, because quantum computing is recognized as a critically important technology for national defense.

For this tutorial seminar, we have invited five leading researchers in this area to explain the basic theories, to report on the progress of current experiments, and to discuss the future development of these technologies.

1. Mathematical Theory for Quantum Information Science

O. Hirota (Tamagawa Univ.)

2. Quantum Teleportation

A. Furusawa (Nikon)

3. Possibility of Quantum Cryptography and Quantum Protocols

K. Nakamura (NEC)

4. Quantum Computation: Concept, Algorithm and Decoherence Problem

A. Hosoya (Tokyo Inst. of Technol.)

5. Experiments on quantum computers

S. Takeuchi (Hokkaido Univ.)

Short Course II

"Semiconductor Integrated Circuit Technology for Realizing High-Performance Extremely Low-Power Mobile Information Terminals"

Organizer: K. Kotani (Tohoku Univ.)

Semiconductor integrated circuit technologies are getting into Giga-scale integration and GHz operation era, where several difficulties arise and LSI's must be designed and fabricated near its physical limit. In the situation, it is necessary to execute required research and development systematically and strategically. This short course is aiming at covering technologies required for realization of high-performance extremely low-power mobile information terminals which are strongly demanded for creating highly-sophisticated information society where people can utilize

an advanced network to play an active role freshly. In this short course, we have invited five leading researchers to explain basic technologies and discuss future strategies from their individual technological positions.

1. Low Power Integrated Circuit Technologies for High-Performance Extremely Low-Power Mobile Information Terminals

T. Sakurai (Univ. of Tokyo)

2. Low Power LSI Design (Tentative)

K. Torki (CMP)

3. RF Analog Circuits and Layout Techniques

T. Tsukahara (NTT)

4. SOI Device Technology for Low-Power LSI Applications

M. Yoshimi (Toshiba)

5. The Non-Volatile Memory Technology and Its Application for Reconfigurable Devices

H. Takasu (Rohm)

ORGANIZING COMMITTEE

Chairperson: T. Ohmi (*Tohoku Univ.*)

Vicechairperson: Y. Horiike (*Univ. of Tokyo*)

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Y. Aoyagi (*RIKEN*)

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H. Hasegawa (*Hokkaido Univ.*)

K. Ohta (*Sharp*)

T. Hattori (*Sony*)

T. Okabe (*SIRIJ*)

M. Hirose (*Hiroshima Univ.*)

K. Okumura (*Toshiba*)

F. Ichikawa (*Ok Electric*)

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K. Tada (*Yokohama Natl. Univ.*)

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R. Ito (<i>Meiji Univ.</i>)	K. Tanaka (<i>JRCAT</i>)
T. Kamiya (<i>NIAD</i>)	K. Taniguchi (<i>Osaka Univ.</i>)
R. Komatsubara (<i>Tokyo Electron</i>)	T. Tsurushima (<i>Kumamoto Technoplis Foundation</i>)
H. Komiya (<i>Selete</i>)	H. Tsuya (<i>Sumitomo Sitix</i>)
K. Kugimiya (<i>Matsushita Electric</i>)	Y. Yasuda (<i>Nagoya Univ.</i>)
K. Maeguchi (<i>Matsushita Electric</i>)	K. Yodoshi (<i>Sanyo Electric</i>)

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H. Ahmed (<i>Univ. Cambridge</i>)	Z.J. Li (<i>Tsinghua Univ.</i>)
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C.Y. Chang (<i>Nat'l Chiao Tung Univ.</i>)	K.H. Ploog (<i>Paul-Drude-Inst.</i>)
B.Y.S. Chen (<i>Inst. Microelec. Sci.</i>)	D. Scharfetter (<i>Intel</i>)
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L. Esaki (<i>Science & Technology Promotion Foundation of Ibaraki</i>)	S. Tanaka (<i>International Superconductivity Technology Center</i>)
J.S. Harris (<i>Stanford Univ.</i>)	A. Wieder (<i>Siemens</i>)
S.J. Hillenius (<i>Bell Labs. Lucent Technol.</i>)	

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Vicechairpersons: Y. Arakawa (*Univ. of Tokyo*)
Secretary: K. Masu (*Tokyo Inst. of Technol.*)
M. Yokoyama (*Tohoku Univ.*)
Treasurer: S. Sugawa (*Tohoku Univ.*)
M. Hirayama (*Tohoku Univ.*)
Local Arrangement: K. Kotani (*Tohoku Univ.*)
H. Nakase (*Tohoku Univ.*)

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Vice chairperson A. Matsuzawa (*Matsushita Electronics*)
N. Yokoyama (*Fujitsu Labs.*)
Secretary: T. Kondo (*Univ. of Tokyo*)
Subcommittee Members:

[1] Advanced Silicon Circuits and Systems

Chair: T. Shibata (*Univ. of Tokyo*)
Members: T. Aoki (*Tohoku Univ.*)
M. Ikeda (*Univ. of Tokyo*)
T. Morie (*Hiroshima Univ.*)
M. Yamashina (*NEC*)

[2] Advanced Silicon Devices and Device Physics

Chair: S. Kawamura (*Fujitsu*)
Members: S. Deleonibus (*LETI*)

D. Hisamoto (*Hitachi*)

K. Ishimaru (*Toshiba*)

T. Kuroi (*Mitsubishi Electric*)

S. Odanaka (*Osaka Univ.*)

N. Sano (*Univ. of Tsukuba*)

K. Takeuchi (*NEC*)

[3] Silicon Process / Materials Technologies

Chair:

T. Kikkawa (*Hiroshima Univ.*)

Members:

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T. Hattori (*Sony*)

H.-K. Kang (*Samsung Electronics*)

H. Katsuhiko (*Toshiba*)

M. Hori (*Nagoya Univ.*)

N. Kobayashi (*Hitachi*)

M. Okuyama (*Osaka Univ.*)

S. Saito (*NEC*)

M. Sekine (*ASET*)

K. Yamabe (*Univ. of Tsukuba*)

[4] High-Speed/High-Frequency Devices and Circuits

Chair:

K. Honjo (*NEC*)

Members:

Y. Itoh (*Mitsubishi Electric*)

K. Joshin (*Fujitsu Labs.*)

H. Kondo (*Hitachi*)

M. Muraguchi (*NTT Elec.*)

D. Pavlidis (*Solid State Electronics Lab.*)

S. Watanabe (*Toshiba*)

[5] Optoelectronic Devices

Chair: H. Ishikawa (*Fujitsu Labs.*)

Members: Y. Nakano (*Univ. of Tokyo*)

H. Sugo (*NEC*)

S. Tanaka (*Hitachi*)

Y. Tohmori (*NTT*)

H. Wada (*Oki Electric*)

W. Wei (*Chinese Academy Sci.*)

[6] Compound Semiconductor Materials and Device Processes

Chair: Y. Horikoshi (*Waseda Univ.*)

Members: K. Ando (*Tottori Univ.*)

K. Imanishi (*Fujitsu Labs.*)

T. Ishibashi (*NTT*)

T. Oka (*Hitachi*)

T. Okumura (*Tokyo Metropolitan Univ.*)

K. Ploog (*Forschungsverbund Berlin e. V*)

[7] Novel Devices , Physics, and Fabrication

Chair: K. Matsumoto (*ETL*)

Members: H. Ahmed (*Univ. of Cambridge*)

S.Y. Chou (*Princeton Univ.*)

N. Horiguchi (*Fujitsu Labs.*)

K. Maezawa (*Nagoya Univ.*)

A. Toriumi (*Univ. of Tokyo*)

Y. Miyamoto (*Tokyo Inst. of Technol.*)

J.-S. Tsai (*NEC*)

[8] New Materials and Characterization

Chair:

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Members:

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H. Kawasaki (*Motorola*)

M. Miyao (*Kyushu Univ.*)

S. Miyazaki (*Hiroshima Univ.*)

K. Nikawa (*NEC*)

I. C. Noyan (*IBM*)

S. Takagi (*Toshiba*)

E. Tokumitsu (*Tokyo Inst. of Technol.*)

[9] Low Power Circuits and Devices

Chair:

K. Ishibashi (*Hitachi*)

Members:

S. Kawahito (*Shizuoka Univ.*)

S. Kawashima (*Fujitsu Labs.*)

T. Kuroda (*Keio Univ.*)

H. Makino (*Mitsubishi Electric*)

[10] Silicon-on-Insulator Technologies

Chair:

M. Yoshimi (*Toshiba*)

Members:

T. Ipposhi (*Mitsubishi Electric*)

Y. Kado (*NTT*)

K. Mitani (*Shinetsu Electronics*)

T. Sugii (*Fujitsu Labs.*)

T. Tsuchiya (*Shimane Univ.*)

[11] Non-Volatile Memories

Chair:

K. Yoshikawa (*Toshiba*)

Members:

Y. Arimoto (*Fujitsu Labs.*)

T. Kobayashi (*Hitachi*)

T. Nakamura (*Rohm*)

T. Okazawa (*NEC*)

T. Otsuki (*Matsushita Electronics*)

[12] Widegap Semiconductor Materials and Devices

Chair:

H. Kawai (*Sony*)

Members:

H. Amano (*Meijo Univ.*)

S. Chichibu (*Univ. of Tsukuba*)

Y. Koide (*Kyoto Univ.*)

Y. Ohno (*NEC*)

H. Okumura (*ETL*)

A. Suzuki (*Sharp*)

[13] Quantum Nanostructures/Devices/Physics

Chair:

Y. Arakawa (*Univ. of Tokyo*)

Members:

K. Asakawa (*FESTA*)

K. Hirakawa (*Univ. of Tokyo*)

Y. Hirayama (*NTT*)

K. Nakamura (*NEC*)

M. Sugawara (*Fujitsu Labs.*)

K. Tsutsui (*Tokyo Inst. of Technol.*)

[14] Photonic Integration and Packaging

Chair:

T. Maruno (*NTT*)

Members:

M. Fujiwara (*NEC*)

K. Kashiwabara (*Furukawa Electric*)

K. Tanaka (*Fujitsu*)

H. Uetsuka (*Hitachi Cable.*)

[15] System-Level Packaging Technologies

Chair:

A. Matsuzawa (*Matsushita Electronics*)

Members:

Y. Kohara (*Oki Electric*)

M. Minamizawa (*Fujitsu*)

K. Ohtsuka (*Meisei Univ.*)

T. Sudo (*Toshiba*)


PREFACE

I would like to welcome you to the 2000 International Conference on Solid State Device and Materials (SSDM2000) on behalf of the Organizing Committee. You will enjoy very much this SSDM2000 due to its well organized program covering widely distributed technology fields from system, circuits and devices to processes, materials and packaging in order to improve the system performance, I believe. At the beginning of 21st century facing with IT revolutionary era, most urgent issue is an establishment of the very advanced global network and the very advanced networked personal-use terminals which strictly request highly advanced system performance. Those very advanced high performance systems will be produced under the very well organized collaborations among all these widely distributed technologies such as system, algorithm, architecture, circuit, device, process, material and packaging. Thus, the SSDM has widened the technology fields described above in order to enhance exciting and focussed discussions among engineers and researchers engaging in these wide variety technology fields.

This year, we have selected 235 papers including 16 late news papers among 359 papers submitted from 18 countries (Japan, Korea, Taiwan, U.S.A., Singapore, U.K., Germany, China, India, Italy, Russia, Belgium, Brazil, Egypt, France, Hong Kong, Israel, and the Netherlands). In addition, we have invited 39 distinguished invited speakers from various technological fields including four plenary session speakers. The plenary session is organized by four invited talks. They are "The relationship between Stanford and Start Ups in Silicon Valley: the Perspective of Valley CEOs," "SOP and SOC: the Best of Both," "Required Device Technologies for Future Photonic Networks," and "The Role of Microfabrication in the Coming 'Century of Biology'," covering major issues in the recent advances in the solid state devices and materials technology. We do hope you're enjoying the SSDM2000.

Finally, I would like to thank all the authors, participants and committee members for their support for the SSDM2000.

August 2000



Tadahiro Ohmi
Chairperson of the Organizing Committee, SSDM2000
Professor of Tohoku University

SSDM Awards

There are three categories of awards for authors presented papers at the SSDM; the SSDM Award, the SSDM Paper Award and SSDM Young Researcher Award. The SSDM Award will be presented to researchers who contributed an outstanding paper at past SSDM. This award is selected by the Organizing Committee. The SSDM Paper Award will be presented to the authors who presented the most excellent paper at the previous year's SSDM. The SSDM Young Researcher Award will be given to a few young researchers, not older than thirty, who presented excellent papers at the previous year's SSDM. The SSDM Paper Award and the SSDM Young Researcher Award are selected by the Program Committee and decided at the Organizing Committee.

SSDM2000 presents the SSDM award to Dr. T. Warabisako, Dr. I. Yoshida, and Dr. T. Tokuyama for their contribution to the development of the threshold voltage control of MOS transistor by the channel ion implantation which has been evaluated as one of the key technologies as well as LOCOS technology for isolation and poly-silicon gate technology to establish MOSLSI era. They presented a paper entitled "Properties of MOS Structures Prepared on Substrates having Ion-Implanted Impurity Distribution Profile" at the 4th conference of Solid State Devices (previous name of SSDM) in 1972.

The SSDM Paper Award is presented to A. C. Irvine, Z. A. K. Durrani and H. Ahmed for their paper entitled "A High-Speed, Silicon-Based Few-Electron Memory Gain Cell."

The SSDM Young Researcher Award is given to three researchers. 1) H. Nakamoto who presented a paper entitled "A Pattern Matching Processor Using Analog-Digital Merged Architecture Based on Pulse Width Modulation," 2) T. Saida who presented a paper entitled "Silica-Based 2X2 Multimode Interference Couplers with Arbitrary Power Splitting Ratio," and 3) M. Hizukuri who presented a paper entitled "Measurement of Dynamic Strain during Ultrasonic Au-Bumping on Si Chip."

Main Hall**P: Opening Session (9:00-12:10)****9:00 P-0**

Welcome Address, T. Ohmi, Organizing Committee Chairperson

9:10 P-1 (Plenary)**9:50 P-2 (Plenary)****10:10 P-3 (Plenary)****11:00 P-4 (Plenary)****11:40 P-5**

SSDM Award Presentation

12:10 Lunch**Tuesday, August 29****Room A****A-1: Silicon Process/Materials Technologies - MOS Devices / Interconnects I - (13:30-15:30)**Chairperson: T. Kikkawa, *Hiroshima Univ.*H.K. Kang, *Samsung Electronics***13:30 A-1-1 (1005)**

Integrated Circuit Challenges, from Transistors to Packages

M. Bohr, *Intel, U.S.A.***14:00 A-1-2 (64)**

New Mechanisms and the Characterization of Plasma Charging Enhanced Hot Carrier Effect in Deep-Submicron N-MOSFET's

S.J. Chen, H.L. Kao, S.S. Chung, C.C. Chen, C.Y. Chang and H.C. Lin*, *National Chiao Tung Univ. and *National Nano Device Lab., Taiwan***14:15 A-1-3 (157)**

Indium Profile Control for Super Steep Retrograde (SSR) Well

T. Matsuda, A. Mineji, N. Nishio and H. Kitajima, *NEC, Japan***14:30 A-1-4 (314)**

A Study on Mechanism of Chemical Mechanical Polishing on Al and Cu Surfaces Employing In-situ Infrared Spectroscopy

H. Ogawa, Y. Tokuyama, M. Yanagisawa*, J. Kikuchi** and Y. Horiike, *Univ. of Tokyo, *Speedfam-IPEC and **Axiomatec, Japan***14:45 A-1-5 (265)**

Characterization of Tungsten Carbide as Diffusion Barrier for Cu Metallization

S.J. Wang, H.Y. Tsai and S.C. Sun*, *National Cheng Kung Univ., Taiwan and *Wafertech, USA***15:00 A-1-6 (310)**

Aluminum Chemical Vapor Deposition Technology for High Deposition Rate and Surface Morphology Improvement

C.-H. Lee, T. Nishimura, K. Masu and K. Tsubouchi, *Tohoku Univ., Japan***15:15 A-1-7 (112)**

Novel Nozzle-Scan Coating Method for Low-k Films

R. Nakata, N. Yamada, A. Kajita, S. Ito, K. Okumura, T. Kitano*, M. Morikawa*, K. Takeshita*, Y. Esaki* and M. Akimoto*, *Toshiba and *Tokyo Electron Kyushu, Japan*

15:30-15:45 Break

A-2: Silicon Process/Materials Technologies - Interconnects II - (15:45-17:45)Chairperson: N. Kobayashi, *Hitachi*

Y. Furumura, *Fujitsu Labs.*

15:45 **A-2-1 (1016)**
Reliability and Electromigration Failure Modes in Dual Inlaid Cu Interconnects
C. Capasso, *Motorola, U.S.A.*

16:15 **A-2-2 (1006)**
Copper Electrodeposition; Principles and Recent Progress
J. Reid, *Novellus Systems, U.S.A.*

16:45 **A-2-3 (175)**
Ultra-Thin Silicon Oxynitride Films as Cu Diffusion Barrier for Lowering Interconnect Resistivity
T. Nanbu, K. Sekine, Y. Saito, S. Nakao, M. Hirayama and T. Ohmi, *Tohoku Univ., Japan*

17:00 **A-2-4 (297)**
Copper Ion Drift Rates in Porous Methylsilsequiazane Dielectric Films
S. Mukaigawa, T. Oda, T. Aoki*, Y. Shimizu* and T. Kikkawa, *Hiroshima Univ. and *Tonen, Japan*

17:15 **A-2-5 (12)**
Dielectric Breakdown and Light Emission in Copper Damascene Structure under Bias-Temperature Stress
K. Takeda, K. Hinode, J. Noguchi and H. Yamaguchi, *Hitachi, Japan*

17:30 **A-2-6 (44)**
Evaluation of PECVD a-SiC:H as a Cu Diffusion Barrier Layer of Cu Dual Damascene Process
S.G. Lee, H.-S. Oh, H.-J. Shin, J.-G. Hong, H.-D. Lee and H. Kang, *Samsung Electronics, Korea*

18:30-20:30 Banquet

Wednesday, August 30

A-3: Silicon Process/Materials Technologies - DRAM Process I - (9:30-10:30)

Chairperson: K. Hieda, *Toshiba*
 M. Okuyama, *Osaka Univ.*

9:00 **A-3-1 (1007)**
Influence of Lattice Distortion and Oxygen Defects in BST Films for Memory Capacitors
N. Fukushima, K. Abe, S. Niwa, T. Aoyama, M. Kiyotoshi, S. Yamazaki, M. Izuha, K. Eguchi, K. Hieda and T. Arikado, *Toshiba, Japan*

9:30 **A-3-2 (288)**
Inductive-Coupled RF Magnetron Plasma Deposition of (Ba, Sr)TiO₃ for Decoupling Capacitors
N. Fujiwara, T. Kikkawa, S. Miyazaki, F. Nishiyama and M. Hirose, *Hiroshima Univ., Japan*

9:45 **A-3-3 (163)**
Gas Phase Reactions in the MOCVD of (Ba,Sr)TiO₃ Films: A Study by Microdischarge Optical Emission Spectroscopy
S. Momose, T. Nakamura and K. Tachibana, *Kyoto Univ., Japan*

10:00 **A-3-4 (188)**
Effects of Step Coverage, CI Content and Deposition Temperature in TiN Top Electrode on the Reliability of Ta₂O₅ and Al₂O₃ MIS Capacitor for 0.13 μ m Technology and Beyond
H.S. Lim, S.B. Kang, I.S. Jeon, G.H. Choi, Y.W. Park, S.I. Lee and J.T. Moon, *Samsung Electronics, Korea*

10:15 **A-3-5 (192)**
Suppression of Storage Node Contact Distortion for Gigabit-Scale DRAM with COB Structure
D.H. Kim, H. Jeoung, H.S. Kim, J.H. Park, K.H. Yeom, S.Y. Kim, J.M. Park, T.K. Kim, J.S. Kim, D.K. Park, Y.J. Park and J.W. Park, *Samsung Electronics, Korea*

10:30-10:45 Break

A-4: Silicon Process/Materials Technologies - DRAM Process II - (10:45-12:00)

Chairperson: N. Fukushima, *Toshiba*
 T. Hattori, *Sony*

10:45 A-4-1 (67)

Optimisation of CoSi₂ Based Electrical Fuses for Redundancy Implementation in Sub-0.13µm Embedded DRAM Applications

C. Kothandaraman, S.K. Iyer*, J.J. Wu* and S.S. Iyer*, *Infineon Technol. and *IBM, USA*

11:00 A-4-2 (20)

An Experimental Study of Reliability Improvement of a Semiconductor Memory Device with a Novel Self-Protected Fuse-Box Technique Using a Poly-Si Etch Stopper

C.-H. Lee, Y.-H. Park, M.-H. Han, E.-Y. Min, W.-H. Jang and W.-S. Lee, *Samsung Electronics, Korea*

11:15 A-4-3 (295)

Reverse Short Channel Effects in Shallow Trench Isolated MOSFET

H. Lim, J.-M. Youn, S.J. Hong, J.-H. Kim, K.-J. Kim and K.-T. Kim, *Samsung Electronics, Korea*

11:30 A-4-4 (181)

An Advanced Room Temperature Cleaning Using a pH Controlled Ozonated Ultrapure Water

I. Yokoi, G.-M. Choi and T. Ohmi, *Tohoku Univ., Japan*

11:45 A-4-5 (176)

Strategy in Cleaning Processes for Future Materials

G.-M. Choi, F. Pipia and T. Ohmi, *Tohoku Univ., Japan*

12:00-13:30 Lunch

A-5: Silicon Process/Materials Technologies - Gate Insulator - (13:30-15:30)

Chairperson: T. Hattori, *Sony*
K. Hieda, *Toshiba*

13:30 A-5-1 (174)

Ultra-Thin Silicon Oxynitride Film Grown at Low-Temperature by Microwave-Excited High-Density Kr/O₂/N₂ Plasma

K. Ohtsubo, Y. Saito, K. Sekine, M. Hirayama, S. Sugawa, H. Aharoni and T. Ohmi, *Tohoku Univ., Japan*

13:45 A-5-2 (264)

High Performance NMOS Devices Using Ultra-Thin VHP Oxynitride

T.Y. Luo, H.N. Al-Shareef*, A. Karamcheti*, V.H.C. Watt*, G.A. Brown*, M.D. Jackson*, H.R. Huff*, B. Evans** and D.L. Kwong, *Univ. of Texas, *International Sematech and **Gasonics International, USA*

14:00 A-5-3 (135)

Ultrathin Fluorinated Silicon Nitride Gate Dielectric Films Formed by Plasma Enhanced Chemical Vapor Deposition Employing NH₃ and SiF₄

H. Ohta, A. Nagashima, M. Hori and T. Goto, *Nagoya Univ., Japan*

14:15 A-5-4 (296)

Novel Nitrogen Profile Control Technology in Ultra Thin Gate Oxide for Deep Submicron CMOS

T. Ogura, H. Kotaki, S. Kakimoto, S. Zaima* and Y. Yasuda*, *Sharp and *Nagoya Univ., Japan*

14:30 A-5-5 (180)

Low Temperature Gate Oxidation MOS Transistor Produced by Kr/O₂ Microwave Excited High-Density Plasma

T. Hamada, Y. Saito, K. Sekine, H. Aharoni and T. Ohmi, *Tohoku Univ., Japan*

14:45 A-5-6 (197)

Dual-Thickness Gate Oxidation Technology with Halogen/Xenon Implantation for Embedded DRAMs

T. Sugizaki, A. Murakoshi*, Y. Ozawa*, T. Nakanishi and K. Suguro*, *Fujitsu Labs. and *Toshiba, Japan*

15:00 A-5-7 (243)

Impacts of Chlorine in CVD-TiN Gate Electrode on the Gate Oxide Reliability in Multiple-Thickness Oxide Technology

M. Moriwaki and T. Yamada, *Matsushita Electronics, Japan*

15:15 A-5-8 (214)

Boron Diffusion in SiO₂ Involving High-Concentration Effects

T. Aoyama, H. Arimoto and K. Horiuchi, *Fujitsu Labs., Japan*

15:30-15:45 Break

A-6: Silicon Process/Materials Technologies - Deposition and Etching - (13:30-15:30)

Chairperson: M. Sekine, *ASET*
Y. Furumura, *Fujitsu Labs*

15:45 A-6-1 (249)

Precise CD-Controlled Gate Etching Using UHF-ECR Plasma
M. Mori, N. Itabashi, H. Ishimura, H. Akiyama, T. Fujii, G. Saito, M. Yoshigai*, M. Kojima, K. Okamoto**, K. Tsujimoto and S. Tachi, *Hitachi, *Hitachi Techno Eng. and **Hitachi ULSI Systems, Japan*

16:00 A-6-2 (328)

Etch Damage of n+Poly-Si Gate Side Wall as Evaluated by Gate Tunnel Leakage Current
H. Murakami, T. Mihara, S. Miyazaki and M. Hirose, *Hiroshima Univ., Japan*

16:15 A-6-3 (179)

Perfectly Etching Uniformity Control of Various Doped Oxide Films Using an Anhydrous HF Gas
H. Arakawa, Y. Shirai and T. Ohmi, *Tohoku Univ., Japan*

16:30 A-6-4 (284)

Theoretical Study on the Formation Process of Empty Space in Silicon (ESS)
K. Mitsutake and Y. Ushiku, *Toshiba, Japan*

16:45 A-6-5 (177)

Impurity Measurement in Specialty Gases Using Atmospheric Pressure Ionization Mass Spectrometer with Two Compartments Ion Source
M. Kitano, Y. Shirai, A. Ohki* and T. Ohmi, *Tohoku Univ., and *Osaka Sanso Kogyo, Japan*

17:00 A-6-6 (274)

Low-Temperature Selective Deposition of Silicon by Time-Modulation Exposure of Disilane and Formation of Silicon Nanowires
S. Yokoyama, K. Ohba, K. Kawamura, T. Kidera and A. Nakajima, *Hiroshima Univ., Japan*

17:15 A-6-7 (24)

Channel Width Dependence of Mobility in Ge Channel Modulation Doped Structures
T. Irisawa, H. Miura, T. Ueno and Y. Shiraki, *Univ. of Tokyo, Japan*

17:30 A-6-8 (248)

In-Situ Impurity Doping in Si_{1-x}yGexCy Epitaxial Growth Using Ultraclean LPCVD
D. Lee, T. Noda, H. Shim, M. Sakuraba, T. Matsuura and J. Murota, *Tohoku Univ., Japan*

18:00-20:00 Rump Session

Thursday, August 31

A-7: Silicon Process/Materials Technologies - Shallow Junctions - (9:00-10:30)

Chairperson: S. Saito, *NEC*
T. Kikkawa, *Hiroshima Univ.*

9:00 A-7-1 (266)

Retarding Mechanism of Si Selective Epitaxial Growth on CMOS Structure due to Doped Arsenic in the Si Substrate
K. Miyano, I. Mizushima and Y. Tsunashima, *Toshiba, Japan*

9:15 A-7-2 (159)

Ultra Shallow Junction Formation for 80 nm CMOS by Controlling Transient Enhanced Diffusion
K. Ohuchi, K. Adachi, A. Murakoshi, A. Hokazono, T. Kanemura, N. Aoki, M. Nishigohri, K. Suguro and T. Toyoshima, *Toshiba, Japan*

9:30 A-7-3 (319)

Characteristics of Boron and Arsenic Ultra-Shallow Junction Using Laser Annealing with Pre-Amorphization Implantation

C.M. Park, K. Min, S.D. Kim, S.A. Prussin, M.K. Han* and J.C.S. Woo, *Univ. of California, USA and *Seoul National Univ., Korea*

9:45 A-7-4 (238)

Ultra-Shallow and Low-Leakage p+n Junctions Formation by Plasma Immersion Ion Implantation (PIII) and Low-Temperature Post-Implantation Annealing

K. Kanemoto, H. Aharoni and T. Ohmi, *Tohoku Univ., Japan*

10:00 A-7-5 (232)

Effect of Silicon Surface Conditions before Cobalt-Silicidation on Ultra Shallow p+-n Junction Properties

Y. Sugita and K. Goto, *Fujitsu Labs., Japan*

10:15 A-7-6 (70)

The Formation of High Temperature Stable Co-Silicide from Co_{1-x}Tax/Si Systems

D.-H. Lee, D.-H. Ko, H.-J. Choi, J.-H. Ku*, S. Choi*, K. Fujihara*, H.-K. Kang*, S.-H. Oh**, C.-G. Park** and H.-J. Lee***, *Yonsei Univ., *Samsung Electronics, **POSTECH, Korea and ***Stanford Univ., USA*

10:30-10:45 Break

A-8: System-Level Packaging Technologies I (10:45-12:00)

Chairperson: A. Matsuzawa, *Matsushita Electric*

M. Minamizawa, *Fujitsu*

10:45 A-8-1 (1034)

Current State of Research and Development for Electric System Integration

M. Bonkohara, *ASET, Japan*

11:15 A-8-2 (341)

Investigation of ALIVH Substrate for High Frequency Application

T. Nakamura, N. Okazaki*, H. Higashitani, T. Sugawa, D. Andoh, S. Kokufu, Y. Kawakita, F. Echigo, Y. Taguchi, S. Ida* and K. Fukuoka*, *Matsushita Electric and *Matsushita Electronic Components, Japan*

11:30 A-8-3 (235)

Interconnect and Substrate Structure for High Speed Giga-Scale Integration

A. Morimoto, K. Kotani, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

11:45 A-8-4 (308)

GHz Signal Propagation through Transmission Line on ULSI Chip

K. Masu and K. Tsubouchi, *Tohoku Univ., Japan*

12:00-13:30 Lunch

A-9: System-Level Packaging Technologies II (13:30-14:45)

Chairperson: M. Minamizawa, *Fujitsu*

A. Matsuzawa, *Matsushita Electric*

13:30 A-9-1 (1036)

Progress of Three-Dimensional Integration Technology

M. Koyanagi, *Tohoku Univ., Japan*

14:00 A-9-2 (334)

Deep Trench Etching in SOI Wafer for Three-Dimensional LSIs

K.W. Lee, T. Nakamura, Y. Yamada, K.T. Park, H. Kurino and M. Koyanagi, *Tohoku Univ. Japan*

14:15 A-9-3 (340)

Fine Pitch CSP Technology using Au Ball Bumps as External Terminals

S. Nakajyo, M. Onodera, M. Ikumo and T. Kawahara, *Fujitsu, Japan*

14:30 A-9-4 (254)

Dynamic Strain and Its Distribution during Ultrasonic Flip Chip Bonding

M. Hizukuri, N. Watanabe and T. Asano, *Kyushu Inst. of Technol., Japan*

Tuesday, August 29

Room B

B-1: Advanced Silicon Devices and Device Physics I (13:30-15:30)

Chairperson: K. Ishimaru, *Toshiba*
T. Kuroi, *Mitsubishi Electric*

13:30 B-1-1 (262)

Deuterium Effect on Both Interface-State Generation and Stress-Induced-Leakage-Current under Fowler-Nordheim Electron Injection

Y. Mitani, H. Satake, H. Ito and A. Toriumi, *Toshiba, Japan*

13:45 B-1-2 (52)

Quantitative Understanding of Electron Mobility Limited by Coulomb Scattering in MOSFETs with N₂O and NO Oxynitrides

T. Ishihara, S. Takagi and M. Kondo, *Toshiba, Japan*

14:00 B-1-3 (25)

The Impact for Gate Oxide Scaling (32A-12A) and Power Supply for Sub-0.1 μ m CMOSFETs

W.K. Yeh, C.Y. Lin, S.M. Cheng, C.T. Huang, H.H. Shih, J.K. Chen and F.T. Liou, *United Microelectronics, Taiwan*

14:15 B-1-4 (303)

Surface Channel Metal Gate CMOS with Light Counter Doping and Single Work Function Gate Electrode

K.T. Nishinohara, Y. Akasaka, T.Saito, A. Yagishita, A. Murakoshi, K. Suguro and T. Arikado, *Toshiba, Japan*

14:30 B-1-5 (150)

High Density 0.16 μ m Embedded-DRAM-ASIC Process Technology for a SoC Platform

J. Ida, H. Tanaka, K. Fukuda, M. Takeda, H. Shinohara, N. Nakayama, E. Seo, K. Yoshida, H. Higashino, Y. Miyakawa, M. Kageyama, Y. Harada, M. Matsumoto, T. Inoue and F. Yokoyama, *Okai Electric, Japan*

14:45 B-1-6 (119)

70nm NMOSFET Fabrication with 12nm n⁺-p Junctions Using As²⁺ Low Energy Ion Implantations

B.Y. Choi, S.K. Sung, B.G. Park and J.D. Lee, *Seoul National Univ., Korea*

15:00 B-1-7 (152)

Self-Aligned Pocket Implantation into Elevated Source/Drain MOSFETs for Reduction of Junction Capacitance and Leakage Current

N. Miura, Y. Abe, K. Sugihara, T. Oishi, T. Furukawa, T. Nakahata, K. Shiozawa, S. Maruno and Y. Tokuda, *Mitsubishi Electric, Japan*

15:15 B-1-8 (45)

A Novel T-Shaped Shallow Trench Isolation Technology Using Sidewall Spacer for 512Mbit Flash Memories and Beyond

S.H. Hong, D.H. Ahn, M.H. Park, T.K. Kim, H.K. Kang and J.T. Moon, *Samsung Electronics, Korea*

15:30-15:45 Break

B-2: Advanced Silicon Devices and Device Physics II (15:45-17:45)

Chairperson: D. Hisamoto, *Hitachi*
K. Takeuchi, *NEC*

15:45 B-2-1 (1004)

20nm MOS Devices for the Birth of the 21st Century, the Era of Ultimate CMOS

S. Deleonibus, *LETI, France*

16:15 B-2-2 (165)

A Study of the VTH Fluctuation for 25nm CMOS

K. Takeuchi, R. Koh and T. Mogami, *NEC, Japan*

16:30 B-2-3 (16)

Comparison of Sub-Bandgap Impact Ionization in Deep-Sub-Micron Conventional and Lateral Asymmetrical Channel nMOSFETs

A.K. G., S. Mahapatra*, V.R. Rao* and I. Eisele, *Univ. der Bundeswehr Munich, Germany and *Indian Inst. of*

Technol., India

16:45 B-2-4 (129)

Impact of Strained-Si Channel on CMOS Circuit Performance under the Sub-100 nm Regime
T. Hatakeyama, K. Matsuzawa and S. Takagi, *Toshiba, Japan*

17:00 B-2-5 (268)

Improved Low Temperature Characteristics of Raised Source and Drain (RSD) Si_{1-x}Ge_x PMOSFET's
H.J. Huang, K.M. Chen, T.Y. Huang, G.W. Huang* and C.Y. Chang, *National Chiao Tung Univ. and *National Nano Device Labs., Taiwan*

17:15 B-2-6 (195)

Measurement of Hole Transport Parameters in Ultra-Thin SiGe Layers and Their Application in 2D Device Simulations of Heterojunction pMOSFETs
R.J.P. Lander, Y.V. Ponomarev, W.B. de Boer, R. Loo* and M. Caymax*, *Philips Res. Labs., The Netherlands and *IMEC, Belgium*

17:30 B-2-7 (102)

Bandgap and Strain Engineering in SiGe Heterojunction Bipolar Transistors
K. Yuki, K. Toyoda, T. Takagi, Y. Kanazawa, K. Nozawa, T. Saitoh and M. Kubo, *Matsushita Electric, Japan*

18:30-20:30 Banquet

Wednesday, August 30

B-3: Advanced Silicon Devices and Device Physics III (9:00-10:30)

Chairperson: S. Deleonibus, *LETI*
N. Sano, *Univ. of Tsukuba*

9:00 B-3-1 (62)

Edge Direct Tunneling (EDT) Induced Drain and Gate Leakage in Ultrathin Gate Oxide MOSFETs
K.N. Yang, H.T. Huang, M.J. Chen, Y.M. Lin*, M.H. Yu*, S.M. Jang*, C.H. Yu* and M.S. Liang*, *National Chiao Tung Univ. and *TSMC, Taiwan*

9:15 B-3-2 (19)

Quantitative Evaluation of Quantum Mechanical Influence on Flat-Band Capacitance of Poly-Si/SiO₂/Si Substrate System and the Impact of Oxide Charge Density
A. Shimizu and Y. Omura, *Kansai Univ., Japan*

9:30 B-3-3 (320)

Modeling of the Series Resistance for Below 100nm MOSFET Regime
S.-D. Kim, C.-M. Park and J.C.S. Woo, *Univ. of California, USA*

9:45 B-3-4 (94)

Compact Expressions for Crosstalk of Multiple Bit Lines in DRAM
H. Lin, Y.-T. Lai and S.-C. Wong*, *National Chung Hsing Univ. and *TSMC, Taiwan*

10:00 B-3-5 (54)

Statistical Threshold Fluctuations in Si-MOSFETs: Jellium vs. Atomistic Dopant Variations
N. Sano, M. Tomizawa* and K. Natori, *Univ. of Tsukuba and *NTT, Japan*

10:15 B-3-6 (168)

Characteristic of Electron Pumps Based on Silicon Coulomb Blockade Devices
T. Altebaeumer and H. Ahmed, *Univ. of Cambridge, U.K*

10:30-10:45 Break

B-4: Advanced Silicon Devices and Device Physics IV (10:45-11:15)

Chairperson: S. Kawamura, *Fujitsu*
S. Deleonibus, *LETI*

10:45 B-4-1 (1003)

The Vertical Replacement-Gate (VRG) MOSFET: A High-Performance Vertical MOSFET with

Lithography-Independent Critical Dimensions
J. Hergenrother and D. Monroe, *Bell Lab., U.S.A.*

11:15-12:00 Late News

12:00-13:30 Lunch

B-5: New Materials and Characterization - High K Gate Dielectrics - (13:30-15:30)

Chairperson: H. Iwai, *Tokyo Inst. of Technol.*
A.I. Kingon, *North Carolina State Univ.*

13:30 B-5-1 (1017)

A Comparison of SiO₂-Based Alloys as High Permittivity Gate Dielectrics
A.I. Kingon and J.-P. Maria, *North Carolina State Univ., U.S.A.*

14:00 B-5-2 (204)

Study on Zr-Silicate Interfacial Layer of ZrO₂-MIS Structure Fabricated by Pulsed Laser Ablation Deposition Method
T. Yamaguchi, H. Satake and A. Toriumi, *Toshiba, Japan*

14:15 B-5-3 (31)

Charge Trapping in SiO_x/ZrO₂ Gate Dielectric Stacks
M. Housaa, M. Naili*, M.M. Heyns* and A. Stesmans, *Katholieke Univ. Leuven and *IMEC, Belgium*

14:30 B-5-4 (22)

Chemical Bonding at Interfaces between Si (100) and High-K Dielectrics: Competing Effects of i) Process Gas-Substrate and ii) Film Deposition Reactions
G. Lucovsky, H. Niimi, R. Johnson, J.G. Hong, R. Therrien and B. Rayner, *North Carolina State Univ., USA*

14:45 B-5-5 (4)

Degradation of Ta₂O₅ Gate Dielectric by TiCl₄-Based Chemically Vapor Deposited TiN Film in W/TiN/Ta₂O₅/Si System
J.W. Lee, C.H Han, J.-S Park and J.W Park, *Hyundai Electronics, Korea*

15:00 B-5-6 (120)

High Quality Ultrathin TaO_xNy Gate Dielectric Prepared by Nitridation of Ta₂O₅
H. Jung, K. Im, S. Jeon, D. Yang* and H. Hwang, *KJIST and *Jusung Eng., Korea*

15:15 B-5-7 (74)

TaO_xNy Gate Dielectric with Improved Thermal Stability
H.-J. Cho, D.-G. Park, I.-S. Yeo, J.-S. Roh and J.-M. Hwang, *Hyundai Electronics, Korea*

15:30-15:45 Break

B-6: New Materials and Characterization - Gate Oxide Reliability - (15:45-17:30)

Chairperson: S. Takagi, *Toshiba*
G. Lucovsky, *North Carolina State Univ.*

15:45 B-6-1 (21)

Intrinsic Limitations on Ultimate Device Performance and Reliability from Transition Regions at i) Si-Dielectric Interfaces and ii) Internal Interfaces
G. Lucovsky, *North Carolina State Univ., USA*

16:00 B-6-2 (226)

The Polarity Dependence of Soft-Breakdown Characterization for Ultra-Thin Gate Oxides Affected by Nitrogen and Fluorine
C.S. Lai and T.S. Chao*, *Chang Gung Univ. and *National Nano Device Lab., Taiwan*

16:15 B-6-3 (327)

Temperature-Dependent Soft Breakdown in Ultrathin Gate Oxides
W. Mizubayashi, Y. Yoshida, M. Narasaki, S. Miyazaki and M. Hirose, *Hiroshima Univ., Japan*

16:30 B-6-4 (63)

A Novel Sphere-Based Statistical Model for "Local Oxide Thinning" Induced Gate Oxide Breakdown

H.-T. Huang and M.-J. Chen, *National Chiao Tung Univ., Taiwan*

16:45 **B-6-5 (205)**

Impact of TDDB Distribution Function on Lifetime Estimation in Ultra-Thin Gate Oxides

H. Satake and A. Toriumi, *Toshiba, Japan*

17:00 **B-6-6 (29)**

Gate Oxide Reliability Concern Associated with X-Ray Lithography

B.J. Cho, S.J. Kim, C.H. Ang, C.H. Ling, M.S. Joo* and I.S. Yeo*, *National Univ. of Singapore, Singapore and *Hyundai Electronics, Korea*

17:15 **B-6-7 (246)**

Microscopic Observation of X-Ray Irradiation Damages in Ultra-Thin SiO₂ Films

K. Ohmori, T. Goto, H. Ikeda, A. Sakai, S. Zaima and Y. Yasuda, *Nagoya Univ., Japan*

17:30 **B-6-8 (14)**

A Strong Temperature-Dependent Hole⁴ Direct Tunneling Current in p⁺-Gate/pMOSFET with Ultra-Thin Gate Oxide

C.-H. Ang, C.-H. Ling, Z.-Y. Cheng and B.-J. Cho, *National Univ. of Singapore, Singapore*

18:00-20:00 Rump Session

Thursday, August 31

B-7: New Materials and Characterization - Surface and Interface Control - (9:00-10:30)

Chairperson: S. Zaima, *Nagoya Univ.*

 S. Miyazaki, *Hiroshima Univ.*

9:00 **B-7-1 (155)**

Non-Equilibrium Structures of Si/SiO₂ and Si/SiO_xN_y Interfaces

J. Ushio, J. Schulte* and T. Maruizumi, *Hitachi, Japan and *Univ. of Technol., Sydney, Australia*

9:15 **B-7-2 (220)**

Chemical Structures of Oxynitrides/Si(100) Interface

H. Kato, K. Takahashi, H. Nohira, N. Tamura*, K. Hikazutani*, S. Sano* and T. Hattori, *Musashi Inst. of Technol. and *Fujitsu, Japan*

9:30 **B-7-3 (221)**

SiO₂/Si(111) Interface Structures Formed by Atomic Oxygen

K. Takahashi, H. Nohira, T. Nakamura, T. Ohmi* and T. Hattori, *Musashi Inst. of Technol. and *Tohoku Univ., Japan*

9:45 **B-7-4 (161)**

Atomic Scale Characterization of Nitridation Process on Si(100)-2x1 Surfaces by Radical Nitrogen

D. Matsushita, H. Ikeda, A. Sakai, S. Zaima and Y. Yasuda, *Nagoya Univ., Japan*

10:00 **B-7-5 (261)**

Theoretical Calculations for the Elimination of Silanol and Decrease in Dielectric Constant

A. Fujimoto and O. Sugiura, *Tokyo Inst. of Technol., Japan*

10:15 **B-7-6 (213)**

Molecular Orbital Calculations of Sulfur Doping Reactions in Diamond CVD

H. Zhou, Y. Yokoi, H. Tamura, K. Sugisako, S. Takami, M. Kubo, A. Miyamoto, A. Imamura*, M.N. Gamo** and T. Ando**, *Tohoku Univ., *Hiroshima Kokusai Gakuin Univ. and **CREST, Japan*

10:30-10:45 Break

B-8: New Materials and Characterization - Novel Devices and Fabrication - (10:45-11:45)

Chairperson: T. Fuyuki, *Nara Inst. Science of Technol.*

 E. Tokumitsu, *Tokyo Inst. of Technol.*

10:45 **B-8-1 (91)**

Ion Irradiation Stimulated Crystal Nucleation in Amorphous Si on SiO₂

M. Miyao, I. Tsunoda, T. Sadoh and A. Kenjo, *Kyushu Univ., Japan*

11:00 B-8-2 (278)
Selective Single-Crystalline-Silicon Growth on Non-Alkali Glass
A. Hara and N. Sasaki, *Fujitsu Labs., Japan*

11:15 B-8-3 (95)
Hot Carrier Effect in Low Temperature Poly-Silicon Thin Film Transistors
Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura* and Y. Tsuchihashi*, *Nara Inst. of Science and Technol. and *Matsushita Electric, Japan*

11:30 B-8-4 (80)
Simple Process for Buried Nanopyramid Array (BNPA) Fabrication by Means of Dopant Ion Implantation and Dual Wet Etching
M. Koh, T. Goto, A. Sugita, T. Tanii, T. Shinada, T. Matsukawa* and I. Ohdomari, *Waseda Univ. and *ETL, Japan*

11:45-13:30 Lunch

B-9: New Materials and Characterization - Metal Gate and New Characterization - (13:30-15:00)

Chairperson: M. Niwa, *Matsushita Electric*
M. Miyao, *Kyushu Univ.*

13:30 B-9-1 (312)
A Guideline for Accurate Two-Frequency Capacitance Measurement for Ultra-Thin Gate Oxides
A. Nara, N. Yasuda, H. Satake and A. Toriumi, *Toshiba, Japan*

13:45 B-9-2 (136)
Spin-Dependent Trap-Assisted Tunneling Current in Ultra-Thin Gate Dielectrics
Y. Miura and S. Fujieda, *NEC, Japan*

14:00 B-9-3 (285)
Non-Destructive and Contactless Monitoring Technique of Si Surface Stress by Photoreflectance
M. Sougawa, T. Kanashima, M. Agata, K. Yamashita, M. Okuyama, A. Fujimoto* and K. Eriguchi**, *Osaka Univ., *Wakayama National College of Technol. and **Matsushita Electronics, Japan*

14:15 B-9-4 (79)
Novel Method of Threshold Voltage Control of Metal Gate CMOSFETs Using Channel Epitaxy
W.S. Kim, S. Song, Y. Khang, T.H. Choe, J.Y. Yoo, N.I. Lee, K. Fujihara, H.K. Kang and J.T. Moon, *Samsung Electronics, Korea*

14:30 B-9-5 (134)
Low Resistivity PVD TaNx/Ta/aNx Stacked Metal Gate CMOS Technology Using Self-Grown bcc-Phased Tantalum on TaNx Buffer Layer
H. Shimada, I. Ohshima, T. Ushiki, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

14:45 B-9-6 (153)
Conformal Platinum Electrodes Prepared by Chemical Vapor Deposition Using a Liquid MeCpPtMe₃ Precursor in an Oxidizing Atmosphere
Y. Matsui, M. Hiratani, T. Nabatame, Y. Shimamoto, K. Imagawa and S. Kimura, *Hitachi, Japan*

Tuesday, August 29

Room C

C-1: Optoelectronic Devices I (13:30-15:30)

Chairperson: Y. Nakano, *Univ. of Tokyo*
H. Wada, *Oki Electric*

13:30 C-1-1 (1010)
Ultrafast Demultiplexing and Bit-Wise Logic Operation of Hybrid-Integrated Symmetric Mach-Zehnder All-Optical Switch
K. Tajima, S. Nakamura, Y. Ueno, J. Sasaki, T. Sugimoto, T. Kato, T. Shimoda, H. Hatakeyama, T. Tamanuki and T. Sasaki, *NEC, Japan*

14:00 C-1-2 (258)
500 GHz Optical Pulse Generation from a Short-Cavity GRIN-SCH-MQW Mode-Locked Laser Diode

S. Arahira, Y. Katoh and Y. Ogawa, *Oki Electric, Japan*

14:15 C-1-3 (115)

Optical BPSK Subcarrier Modulation Using an Integrated Hybrid Device

M. Shin, J. Lim, J. Kim*, J.S. Kim*, K.E. Pyun* and S. Hong, *KAIST and *ETRI, Korea*

14:30 C-1-4 (209)

Variable Wavelength Shifter Using Four-Wave Mixing in a Wavelength Selectable Laser

T. Simoyama, H. Kuwatsuka, M. Bouda, M. Matsuda, Y. Kotaki and H. Ishikawa, *Fujitsu Labs., Japan*

14:45 C-1-5 (131)

Demonstration of All-Optical Wavelength Converter Based on Fabry-Perot Semiconductor Optical Amplifier

M. Saitoh, M. Takenaka, B. Ma and Y. Nakano, *Univ. of Tokyo, Japan*

15:00 C-1-6 (60)

Polarization-Dependent Optical Gain and Gain Saturation in Vertical-Cavity Surface-Emitting Lasers

Y. Takahashi and H. Kawaguchi, *Yamagata Univ., Japan*

15:15 C-1-7 (256)

All-Optical 2-D Serial-to-Parallel Pulse Converter Using an Organic Film with Femtosecond Optical Response

S. Tatsuura, O. Wada, M. Furuki*, M. Tian*, Y. Sato* and L.S. Pu*, *FESTA and *Fuji Xerox, Japan*

15:30-15:45 Break

C-2: Optoelectronic Devices II (15:45-17:45)

Chairperson: H. Ishikawa, *Fujitsu Labs.*

Y. Tohmori, *NTT*

15:45 C-2-1 (1009)

High-Speed Uni-Traveling-Carrier Photodiodes for Fiber-Optic Communications

H. Ito, *NTT, Japan*

16:15 C-2-2 (124)

Velocity Mismatching Effect of Traveling Wave Electroabsorption Modulator

J. Lim, M. Shin, J. Kim*, J.S. Kim*, K.E. Pyun* and S. Hong, *KAIST and *ETRI, Korea*

16:30 C-2-3 (43)

A Novel High Responsivity, Wide Band Silicon Photodiode

T.N. Swe and K.S. Yeo, *Nanyang Technological Univ., Singapore*

16:45 C-2-4 (73)

A New High Radiance LED Structure with Circular 45 Corner Reflector

E.-H. Park, J.-H. Cha and Y.-S. Kwon, *KAIST, Korea*

17:00 C-2-5 (185)

High-Brightness Wafer-Bonded ITO/AlGaInP/Mirror/Si Light Emitting Diodes

R.H. Horng, Y.C. Lien*, W.C. Peng* and D.S. Wu*, *National Chung Hsing Univ. and *Da-Yeh Univ., Taiwan*

17:15 C-2-6 (113)

1.55um Spot-Size Converter Integrated Laser Diodes Fabricated by Selective Area MOVPE Growth with Various Mask Patterns

H.-S. Kim, O.D. Kon*, M.-H. Park*, N. Hwang* and I.-H. Choi, *Korea Univ. and *ETRI, Korea*

17:30 C-2-7 (301)

Front Mirror Absorption Characterization on High-Power GaAs Laser Diodes by Means of Thermoreflectance Technique

S. Emmanuel and T. Baba, *NRLM, Japan*

18:30-20:30 Banquet

Wednesday, August 30

C-3: Non-Volatile Memories - FeRAM I - (9:00-10:30)

Chairperson: T. Otsuki, *Matsushita Electronics*
M. Tsukada, *Fujitsu Labs*

9:00 C-3-1 (1023)

The Role of Ferroelectric Domains in Long Term Reliability
J.T. Evans, *Radiant Technologies, U.S.A.*

9:30 C-3-2 (1024)

Hydrogen-Robust Submicron Ir/PZT/Ir Capacitors for Embedded Ferroelectric Memory
T. Sakoda, *Texas Instruments, U.S.A.*

10:00 C-3-3 (142)

Nonvolatile Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMS)-FETs Using
Pt/SrBi₂Ta₂O₉/Pt/SrTa₂O₆/SiON/Si Structures Operating at 3.5V
E. Tokumitsu, K. Okamoto and H. Ishiwara, *Tokyo Inst. of Technol., Japan*

10:15 C-3-4 (141)

Characterization of Ferroelectric Domain Behavior in MOCVD-PZT Capacitors for CMVP FeRAMs
K. Ito, Y. Mochizuki, T. Tatsumi, N. Inoue, H. Hada, T. Hase and Y. Miyasaka, *NEC, Japan*

10:30-10:45

C-4: Non-Volatile Memories - FeRAM II - (10:45-12:15)

Chairperson: T. Nakamura, *ROHM*
I. Kunishima, *Toshiba*

10:45 C-4-1 (263)

SPM Studies of Hydrogen-Induced Degradation of Pt/PLZT/Pt Capacitors
C. Yoshida, T. Tamura, K. Kondo* and K. Takasaki*, *Fujitsu and *Fujitsu Labs., Japan*

11:00 C-4-2 (299)

Pb Content Control in Sputtered PZT Films for FRAM Mass Production
S. Ozawa, S. Mihara, H. Noshiro, Y. Horii, M. Shibata, T. Takamatsu, M. Nakamura and T. Yamazaki, *Fujitsu, Japan*

11:15 C-4-3 (217)

Studies on Improving Retention Time of Memorized State of MFIS Structure for Ferroelectric Gaet FET Memory
M. Takahashi, H. Sugiyama, T. Nakaiso, M. Noda and M. Okuyama, *Osaka Univ., Japan*

11:30 C-4-4 (323)

A Novel SPICE Model of Ferroelectric Capacitors Using Schmitt Trigger Circuit
S. Yamamoto, T. Kato and H. Ishiwara, *Tokyo Inst. of Technol., Japan*

11:45 C-4-5 (219)

Low-Temperature Preparation of Ferroelectric Sr₂(Ta_{1-x}Nb_x)₂O₇ Thin Films by Pulsed Laser Deposition and Their
Application to MFIS Structure
T. Nakaiso, M. Noda and M. Okuyama, *Osaka Univ., Japan*

12:00 C-4-6 (78)

Electrical Characteristics of Pt/SrBi₂Ta₂O₉/Ta₂O₅/Si Using Ta₂O₅ as the Buffer Layer
H.S. Choi, K.S. Park, Y.T. Kim* and I.-H. Choi, *Korea Univ. and *KIST, Korea*

12:15-13:30 Break

C-5: Non-Volatile Memories - Flash I - (13:30-15:30)

Chairperson: K. Yoshikawa, *Toshiba*
T. Kobayashi, *Hitachi*

13:30 C-5-1 (1022)

Technology Considerations for High-Speed High-Density Embedded Flash
K.-M. Chang, *Motorola, U.S.A.*

14:00 C-5-2 (6)

A Novel P-Channel Flash EEPROM Cell with Simple Process and Low Power Consumption

C.J. Huang, Y.C. Liu, S.F. Hong, A. Wu, M.C. Wang, S. Hsu, L.C. Hsia, Y.J. Chang, Y.T. Lo and F.-T. Liu, *United Microelectronics, Taiwan*

14:15 C-5-3 (36)

Electrical Characterization of a Triple Self-Aligned Split-Gate Flash Cell for 0.18um Embedded Application

J. Yan, C. Gruensfelder, A. Schmidt, K. Kim, R. Mih*, J. Harrington*, K. Houlihan*, H.K. Lee*, K. Chan*, J. Johnson*, B. Chen*, C. Lo**, D. Lee**, A. Levi**, C. Lam* and D. Shum, *Infineon Technologies, *IBM and **Silicon Storage Technology, USA*

14:30 C-5-4 (98)

A New Dual Floating Gate Flash Cell for Multilevel Operation

J.T.-Y. Chen, H. Lin and S.-C. Wong*, *National Chung Hsing Univ. and *TSMC, Taiwan*

14:45 C-5-5 (125)

A Body Effect Assisted NOR-Type (BeNOR) Multilevel Flash Memory

Y.-S. Wang, H.-P. Tsai, E.C.-S. Yang, Y.-C. King, S. Chen* and C.C.-H. Hsu, *National Tsing Hua Univ. and *Winbond Electronics, Taiwan*

15:00 C-5-6 (313)

Auger Recombination Enhanced Hot Electron Programming in Flash EEPROMs

N.K. Zous, L. P. Chiang, C.W. Tsai and T. Wang, *National Chio-Tung Univ., Taiwan*

15:15 C-5-7 (326)

On the Capacitance Coupling Ratios of a Source-Side Injection Flash Memory Cell

C.-M. Liu, J. Brennan, Jr., K. Chan, P. Guo, A.V. Kordesch and K.-Y. Su, *Winbond Electronics, USA*

15:30-15:45 Break

C-6: Non-Volatile Memories - Flash II - (15:45-16:45)

Chairperson: T. Okazawa, *NEC*

N. Ajika, *Mitsubishi Electric*

15:45 C-6-1 (61)

Characteristics of Tunneling Nitride Grown by Electron Cyclotron Resonance Nitrogen Plasma Nitridation and Its Application to Low Voltage EEPROM

K.-S. Min and K. Lee*, *Hyundai Electronics and *KAIST, Korea*

16:00 C-6-2 (96)

Analysis of Gate Disturb Degradation by Nitridation of Flash Tunnel Oxide

M. Arai, T. Hashizume, T. Nitta, Y. Odake and I. Matsuo, *Matsushita Electronics, Japan*

16:15 C-6-3 (336)

Simulation of Positive Oxide Trapped Charge Induced Leakage Current and Read-Disturb in Flash EEPROMs

N.K. Zous, C.W. Tsai, L.P. Chiang, C.C. Yeh and T. Wang, *National Chiao-Tung Univ.*

16:30 C-6-4 (318)

Screening for Flash Cells with Retention Related Defects

D. Giardini and F.P. Scarlata, *STMicroelectronics, Italy*

18:00-20:00 Rump Session

Thursday, August 31

C-7: Silicon-on-Insulator Technologies I (9:00-10:30)

Chairperson: M. Yoshimi, *Toshiba*

Y. Kado, *NTT*

9:00 C-7-1 (1020)

Low-Power SOI-CMOS Technology and Its Application to Watch-IC

H. Mikoshiba, M. Hogyoku, A. Ebina, T. Kadowaki, Y. Sato and M. Yamaguchi, *Seiko Epson, Japan*

9:30 C-7-2 (1019)

Low-Power RF Circuits in SOI
M. Harada, *NTT, Japan*

10:00 C-7-3 (321)

Advanced CMOS Technology on Sapphire Substrate for RF Systems on a Chip
Y.-C. Tseng, J.Cable*, M. Stuber*, R. Reedy* and J.C.S. Woo, *Univ. of California and *Peregrine Semiconductor, USA*

10:15 C-7-4 (39)

On the Temperature Dependence of Hysteresis Effect in Floating-Body Partially-Depleted SOI CMOS Circuits
R. Puri, C.T. Chuang, M.B. Ketchen, M.M. Pelella* and M.G. Rosenfield, *IBM and *Univ. of Florida, USA*

10:30-10:45

C-8: Silicon-on-Insulator Technologies II (10:45-12:15)

Chairperson: T. Tsuchiya, *Shimane Univ.*
T. Sugii, *Fujitsu Labs.*

10:45 C-8-1 (130)

A Novel Fabrication Technique of Ultra-Thin and Relaxed SiGe Buffer Layers with High Ge Content for Sub-100 nm Strained Silicon-on-Insulator MOSFETs
T. Tezuka, N. Sugiyama, T. Mizuno, M. Suzuki and S. Takagi, *Toshiba, Japan*

11:00 C-8-2 (210)

Design of SiGe/Buried Oxide Layered Structure to Form Highly Strained Si Layer on Insulator for SOI MOSFETs
N. Sugiyama, T. Mizuno, M. Suzuki and S. Takagi, *Toshiba, Japan*

11:15 C-8-3 (207)

Optimization of Selective Epitaxy Process for Elevated Source/Drain Applicable to 0.15um Fully Depleted CMOS on 25nm SOI
T. Nakamura, H. Matsushashi, Y. Katakura and J. Kanamori, *Oki Electric, Japan*

11:30 C-8-4 (206)

Advanced Co Salicide Technology for Sub-0.20um FD-SOI Devices
T. Ichimori, N. Hirashita and J. Kanamori, *Oki Electric, Japan*

11:45 C-8-5 (17)

Proposal of a Partial-Ground-Plane(PGP) Silicon-on-Insulator(SOI) MOSFET for Deep Sub-100-nm Channel Regime
S. Yanagi, A. Nakakubo and Y. Omura, *Kansai Univ., Japan*

12:00 C-8-6 (13)

Reduced Reverse Narrow Channel Effect in Thin SOI nMOSFET's
S.J. Chang, C.Y. Chang, S.D.Wu, T.Y. Huang and T.S. Chao*, *National Chiao Tung Univ. and *National Nano Device Labs., Taiwan*

12:15-13:15 Lunch

C-9: Silicon-on-Insulator Technologies III (13:15-15:00)

Chairperson: T. Ipposhi, *Mitsubishi Electric*
K. Mitani, *Shin-Etsu Electronics*

13:15 C-9-1 (89)

A Single Chip Automotive Control LSI Using SOI BiCDMOS
K. Kawamoto, S. Mizuno, H. Abe, Y. Higuchi, S. Fujino and I. Shirakawa*, *Denso and *Osaka Univ., Japan*

13:30 C-9-2 (255)

SOI-MOS/Diode Composite Photodetector Device
Y. Uryu and T. Asano, *Kyushu Inst. of Technol., Japan*

13:45 C-9-3 (1021)

Substrate Characteristics of Nanocleave(TM) SOI Wafers

Malik, I.J., *Silicon Genesis, U.S.A.*

14:15 C-9-4 (81)

Evaluation of SOI Substrates by Positron Annihilation

A. Ogura, A. Uedono* and S. Tanigawa*, *NEC and *Univ. of Tsukuba, Japan*

14:30 C-9-5 (110)

Charging Damage of SOI Wafer Diagnosed by Scanning Maxwell-Stress Microscopy

T. Matsukawa, H. Fujii*, S. Kanemaru, M. Nagao, H. Yokoyama and J. Itoh, *ETL and *Kobe Steel, Japan*

14:45 C-9-6 (211)

Thermally-Induced Structural Changes of Ultrathin Silicon-on-Insulator Structure

R. Nuryadi, Y. Ishikawa and M. Tabe, *Shizuoka Univ., Japan*

Room D

Tuesday, August 29

D-1: Novel Devices, Physics, and Fabrication - Novel Electron Devices - (13:30-15:15)

Chairperson: Y. Miyamoto, *Tokyo Inst. of Technol.*

K. Maezawa, *Nagoya Univ.*

13:30 D-1-1 (1015)

Organic Transistors for Logic and Flexible Display Applications

A. Dodabalapur, B. Crone, J.A. Rogers, Z. Bao, Y.Y. Lin, V.R. Raju and H.E. Katz, *Bell Labs., U.S.A.*

14:00 D-1-2 (208)

Ultra-Low Biased Field Emitter Using Single Wall Carbon Nanotube Directly Grown onto Silicon Tip by Thermal CVD

K. Matsumoto, S. Kinoshita, Y. Gotoh and M. Ishii*, *ETL and *CREST, Japan*

14:15 D-1-3 (90)

High Performance MOS Tunneling Cathode with CoSi₂ Gate Electrode

T. Sadoh, Y. Zhang, H. Yasunaga, A. Kenjo, T. Tsurushima and M. Miyao, *Kyushu Univ., Japan*

14:30 D-1-4 (247)

Resonant Tunneling Cathodes Using GaAs/AlAs Quantum Structures

H. Mimura, K. Okamura, Y. Neo, H. Shimawaki and K. Yokoo, *Tohoku Univ., Japan*

14:45 D-1-5 (315)

An Evidence for Ballistic Transport in Nanocrystalline Porous Silicon Layer by Time-of-Flight Measurements

A. Kojima and N. Koshida, *Tokyo Univ. of Agri. and Technol., Japan*

15:00 D-1-6 (234)

Highly Sensitive MISFET Sensors for Detecting CO Gas Using Porous Platinum and Tungsten Oxide Thin Films

H. Fukuda, R. Zohnishi and S. Nomura, *Muroran Inst. of Technol., Japan*

D-2: Novel Devices, Physics and Fabrication - Single Electron Devices I - (15:45-18:00)

Chairperson: A. Toriumi, *Univ. of Tokyo*

N. Horiguchi, *Fujitsu Labs.*

15:45 D-2-1 (1014)

Quantised Current in One Dimensional Channels Induced by Surface Acoustic Waves

M. Pepper, *Univ. of Cambridge, U.K.*

16:15 D-2-2 (30)

Properties and Applications of a Novel Electroacoustic Interaction in GaAs Resonant Tunneling Structures

A.B. Hutchinson, V.I. Talyanskii, M. Pepper, G. Gumbs*, G.R. Aizin**, D.A. Ritchie and E.H. Linfield, *Univ. of Cambridge, UK, *Hunter College of the City Univ. and **Univ. of New York, USA*

16:30 D-2-3 (105)

Single-Electron Transistors with Two Self-Aligned Gates

K. Nishiguchi and S. Oda, *Tokyo Inst. of Technol., Japan*

16:45 D-2-4 (169)

Structural and Electrical Characterization of Nanocrystalline Silicon (nc-Si) Single Electron Transistors
Y.T. Tan, T. Kamiya, Z.A.K. Durrani and H. Ahmed, *Univ. of Cambridge, U.K.*

17:00 D-2-5 (270)

SET/CMOS Hybrid for Future Low-Power LSI -Experimental Demonstration, Power Estimation, and Strategy for Its Reduction-
K. Uchida, J. Koga, R. Ohba and A. Toriumi, *Toshiba, Japan*

17:15 D-2-6 (271)

Novel Si Quantum Memory Structure with Self-Aligned Stacked Nanocrystalline Dots
R. Ohba, N. Sugiyama, J. Koga, K. Uchida and A. Toriumi, *Toshiba, Japan*

17:30 D-2-7 (304)

Transient Characteristics of Electron Charging in Si-Quantum-Dot Floating Gate MOS Memories
A. Kohno, H. Murakami*, M. Ikeda*, H. Nishiyama*, S. Miyazaki* and M. Hirose*, *Fukuoka Univ and *Hiroshima Univ., Japan*

17:45 D-2-8 (170)

Single Electron Charging Phenomena in Silicon Nano-Pillars With and Without Silicon Nitride Tunnel Barriers
D.M. Pooley, H. Ahmed, H. Mizuta* and K. Nakazato*, *Univ. of Cambridge and *Hitachi Cambridge Lab., U.K.*

18:30-20:30 Banquet

Wednesday, August 30

D-3: Novel Devices, Physics and Fabrication - Single Electron Devices II - (9:00-10:30)

Chairperson: J.-S. Tsai, *NEC*
K. Matsumoto, *ETL*

9:00 D-3-1 (200)

Analog Computation Using a Quantum-Dot Cell Network
N.-J. Wu, K. Saito and H. Yasunaga*, *Univ. of Aizu and *Univ. of Electro-Communications, Japan*

9:15 D-3-2 (198)

A Multi-Quantum-Dot Associative Circuit Using Thermal-Noise Assisted Tunneling
T. Matsuura, T. Morie, M. Nagata and A. Iwata, *Hiroshima Univ., Japan*

9:30 D-3-3 (1013)

Single Far-Infrared Photon Detection Using an SET
O. Astafiev, *Univ. of Tokyo, Japan*

10:00 D-3-4 (151)

Single FIR-Photon Detection Using an RF-SET
T. Kutsuwa, V. Antonov*, O. Astafiev* and S. Komiyama, *Univ. of Tokyo and *JST, Japan*

10:15 D-3-5 (332)

Novel Single Electron Memory Device Using Metal Nano-Dots and Schottky In-Plane Gate Quantum Wire Transistors
H. Okada and H. Hasegawa, *Hokkaido Univ., Japan*

10:30-10:45 Break

D-4: Quantum Semiconductor Materials and Devices - Quantum Dots - (10:45-12:15)

Chairperson: R.-H. Blick, *Univ. of Munich*
M. Sugawara, *Fujitsu Labs.*

10:45 D-4-1 (1035)

Quantum Dots
R. Deutschmann and G. Abstreiter, *Germany*

11:15 D-4-2 (203)

Lasng Characteristics and Carrier Dynamics of 1.3-um InGaAs/GaAs Quantum Dot Lasers

Y. Nakagawa, M. Sugawara, K. Mukai*, Y. Nakata* and H. Ishikawa, *Tokyo Inst. of Technol. and *Fujitsu Labs., Japan*

11:30 D-4-3 (146)

InAs Self-Assembled Quantum Dots Coupled with GaSb Monolayer Quantum Well

M. Yamaguchi, Y. Sugiyama, Y. Nakata, T. Ohshima*, H. Sasakura**, S. Muto**, Y. Awano and N. Yokoyama, *Fujitsu, *Fujitsu Labs. and **Hokkaido Univ., Japan*

11:45 D-4-4 (202)

A Model of Carrier Capturing and Recombination Process in Quantum-Dot System: Influence of Excitation Power on Spontaneous Emission Intensity and Lifetime

K. Mukai, Y. Nakata and M. Sugawara, *Fujitsu Labs., Japan*

12:00 D-4-5 (186)

Memory Operation of InAs Quantum Dot Field Effect Transistor

H. Son, J. Kim, M. Kim* and S. Hong, *KAIST and *Samsung Electronics, Korea*

12:15-13:30 Lunch

D-5: Quantum Nanostructures/Devices/Physics - Quantum Nanostructures - (13:30-15:30)

Chairperson: Y. Arakawa, *Univ. of Tokyo*

K. Tsutsui, *Tokyo Inst. of Technol.*

13:30 D-5-1 (1028)

Nano-electromechanical Systems and Single Electron Tunneling

R.H. Blick, *Univ. of Munich, Germany*

14:00 D-5-2 (286)

Back-Gated Point Contact

K. Hashimoto, S. Miyashita*, T. Saku and Y. Hirayama, *NTT and *NTT-AT, Japan*

14:15 D-5-3 (333)

Ridge Uniformity Improvement Toward Growth of Sub-10nm InGaAs Ridge Quantum Wires by Selective MBE on Patterned InP Substrate

C. Jiang, T. Muranaka and H. Hasegawa, *Hokkaido Univ., Japan*

14:30 D-5-4 (167)

UHV-STM Study of Electron Emission from Individual Silicon Nanopillars

P.A. Lewis, B.W. Alphenaar *and H. Ahmed, *Univ. of Cambridge and *Hitachi Cambridge Lab., U.K.*

14:45 D-5-5 (302)

Kelvin Probe Force Microscopy for Surface Potential Measurements on InAs Nanostructures Grown on (110) GaAs Vicinal Substrates

S. Ono, M. Takeuchi* and T. Takahashi, *Univ. of Tokyo and *RIKEN, Japan*

15:00 D-5-6 (162)

Control of Thermal Emission by Using Periodic Microstructures

A. Ueda, F. Kusunoki, J. Takahara and T. Kobayashi, *Osaka Univ., Japan*

15:15 D-5-7 (269)

Spherical SiGe Quantum Dots Prepared by Thermal Evaporation Method

Y.-C. Liao, S.-Y. Lin, S.-C. Lee and C. Chia*, *National Taiwan Univ. and *N.N.U., Taiwan*

15:30-15:45 Break

D-6: Quantum Nanostructures/Devices/Physics - Tunneling and Spin Related Phenomena - (15:45-17:45)

Chairperson: G. Abstreiter, *Technical Univ. of Munich*

K. Hirakawa, *Univ. of Tokyo*

15:45 D-6-1 (1030)

Spin-Polarized Current Injection in Ferromagnetic Semiconductor Heterostructures

Y. Ohno, D.K. Young*, B. Beschoten*, F. Matsukura, H. Ohno and D.D. Awschalom*, *Tohoku Univ., Japan and *UC,*

Santa Barbara, U.S.A.

16:15 D-6-2 (339)

Fabrication of Hollow Cylinder Shape Permalloy on the Si Pole

Y.-G. Hong, N. Nakamura, K.-T. Park, M. Sasaki, H. Kurino, K. Hane and M. Koyanagi, *Tohoku Univ., Japan*

16:30 D-6-3 (237)

THz Emission due to Miniband Transport in GaAs/AlGaAs Superlattices

Y. Shimada, T. Matsuno and K. Hirakawa, *Univ. of Tokyo, Japan*

16:45 D-6-4 (212)

Terahertz Electromagnetic Wave Generation from Quantum Nanostructure

I. Morohashi, K. Komori*, T. Hidaka, T. Sugaya*, X.L. Wang*, M. Ogura* and T. Nakagawa*, *Shonan Inst. of Technol. and *ETL, Japan*

17:00 D-6-5 (173)

Phase Breaking Effect Appearing in I-V Characteristics of Double-Barrier Resonant-Tunneling Diodes -Theoretical Fitting Over Four Orders of Magnitude -

M. Nagase, K. Furuya and N. Machida, *Tokyo Inst. of Technol., Japan*

17:15 D-6-6 (275)

Formation Process of High-Field Domain in Superlattices Observed by Photoluminescence Spectra Branch

M. Hosoda, N. Ohtani*, C. Domoto* and T. Aida*, *Osaka City Univ. and *ATR, Japan*

17:30 D-6-7 (87)

Nonlinear Dynamics of Periodic Electric-Field Domains in Quantum Well Infrared Photodetectors

M. Ryzhii, V. Ryzhii, R. Suris* and C. Hamaguchi**, *Univ. of Aizu, Japan, *A.F. Ioffe Physical-Technical Inst. RAS, Russia and **Osaka Univ., Japan*

18:00-20:00 Rump Session

Thursday, August 31

D-7: Compound Semiconductor Materials and Device Processes I (9:00-10:30)

Chairperson: Y. Watanabe, *Fujitsu Labs.*

T. Oka, *Hitachi*

9:00 D-7-1 (1011)

Modern Processing Technology for 6-inch GaAs Wafers

Bayraktaroglu, B., *ANADIGICS, U.S.A.*

9:30 D-7-2 (329)

In-Situ XPS Study of Etch Chemistry of Methane-Based RIBE of InP Using N₂

Z. Jin, H. Takahashi, T. Hashizume and H. Hasegawa, *Hokkaido Univ., Japan*

9:45 D-7-3 (164)

Vertical High Quality Mirrorlike Facet of GaN-Based Device by Reactive Ion Etching

C.H. Chen, Y.K. Su, S.J. Chang, J.K. Sheu and I.C. Lin, *National Cheng Kung Univ., Taiwan*

10:00 D-7-4 (337)

Lateral Thickness Modulation of InGaAs/GaAs Structures by Selective Area MOVPE

T. Terasawa, F. Nakajima, J. Motohisa and T. Fukui, *Hokkaido Univ., Japan*

10:15 D-7-5 (139)

Nitrogen Doping into Cu₂O Thin Films Deposited by Reactive Sputtering Method

S. Ishizuka, S. Kato, T. Maruyama and K. Akimoto, *Univ. of Tsukuba, Japan*

10:30-10:45 Break

D-8: Compound Semiconductor Materials and Characterization (10:45-12:00)

Chairperson: T. Ando, *Tottori Univ.*

K. Horikoshi, *Waseda Univ.*

10:45 D-8-1 (324)

Field Effect Photoluminescence from Excitons Bound to Nitrogen Pairs in GaAs

K. Onomitsu, T. Okabe, T. Makimoto*, H. Saito* and Y. Horikoshi, *Waseda Univ. and *NTT, Japan*

11:00 D-8-2 (300)

Strain Relaxation Mechanism in the Growth of InAs on GaAs(110) Surfaces Studied by Scanning Tunneling Microscopy

H. Yamaguchi and N. Oyama*, *NTT and *Keio Univ., Japan*

11:15 D-8-3 (305)

Initial Stage of InGaAs Growth on GaAs Multiatomic Steps by MOVPE

S. Lee, M. Akabori, T. Shirahata*, J. Motohisa and T. Fukui, *Hokkaido Univ. and *Air Water, Japan*

11:30 D-8-4 (287)

Fabrication of Periodically Domain-Inverted AlGaAs Quasi-Phase-Matched Devices by GaAs/Ge/GaAs Sublattice Reversal Epitaxy

S. Koh, T. Kondo, Y. Shiraki and R. Ito*, *Univ. of Tokyo and *Meiji Univ., Japan*

11:45 D-8-5 (9)

Resonance-Induced Modification of Spatially Direct and Indirect Stark Ladder Transitions in a GaAs/AlAs Superlattice p-I-n Diode

T. Nogami, T. Takeda and K. Fujiwara, *Kyushu Inst. of Technol., Japan*

12:00-13:30 Lunch

D-9: Compound Semiconductor Materials and Device Processes II (13:00-15:00)

Chairperson: T. Ishibashi, *NTT*
T. Fukui, *Hokkaido Univ.*

13:30 D-9-1 (1012)

Device Technology for InP/InGaAs HBT Lightwave Communication ICs

S. Yamahata, M. Ida, K. Kurishima, H. Nakajima and E. Sano, *NTT, Japan*

14:00 D-9-2 (230)

High Linearity and High Power Device Fabricated by Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As Double Doped-Channel Heterostructure

F.-T. Chien and Y.-J. Chan*, *Chino-Excel Technol. and *National Central Univ., Taiwan*

14:15 D-9-3 (37)

High-Linearity and Current-Enhancement Camel-Gate Field Effect Transistor Utilizing Delta-Doping Channels

J.-H. Tsai, *Chien Kuo Inst. of Technol., Taiwan*

14:30 D-9-4 (187)

A Thermal Resistance Measurement of HBT with Pulsed Current I-V Setup and Its Scalability with the Total Emitter Area

H.-M. Park, S.-H. Cheon and S. Hong, *KAIST, Korea*

14:45 D-9-5 (330)

DLTS, PL and CL Study of Dominant Deep Level and Its Removal in InGaP/GaAs Heterostructure Grown by TBP-Based GSMBE

F. Ishikawa, A. Hiramama and H. Hasegawa, *Hokkaido Univ., Japan*

Room E

Tuesday, August 29

E-1: Widegap Semiconductor Materials and Devices - ZnO and SiC Devices - (13:30-15:30)

Chairperson: Y. Koide, *Kyoto Univ.*
H. Okumura, *ETL*

13:30 E-1-1 (1026)

Can ZnO Eat Market in Optoelectronic Applications?

M. Kawasaki, *Tokyo Inst. of Technol., Japan*

14:00 E-1-2 (99)

Electrical and Structural Properties of Ti/Au Ohmic Contacts on N-ZnO:Al
H.-K. Kim, S.-H. Han, K.-K. Kim, W.-K Choi* and T.-Y Seong, *KJIST and *KIST, Korea*

14:15 E-1-3 (250)

C-V Characteristics of ZnO Thin-Film Field Effect Transistor Structures Formed on Glass Substrates
Y. Ohmaki, S. Kishimoto, Y. Ohno, F. Matsukura, H. Ohno, K. Saikusa*, T. Aita*, A. Ohtomo* and M. Kawasaki*,
*Tohoku Univ. and *Tokyo Inst. of Technol., Japan*

14:30 E-1-4 (1027)

Recent Progress in SiC MOS and Ion Implantation Technologies for High Power Devices
T. Kimoto, H. Yano, N. Miyamoto and H. Matsunami, *Kyoto Univ., Japan*

15:00 E-1-5 (172)

Passivation of Deep Levels in 3C-SiC on Si by a Hydrogen Plasma Treatment
M. Kato, F. Sobue, M. Ichimura, E. Arai, N. Yamada*, Y. Tokuda** and T. Okumura***, *Nagoya Inst. of Technol.,
*Toyota Central Res. and Develop. Labs., **Aichi Inst. of Technol. and ***Tokyo Metropolitan Univ., Japan*

15:15 E-1-6 (292)

Radiation Hardness of Epitaxial and Non-Epitaxial 6H-SiC MOS Capacitors
E.A. de Vasconcelos, E.F. da Silva Jr., T. Katsube*, S. Yoshida* and Y. Nishioka**, *Univ. Federal de Pernambuco,
Brazil, *Saitama Univ. and ** TI Tsukuba Res. and Development Center, Japan*

15:30-15:45 Break

E-2: Widegap Semiconductor Materials and Devices - GaN Devices - (15:45-17:30)

Chairperson: | H. Amano, *Maijo Univ.*
| Y. Ohno, *NEC*

15:45 E-2-1 (1025)

Physics of GaN-based Electronic Devices
M.S. Shur, R. Gaska and A. Khan, *Rensselaer Polytechnic Inst., U.S.A.*

16:15 E-2-2 (47)

Computational Chemistry Study on Crystal Growth Process of InGaN/GaN
Y. Inaba, T. Onozu, S. Takami, M. Kubo, A. Miyamoto and A. Imamura*, *Tohoku Univ. and *Hiroshima Kokusai
Gakuin Univ., Japan*

16:30 E-2-3 (316)

Electronic Structure of InGaN Quantum Dots in GaN: Atomic Scale Calculations
T. Saito and Y. Arakawa, *Univ. of Tokyo, Japan*

16:45 E-2-4 (183)

The Study of GaN and InGaN Metal-Semiconductor-Metal Photodetectors with Different Schottky Contact Metals
Y.K. Su, F.S. Juang*, S.J. Chang, Y.C. Chiou and J.K. Shiu, *National Cheng Kung Univ. and *National Huwei Inst. of
Technol., Taiwan*

17:00 E-2-5 (149)

AlGaIn/GaN Heterojunction High Electron Mobility Transistors Using Ga-Polarity Crystal Growth by Plasma-Assisted
Molecular Beam Epitaxy
T. Ide, M. Shimizu*, A. Suzuki**, X.-Q. Shen*, H. Okumura* and T. Nemoto, *Meiji Univ., *ETL and **Tokai Univ.,
Japan*

17:15 E-2-6 (322)

Room Temperature Electron Mobility in AlGaIn/GaN Heterostructures Grown on Sapphire Substrate by MOCVD
T. Someya, K. Hoshino and Y. Arakawa, *Univ. of Tokyo, Japan*

18:30-20:30 Banquet

Room E

Wednesday, August 30

E-3: Advanced Silicon Circuits and Systems I (9:00-10:30)

Chairperson: M. Yamashina, *NEC*
M. Ikeda, *Univ. of Tokyo*

9:00 E-3-1 (1002)

Fingerprint Identification System on a Single Chip Based on Advanced Circuit and Device Technologies
S. Shigematsu, H. Morimura, Y. Tanabe, K. Machida and H. Kyuragi, *NTT, Japan*

9:30 E-3-2 (144)

Eliminating Needless Calculations on Circuit Level: Most-Significant-Digit-First Digit-Serial Processing
T. Nozawa, M. Imai, K. Mochizuki and T. Ohmi, *Tohoku Univ., Japan*

9:45 E-3-3 (240)

A Stacked-CMOS LSI Architecture for Reducing Operation Voltage and Current
M. Nishisaka and Y. Ohtomo, *NTT, Japan*

10:00 E-3-4 (283)

A Dynamically Reconfigurable Processor with Multi-Mode Operation Based on Newly Developed Full-Adder /
D-Flip-Flop Merged Module (FDMM)
S. Sakaidani, N. Miyamoto and T. Ohmi, *Tohoku Univ., Japan*

10:15 E-3-5 (252)

Fast and Compact Central Arbiter for High Access-Bit-Rate Multi-Port Caches
N. Omori, K. Kishi, T. Gyohten, J. Kim and H.J. Mattausch, *Hiroshima Univ., Japan*

10:30-10:45 Break

E-4: Advanced Silicon Circuits and Systems II (10:45-12:15)

Chairperson: T. Shibata, *Univ. of Tokyo*
T. Aoki, *Tohoku Univ.*

10:45 E-4-1 (1001)

Prospective of Implantable Microsystem Technology and Experience on the Artificial Vision System
W. Liu, *North Carolina State Univ., U.S.A.*

11:15 E-4-2 (222)

A vMOS Vision Chip Based on the Cellular-Automaton Processing
T. Sunayama, T. Asai, Y. Amemiya and M. Ikebe*, *Hokkaido Univ. and *Dai Nippon Printing, Japan*

11:30 E-4-3 (201)

A High-Resolution Hadamard Transform Circuit Using Pulse Width Modulation Technique
K. Katayama, M. Nagata, T. Morie and A. Iwata, *Hiroshima Univ., Japan*

11:45 E-4-4 (199)

Image Object Extraction Using Resistive-Fuse and Oscillator Networks and a Pulse-Modulation Circuit for Their LSI
Implementation
H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata, *Hiroshima Univ., Japan*

12:00 E-4-5 (106)

A Novel, Large-Scale Packet Switch System and 60 Gbps Arbiter Circuit Operation Using SFQ Technology
S. Yorozu, Y. Kameda and S. Tahara, *NEC, Japan*

12:15-13:30 Lunch

E-5: Low Power Circuits and Devices (13:30-15:30)

Chairperson: T. Kuroda, *Keio Univ.*
K. Ishibashi, *Hitachi*

13:30 E-5-1 (1018)

Optimum Device Parameters and Scalability of Variable Threshold CMOS (VTCMOS)
T. Hiramoto, *Univ. of Tokyo, Japan*

14:00 E-5-2 (137)

Quantitative Study of an SA-Vt CMOS Circuit: Evaluation of Fluctuation in Device and Circuit Performance
G. Ono, M. Miyazaki and K. Ishibashi, *Hitachi, Japan*

14:15 **E-5-3 (111)**

Ultra-Low Standby Current in SOI-CMOS LSI Circuits by Using Body-Bias-Control Technology
K. Higashi, T. Ohmi*, A.O. Adan, H. Morimoto, K. Niimi, T. Ashida and S. Sugawa*, *Sharp and *Tohoku Univ., Japan*

14:30 **E-5-4 (26)**

A 3.26um² Full CMOS SRAM Cell Using Non-Overlap Contacts for Super Low Power Applications
H.S. Ha, J.E. Song, H.S. Chang, K.H. Lee, S.G. Kim, K.J. Kim and K.T. Kim, *Samsung Electronics, Korea*

14:45 **E-5-5 (85)**

Three-Dimensional Capacitance Analysis in an SRAM Cell
Y. Takemura, K. Osada, M. Yagyu, K. Yamaguchi, J. Ushio and T. Maruizumi, *Hitachi, Japan*

15:00 **E-5-6 (331)**

Low-Power Area-Efficient Design of Parallel Pipeline A/D Converters
D. Miyazaki and S. Kawahito, *Shizuoka Univ., Japan*

15:15 **E-5-7 (311)**

Novel FET LSI for OFDM Using Current Mode Circuit
S.-K. Kim, J.-S. Cha, H. Nakase and K. Tsubouchi, *Tohoku Univ., Japan*

15:30-15:45

E-6: High-Frequency / High Speed Devices and Circuits (15:45-17:45)

Chairperson: H. Kondoh, *Hitachi*
 K. Josin, *Fujitsu Labs.*

15:45 **E-6-1 (1008)**

Self-Aligned SiGe HBT Technology for Optical-Fiber-Links and Millimeter-Wave Applications
K. Washio, *Hitachi, Japan*

16:15 **E-6-2 (291)**

Effect of Ti Silicidation on f_{max} and Base Resistance of SiGe Hetero-Junction Bipolar Transistors
S.-Y. Lee, H.-S. Kim, K.-H. Shim and J.-Y. Kang, *ETRI, Korea*

16:30 **E-6-3 (5)**

A New High Speed Switching Bipolar Power Transistor with Corrugated Base Junctions
C. Park, Y. Yoon*, D.J. Kim* and K Lee, *KAIST and *Fairchild Korea Semiconductor, Korea*

16:45 **E-6-4 (116)**

Low Voltage Actuated RF MEMS Switches Using Push-Pull Operation
D. Hah, E. Yoon and S. Hong, *KAIST, Korea*

17:00 **E-6-5 (276)**

Frequency Dispersion in Drain Conductance of InAlAs/InGaAs HEMTs and Its Correlation with Impact Ionization
T. Kosugi, Y. Umeda, T. Suemitsu, T. Enoki and Y. Yamane, *NTT, Japan*

17:15 **E-6-6 (46)**

Accurate Small-Signal Modeling and Parameter Extraction for RF MOSFETs
S. Lee, C.S. Kim* and H.K. Yu*, *Hankuk Univ. of Foreign Studies and *Electronics and Telecommunications Res. Inst., Korea*

17:30 **E-6-7 (309)**

A Silicon RF-CMOS Class-B Push-Pull Power Amplifier for IMT-2000
M. Yokoyama, R. Tachibana, T. Saito, K. Masu and K. Tsubouchi, *Tohoku Univ., Japan*

18:00-20:00 Rump Session

Tuesday, August 29

E-7: Photonic Integration and Packaging I (9:00-10:30)

Chairperson: T. Maruno, *NTT*
H. Uetsuka, *Hitachi Cable*

9:00 E-7-1 (1032)

Terabit Photonic Networks
H. Onaka, *Fujitsu Labs., Japan*

9:30 E-7-2 (1031)

MEMS and Optical Applications
H. Fujita and H. Toshiyoshi, *Univ. of Tokyo, Japan*

10:00 E-7-3 (145)

PLC-Type Hybrid External Cavity Laser Integrated with a Front-Monitor PD on a Si Platform
T. Tanaka, Y. Hibino, T. Hashimoto, R. Kasahara, Y. Inoue, A. Himeno, M. Ito, M. Abe and Y. Tohmori, *NTT, Japan*

10:15 E-7-4 (338)

Hybrid Integrated 8-Channel SOAG Peceptacle Module with Driver Circuits
T. Sugimoto, T. Kato, J. Sasaki, T. Shimoda, H. Hatakeyama, T. Tamanuki, T. Sasaki and M. Itoh, *NEC, Japan*

10:30-10:45 Break

E-8: Photonic Integration and Packaging II (10:45-12:00)

Chairperson: M. Fujiwara, *NEC*
K. Tanaka, *Fujitsu Labs.*

10:45 E-8-1 (1033)

Silica-Based Planar Lightwave Circuits for the Future Photonic Networks
A. Himeno, *NTT, Japan*

11:15 E-8-2 (82)

Wide-Band Thermo-Optic Wavelength Tunable Filter Using Silicone Resin with a Fast Response for WDM Systems
S. Toyoda, N. Ooba, A. Kaneko, M. Hikita, T. Kurihara, A. Tate and T. Maruno, *NTT, Japan*

11:30 E-8-3 (42)

Flat Passband and Low Crosstalk 32ch-50GHz Spacing Multiplexer/Demultiplexer Combined by Two 100GHz Spacing AWGs and FBGs
T. Saito, T. Ota, H. Ogoshi and T. Tsuda, *Furukawa Electric, Japan*

11:45 E-8-4 (298)

A Novel Lithographic Method for Fabricating Three Dimensional Periodic Stacks
T. Matsuura, K. Matsuda and J. Murota, *Tohoku Univ., Japan*