Advanced Program Part II

LATE NEWS PAPERS

Wednesday, September 26

Room B

LB-1:Late News(17:00-17:15)
(System-Level Integration and Packaging Technologies)

17:00 LB-1-1 Micro Bump Interconnection Technologies in 20 μm Pitch on 3D System in Package
T. Morifuji, Y. Tomita, R. Kajiwara and K. Takahashi,
ASET, Japan

Thursday, September 27

Room A

LA-1:Late News (13:40-14:10)
(Silicon Process / Materials Technologies)

13:40 LA-1-1 Direct Growth of Single Crystalline CeO_2 High-k Gate Dielectrics
Y. Nishikawa, N. Fukushima and N. Yasuda,
Toshiba, Japan

13:55 LA-1-2 Influence of Organic Contamination on Reliability and Trap Generation in MOS Devices
T. Yoshino, S. Yokoyama, T. Fujii*, K. Shibahara, A. Nakajima, T. Kikkawa, H. Sunami and Q.D.M. Khosru,
*Hiroshima Univ. and *EBARA Res., Japan*

Room B

LB-2: Late News (17:15 - 17:45)
(Advanced Silicon Devices and Device Physics)

17:15 LB-2-1 GIDL Currents in MOSFETs with High-k Dielectric
S.-I. Chang, J. Lee* and H. Shin,
*KAIST and *Wonkwang Univ., Korea*

17:30 LB-2-2 Antimony Behavior in Laser Annealing Process for Ultra Shallow Junction Formation
K. Shibahara, Y. Ishikawa, D. Onimatsu, N. Maeda, A. Mineji*, K. Kagawa**, A. Matsuno** and T. Nire**,
Hiroshima Univ., NEC and **Komatsu, Japan*

Room C

LC-1: Late News (12:05-12:20)
(Silicon-on-Insulator Technologies)

12:05 LC-1-1 Study on Silicon Optical with T-Shape SiO_2 Waveguide as an Optical Control Gate
H. Kobayashi, Y. Iida and Y. Omura,
Kansai Univ., Japan

Room F

LF-1: Late News (17:00-17:45)
(Organic Semiconductor Devices and Materials)

17:00 LF-1-1 Excimer Laser Crystallization of Amorphous ITO Thin Film Deposited on PES
Y.H. Son, M.S. Park, S.J. Han, J.H. Lee, Y.H. Kim, S.E. Nam and H.J. Kim,
Hong-Ik Univ., Korea

17:15 LF-1-2 Surface Modification Effects on the FET Property of Pentacene Thin Film
M. Yoshida, H. Ushijima, T. Kamata and S. Kobayashi,
AIST, Japan

17:30 LF-1-3 Field-Dependent Mobility of Highly Oriented Pentacene ($C_{22}H_{14}$) Thin Film FETs
T. Komoda, Y. Endo, K. Kyuno and A. Toriumi,
Univ. of Tokyo, Japan

Friday, September 28

Room C

LC-2: Late News (12:05-12:20)
(Non-Volatile Memory Technologies)

12:05 LC-2-1 A New Circuit Simulation Model of Ferroelectric Capacitors
T. Tamura, Y. Arimoto* and H. Ishiwara
*Tokyo Inst. of Technol. and *Fujitsu Labs., Japan*

Room D

LD-1:Late News (12:00-12:30)
(Novel Devices, Physics, & Fabrication)

12:00 LD-1-1 Performance of Silicon Based bi-deirectional Electron Pumps Consisting of Two Coulomb Blockade Devices
T. Altebaeumer and H. Ahmed,
Univ. of Cambridge, UK

12:15 LD-1-2 Single-Electron Detection in Si-Wire Transistors at Room Temperature
A. Fujiwara, K. Yamazaki and Y. Takahashi,
NTT, Japan

LD-1: Late News (16:30-16:45)
16:30 LD-2-1 Non-Volatile Doubly Stacked Si Dot Memory with Si Nano-Crystalline Layer
R. Ohba, N. Sugiyama, K. Uchida, J. Koga and and S. Fujita,
Toshiba, Japan

Withdrawn

Thursday, September 27

Room A

10:20 A-3-5 A New Defect Engineering for Improving nMOSFETs Hot Carrier Immunity by a Low Temperature UHV H_2 Annealing Process
J.W. Park, J.M. Ha, J.R. Ryu, C.S. Kim, S.M. Kim, B.C. Lee, S. Choi, K. Fujihara, H.K. Kang and J.T. Moon
Samsung Electronics, Korea

13:30 A-5-1 Ultrathin Dy-Doped HfO_2 for Gate Dielectric Application
H. Lee, H. Yang, H. Chang, S. Jeon and H. Hwang
KJIST., Korea

13:50 A-5-2 Electrical Characteristics of Ultrathin Pr-Silicate for Gate Dielecrtric Applications
S. Jeon, W. Lee and H. Hwang
KJIST, Korea

16:05 A-6-2 Electrical Properties of MIS-Ta_2O_5/TiO_2 Capacitor for High Density DRAMs
I.-S. Park, J.-H. Yeo, J.-H. Chung, Y. -S. Kim, S.-T. Kim and J.-T. Moon
Samusung Electronics, Korea