SSDM 2002 Advance Program
General Information

DATE
Conference: **September 17-19, 2002**
Short Course: **September 20, 2002(in Japanese)**

LOCATION
NAGOYA CONGRESS CENTER
1-1 Atsuta-Nishimachi, Atsuta-ku, Nagoya 456-0036
TEL 052-683-7711 FAX 052-683-7777
Nagoya Congress Center is approximately 40 minutes by car from Nagoya International Airport, and only 10 minutes by subway from downtown Nagoya.
Web site: http://www.u-net.city.nagoya.jp/ncc/

REGISTRATION (*Deadline of Pre-registration has been changed from August 1 to August 20)
The registration desk will be open from 16 to 20. The registration hours are as follows:

September	16	17:00-19:00		2F lobby
	17	8:00-18:00		"
	18	8:30-18:00		"
	19	8:30-14:00		"
	20	8:30-14:00	(Short Course)	"

Pre-registration is recommended due to the expected large number of participants expected. In order to pre-register for SSDM 2002, the enclosed Registration Form should be returned with your payment by August 20 to the SSDM 2002 Secretariat. Payment should be made in Japanese yen by bank transfer or bank draft payable to the SSDM 2002 Secretariat. **Credit cards are acceptable from every attendee**: Diners, Master Card, VISA and AMEX. No personal checks will be accepted. After your remittance has been received, the receipt and a voucher for the participant's kit will be sent to you by the secretariat in early in September. Students' contribution is encouraged. We are pleased to discount the student registration fee (5,000 yen).

Bank transfer to SSDM A/C No. 075- 2374600 MIZUHO Bank, Hongo Branch, Tokyo
みずほ銀行 本郷支店(店番号(075) (普) 2374600 口座名：SSDM

	Registration Fee		Short Courses in Japanese	Banquet
	On or before August 20	After August 20		
Regular	¥35,000	¥40,000	¥10,000	¥6,000
Student	¥5,000		¥1,000	¥3,000
Accompanying Person				¥3,000

1) The conference registration fee covers the conference attendance and includes a copy of the Extended Abstracts.
2) Student fee of Short Course has been reduced from ¥5,000 to ¥1,000.
3) The short course is presented in Japanese (No Translation).

REGISTRATION CANCELLATION
Conference:
Cancellation fee of ¥3,000 will be deducted from the refund. Cancellation should be made in writing to the SSDM 2002 Secretariat. No cancellation will be accepted after August 25, 2002. Extended Abstracts will be sent to absent registrants after the Conference.

Short Course:
Regular: ¥2,000 will be deducted. Student: No fee will be refund.
Cancellations should be made in writing to the SSDM 2002 Secretariat. No cancellation will be accepted after August 25. A text will be sent to the absent registrants after the Conference.

BANQUET

Banquet will be held at "The Grand Court" of the ANA Hotels, Hotel Grand Court Nagoya (7F) on September 17 from 18:30-20:30. Tickets (Regular ¥6,000 / Student ¥3,000) can be purchased at the registration desk.

LATE NEWS PAPERS

Late News Paper Deadline is July 25, 2002.

Late news papers describing important new developments may be submitted. A 2-page paper must be sent in the camera-ready format as required for the regular papers. The accepted papers will be included in the extended abstracts.
Original 2-page paper plus 15 copies on both sides of a sheet with author application form and copyright transfer form should be sent to SSDM 2002 Secretariat.
Notice of acceptance will be mailed by the middle of August.

EXTENDED ABSTRACTS AND PUBLICATION

Authors of papers accepted for SSDM 2002 are encouraged to submit the original and significant part of the papers to the Special Issue of the Japanese Journal of Applied Physics. The special issue will be published in April 2003.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

Submission of an abstract for review and subsequent acceptance is considered by the committee as an agreement that the work will not be published by the author prior to the presentation at the conference. This policy will be enforced by the automatic withdrawal of the paper by the conference committee.

AWARDS

"SSDM Awards" will be given to excellent papers presented in the previous conferences.
SSDM Award
For the paper, which made an outstanding contribution to the field of solid state devices and materials, among the papers presented prior to 1996.
SSDM Paper Award
For the best paper presented at the last conference.
SSDM Young Researcher Award
For a few excellent papers by young researchers presented at the last conference.

FINANCIAL SUPPORT

Limited financial support for presentations by full time student is available. Student presenter who is interested in the support should directly contact to the secretariat (E-mail: ssdm@bcasj.or.jp) after receiving an accepted letter.

VISA REQUIREMENT

All foreign participants must have valid passport. Participants from countries where a visa is required to enter Japan are recommended to apply at the nearest Japanese embassy in their countries as soon as possible.

OFFICIAL TRAVEL AGENT

JTB Corp. has been appointed as the official travel agent for the conference and will handle accommodations.

JTB Convention Support Center
C/o JTB Event & Convention Service
Koutsu Bldg.6F, 3-13-26 Meieki, Nakamura-ku, Nagoya 450-0002, Japan
Phone:+81-52-541-2521, Fax:+81-52-541-2520
E-mail:jtbecs@cjn.or.jp

HOTEL ACCOMMODATIONS

<Available on the nights of September 15 – 21>

Special rate for the conference has been arranged at the banquet hotel on September 17; ANA Hotels Hotel Grand Court Nagoya.

#	Hotel Name	Single W/bath	Twin W/bath	Location	Grade
①	*ANA Hotels Hotel Grand Court Nagoya**	**¥10,000**	**¥8,000** (per person)	Kanayama Station (walk 1 min)	Deluxe
②	*Nagoya Tokyu Hotel*	**¥13,500**	**¥11,000** (per person)	Subway Station Sakae (walk 5 min)	Deluxe
③	*Cypress Garden Hotel*	**¥9,200**	**¥8,200** (per person)	Kanayama Station (walk 1 min)	Superior
④	*Nagoya Fuji Park Hotel*	**¥8,500**	**¥7,500** (per person)	Subway Station Sakae (walk 2 min)	Standard
⑤	*Princess Garden Hotel*	**¥7,500**	**¥7,000** (per person)	Subway Station Sakae (walk 5 min)	Standard
⑥	*Hotel Econo Nagoya Sakae*	**¥5,900**		Subway Station Sakae (walk 2 min)	Economy

All room rates include breakfast, service charge and consumption tax.

* There is a limousine from the Nagoya airport to ANA Hotels Hotel Grand Court Nagoya. Please access to SSDM Home Page for details.

APPLICATION AND PAYMENT OF DEPOSIT

1. Participants wishing to make reservations for accommodations should complete the application form and return it to JTB by FAX **no later than September 2, 2002.** Reservation should be first come first served basis. Applications for hotel reservations should be accompanied by a deposit of one night room charge plus a handling charge of ¥500 per one room in advance. Please pay for the balance when checking out the hotel.

2. Payments must be made by either one of the following;
   a. Credit cards (**Visa, MasterCard, American Express, Diners, JCB**); Please fill in the Credit Card Authorization in the application form.
   b. Bank transfer; Please remit a deposit of one night room charge plus a handling charge the following account.

Name of bank: **UFJ Bank, Nagoya Ekimae Branch** Name of Account: **JCSC** Account Number: **2354117**

NOTE: Personal checks are not acceptable. We would appreciate your kindly sending us a photocopy of the bank's receipt for your remittance.

CANCELLATION

If you decide to make any changes or cancellations, please inform JTB by FAX. JTB accepts only written notification. The following cancellation fees apply according to the date of your notification.

5 to 2 days prior to the first night	¥1,000
1 day prior to the first night	50% of daily room charge
The first night or no notice given	100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in your home country prior to departure.

CLIMATE

The temperature in Nagoya during the period of the conference ranges between 18℃ and 30℃.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 60 Hz in western Japan including Nagoya and 50 Hz in eastern Japan including Tokyo.

RUMP SESSIONS - September 18 (Wednesday) 19:00-21:00

Rump session A (Room 212, 1F, Bldg.2)

"Toward the 100Gbps/THz Era"

Recent technologies based solid-state devices and materials are providing practical high-speed optoelectronic devices operating at over 40 Gbps. For example, the speed of digital ICs and bandwidths of transistors have been dramatically increased by using SiGe HBTs, InP HEMTs, InP HBTs, and GaN HEMTs. Some ICs are exceeding to 100 Gbps or 100 GHz. Correspondingly, cutoff frequencies of transistors are approaching THz range. Bandwidths of photodetectors and optical modulators are also exceeding 200 GHz and 100 GHz, respectively. These performance races are driven by the strong demands for future networks having large transmission capacity. It is good time to discuss the potential of emerging technologies toward the 100-Gbps era before the applications become concrete.

In the rump session, we would like to informally discuss the flowing issues; (1) Which technology is the most cost-effective in achieving 100-Gbps optical transceivers? (2) What are the device design issues? (3) How will optics and electronics fuse in a chip or a package?

Moderators	Panelists	
M. Rodwell (UC Stanta Barbara, USA)	M. Racanelli (Jazz Semiconductor, USA)	SiGe HBT
O. Wada (Kobe Univ., Japan)	T. Hierl (IQE, USA)	III-V Epitaxy
	M. Rodwell (UCSB, USA)	III-V HBT
	N. Hara (Fujitsu Lab., Japan)	III-V HEMT
Organizers	H. Ito (NTT, Japan)	Photo Detector
T. Enoki (NTT, Japan)	H. Wada (Oki, Japan)	Optical Modulator
K. Kojima (Mitsubishi, Japan)	Y. Ueno (NEC, Japan)	OTDM

Rump session B (Room 211, 1F, Bldg.2)

" Ultimate Device Scaling versus New System Integration: Compete or Cooperate?"

Demand to higher performance and higher packing density in LSIs has accelerated the device size to be scaled down to 50 nm regime. Much smaller device with the gate length of 15 nm has been demonstrated in a research level. However, there exist so many concerns which should be solved in order to realize high performance LSIs using such ultra small device. Then, it is a time just when we should reconsider of device scaling from the viewpoint of system integration. There are possibilities to dramatically improve the system performance by employing new integration technologies combined with package technology, optoelectronic technology, MEMS technology and bio technology even though we use devices with relaxed sizes. Therefore, it is meaningful to discuss which approach of device scaling or system integration is more cost-effective to achieve future high performance systems.

In the rump session, we discuss about the future direction of integration technology from the viewpoint of device scaling based on the technology road map and new silicon integration technology merged with package technology, optoelectronic technology, MEMS technology and bio technology.

Moderators	Panelists	
M. Koyanagi (Tohoku Univ., Japan)	T. Mogami (NEC, Japan)	Device scaling
*Under one more person appointment	T. Nishimura (Mitsubishi, Japan) (pending)	SOI Devices
	A. Matsuzawa (Matsushita, Japan)	LSI Design and SoC
Organizers	Hoi-Jun Yoo (KAIST, Korea)	System Architecture
M. Koyanagi (Tohoku Univ., Japan)	M. Bonkohara (ASET, Japan)	Packaging and SiP
M. Bonkohara (ASET, Japan)	S. Shoji (Waseda Univ., Japan)	MEMS and Bio-chip
	L. G. McIlrath (R3 Logic, USA)	Bio-Inspired Circuit and Systems
	*Under Appointment	Optoelectronic Device and System

SHORT COURSES

Two short courses will be held on September 20 (Friday) for young engineers and students. All lectures are given in Japanese. Please refer the attached information for details.

SSDM 2002 INSTRUCTION for SPEAKERS

<<Oral Presentation>>

Presentation Time

	Session Time	Presentation Time	Discussion
Plenary	45 min.	40 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of the presentation time, Third: End of the discussion time.

Audio-Visual Equipment

The meeting room will contain the following audiovisual equipment:

- Overhead projector
- LCD data projector (PC does not provide)
- Clip-type microphone
- Projection laser pointer

It is strongly recommended that you use the Overhead projector for your presentation.

Authors wishing to present their paper using LCD projector are requested to bring overhead transparencies preparing for an unforeseen accident.

<<Poster Presentation>>

Poster Sessions are scheduled as follows:

16:45-18:45 on Wednesday, September 18

Authors must remain in the vicinity of the bulletin board for the duration of the session to answer questions.

1.8m(W) x 2.1m(H) poster board, a sign indicating your paper number and push pins will be provided at the Shiratori Hall, 1F Bldg.4. Presenters should display, on their poster, the paper title, authors and affiliation.

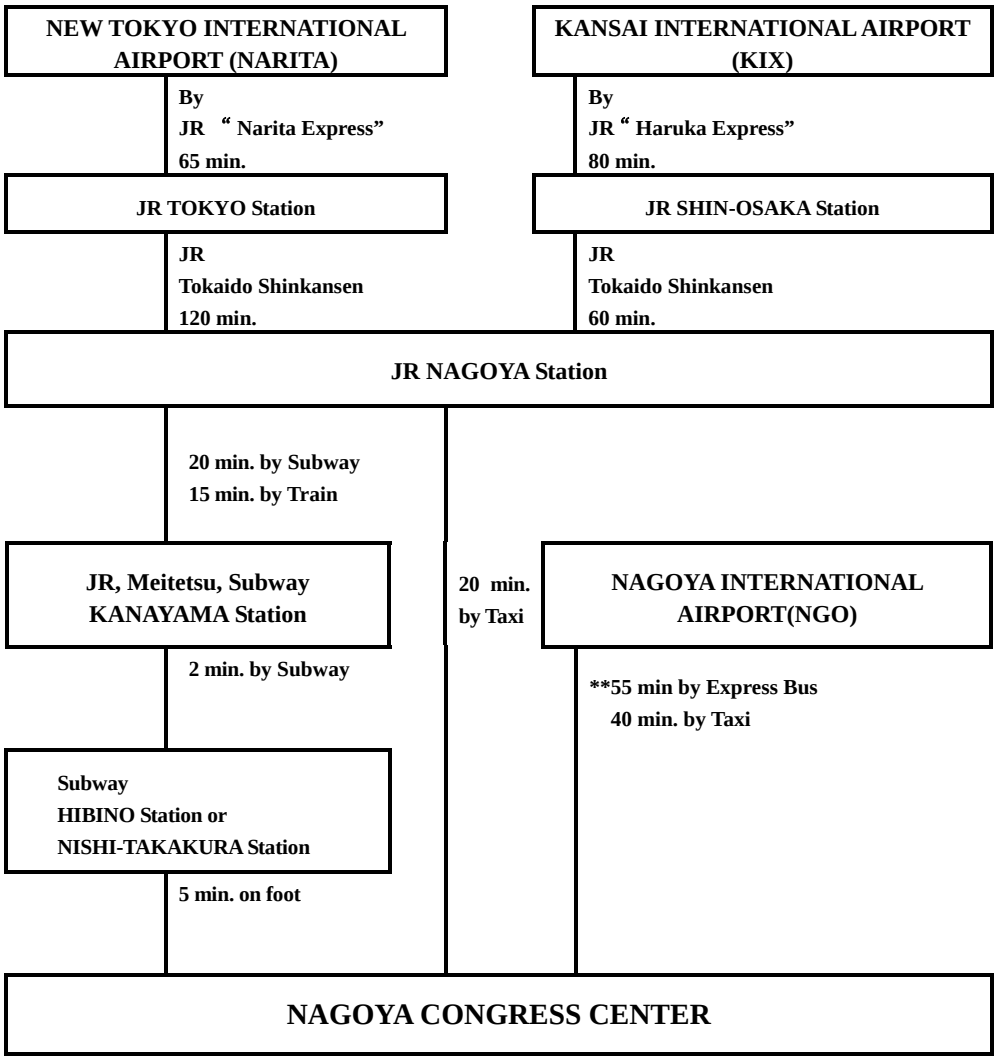
Authors are requested to prepare their poster materials during:

13:00 to 16:00 of September 18.

Please take down their poster materials by:

19:15 on September 18.

ACCESS TO NAGOYA CONGRESS CENTER



***Transportation to Nagoya Congress Center from Nagoya Station**

◆ **Subway**

Take HIGASHIYAMA Line at the Nagoya Station and transfer at SAKAE Station to the MEIJO Line. Take the train for NAGOYA-KO and get off at HIBINO or take the train for ARATAMABASHI and get off at NISHI - TAKAKURA, and on foot about 5min.

◆ **Train**

Take Tokai-Do Line at the Nagoya Station and get off at JR or MEITETSU KANAYAMA Station, transfer to the subway. Take the train for NAGOYA-KO and get off at HIBINO or take the train for ARATAMABASHI and get off at NISHI - TAKAKURA, and on foot about 5min.

****Transportation to Nagoya Congress Center from Nagoya International Airport**

◆ **Express Bus**

It is about 55 minutes in Express Bus on a regular route from the Nagoya airport to the Conference Site.

◆**Limousine Bus**

There is a limousine from the Nagoya airport to ANA Hotels Hotel Grand Court Nagoya (On foot-from Kanayama Station 1 minute). Please access to SSDM Home Page for details.

ACCESS TO BANQUET PLACE (ANA Hotels Hotel Grand Court Nagoya)

別紙A

SCOPE OF CONFERENCE

CORE AREAS

① Advanced Silicon Circuits and Systems	(Chair, T. Kuroda, Keio Univ.)
② Advanced Silicon Devices and Device Physics	(Chair, T. Mogami, NEC)
③ Silicon Process / Materials Technologies	(Chair, N. Kobayashi, Selete)
④ New Materials and Characterization	(Chair, S. Takagi, Toshiba)
⑤ Compound Semiconductor Materials and Devices	(Chair, N. Kobayashi, NTT)
⑥ Optoelectronic Devices and Photonic Crystal Devices	(Chair, O. Wada, Kobe Univ.)
⑦ Novel Devices, Physics & Fabrication	(Chair, K. Ishibashi, Riken)
⑧ Quantum Nanostructures Devices and Physics	(Chair, Y. Arakawa, Univ. of Tokyo)

STRATEGIC AREAS

⑨ Silicon-on-Insulator Technologies	(Chair, T. Nishimura, Mitsubishi Electric)
⑩ Non-Volatile Memory Technologies	(Chair, K. Takasaki, Fujitsu Lab.)
⑪ SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communication	(Chair,T. Enoki , NTT)
⑫ System-Level Integration and Packaging Technologies	(Chair, M. Koyanagi, Tohoku Univ.)
⑬ Organic Semiconductor Devices and Materials	(Chair, Y. Ohmori, Osaka Univ.)
⑭ Micro-Nano Electromechanical/Bio Conjugated Systems	(Chair, Y. Horiike, Univ. of Tokyo)

RUMP SESSION

Following two rump sessions are planned to be held on September 18 (Wednesday). The detail of the rump sessions will be announced in the Advance Program.

"Ultimate Device Scaling versus New System Integration: Compete or Cooperate?

"Toward 100Gbps/THz Era"

別紙B

in cooperation with

IEEE EDS Japan Chapter

IEEE EDS Kansai Chapter

IEEE Japan Council

The Electrochemical Society of Japan

The Institute of Electrical Engineers of Japan

The Institute of Electronics, Information and Communication Engineers

The Institute of Image Information and Television Engineers

別紙C

ORGANIZING COMMITTEE

■Chair

Y. Yasuda (Nagoya Univ.)

■Vice Chair

M. Nakamura (Hitachi)

STEERING COMMITTEE

■Chair

S. Zaima (Nagoya Univ.)

■Vice Chair

S. Kawamura (AIST)

PROGRAM COMMITTEE

■Chair

Y. Aoyagi (Tokyo Inst. of Technol.)

■Vice Chairs

T. Enoki (NTT)

M. Koyanagi (Tohoku Univ.)

Tuesday, September 17

Shiratori Hall

PL: Opening Session (9:30 - 12:30)
Chairpersons: S. Zaima Univ. of Tokyo and Y. Aoyagi, Tokyo Inst. of Technol..

9:30 PL-0
Welcome Address and Award Presentation,
Y. Yasuda, Nagoya Univ., Organizing Committee Chairperson

9:45 PL-1 (Plenary)
Start-Up Companies, University-Industry Relations, and Emerging High Tech Markets: Implementing the New Innovation Systems of the 21st Century
R.B. Dasher, *Stanford Univ., USA*

10:30 PL-2 (Plenary)
Message from the Desk of Automotive Electronics
H. Ono, *Toyota Motor, Japan*

11:15 PL-3 (Plenary)
Ionic-Electronic Hybrids: Ion Channels, Nerve Cells and Brains on Semiconductor Chips
P. Fromherz, *Max Planck, Germany*

12:00-13:30 Lunch

Room A

A-1: Advanced Silicon Devices and Device Physics
- Strained Silicon Devices-Chair: S.Inaba (Toshiba)
N.Sugii (Hitachi)

13:30 A-1-1
Strained Si- and SiGe-On-Insulator (Strained SOI and SGOI) MOSFETs as New Device Options for High Performance CMOS
S. Takagi, *MIRAI-ASET, Japan*

14:00 A-1-2 # 279
Enhanced Performance from SiGe pMOSFETs Fabricated on Novel SiGe Virtual Substrates Grown on 10 μm x 10 μm Si Pillars
A.M. Waite, U.N. Straube, N.S. Lloyd, S.G. Croucher, Y.T. Tang, B. Rong, A.G.R. Evans, T.J. Grasby*, M. Myronov*, T.E. Whall*, E.H.C. Parker*, D.J. Norris** and A.G. Cullis**, *Univ. of Southampton, *Univ. of Warwick and **Univ. of Sheffield, UK*

14:20 A-1-3 # 57
Novel Strained-Si Substrate Technology for Transistor Performance Enhancement
C.-C. Lin, C.-H. Wang, C.-H. Ge, C.-C. Huang, T.-C. Chang, L.-G. Yao, S.-C. Chen. M.-S. Liang, F.-L. Yang, Y.-C. Yeo and C. Hu, *TSMC, Taiwan*

Room B

B-1: Silicon Process/Materials Technologies
- High k Dielectrics I -
Chair: M.Niwa (Matsushita)
N.Hiratani (Hitachi)

13:30 B-1-1 # 5006
Critical Materials Issues for High-k Gate Dielectric Integration
R.M. Wallace, *North Texas Univ., USA*

14:00 B-1-2 # 329
Effects of Oxynitride-Based Interface Control on HfO_2 MIS Properties and FET Performance
H. Ota, N. Yasuda*, T. Yasuda, Y. Morita, N. Miyata, K. Tominaga*, M. Kadoshima*, S. Migita, T. Nabatame* and A. Toriumi, *AIST and *ASET, Japan*

14:20 B-1-3 # 20
Impact of Hf Metal Pre-Deposition in CVD- and PVD-HfO_2 Dielectrics
K. Yamamoto, M. Asai*, S. Hayashi, S. Horii*, M. Niwa and H. Miya*, *Matsushita Electric and *Hitachi Kokusai Electric, Japan*

Room C

C-1: New Materials and Characterization
-Advanced Characterization-
Chair: A.Sakai (Nagoya Univ.)
M.Ichikawa (Univ. of Tokyo)

13:30 C-1-1 # 5050
Advanced Electron Microscopy Characterization of Semiconductor Surface and Interface Processes
R.M. Tromp, *IBM, USA*

14:00 C-1-2 # 118
A Novel TEM/AFM/STM Microscopy for Cu Nano-Wire Electromigration
S. Fujisawa, T. Kikkawa and T. Kizuka*, *AIST and *Univ. of Tsukuba, Japan*

14:20 C-1-3 # 41
Lattice Strain in Scaled Devices Revealed by Using Convergent-Beam Electron Diffraction
A. Toda, K. Okonogi*, N. Ikarashi and H. Ono, *NEC and *Elpida Memory, Japan*

Room D

D-1: Silicon-on-Insulator Technologies
- Main Stream CMOS or SOI -
Chair: T.Nishimura (Mitsubishi)
A.Adan (Sharp)

13:30 D-1-1 # 5028
Advanced Fully-Depleted SOI CMOS Transistors
R. Chau, *Intel, USA*

14:00 D-1-2 # 5029
High Performance SOI Technology for Advanced Microprocessors
M.M. Pelella, *AMD, USA*

14:30 D-1-3 # 166
Non-Monotonous Transition of SOI History Effect from FD to PD Modes
H. Nakayama, H. Komatsu, S. Shimizu, T. Ohno and K. Takeshita, *Sony, Japan*

Room E

Room F

F-1: Novel Devices, Physics and Fabrication
- Carbon Nanotubes & Molecular Based Devices-
Chair: T.Homma (NTT)
Y. Kuwahara (Osaka Univ.)

13:30 F-1-1 # 5022
Controlling and Measuring Molecular-Scale Properties for Molecular Electronic
P. Weiss, *Pennsylvania State Univ., USA*

14:00 F-1-2 # 216
Electronic Transport Properties of C_{60}, C_{90} and Gd@C_{82} Fullerene-Carbon Nanotube Peapods
T. Shimada. T. Okazaki, Y. Ohno, K. Suenaga*, S. Iwatsuki, S. Kishimoto, T. Mizutani, R. Taniguchi, T. Inoue, T. Sugai and H. Shinohara, *Nagoya Univ. and *AIST, Japan*

14:15 F-1-3 # 334
Single Electron Transistor with Ultra-High Coulomb Energy of 5000K Using Position Controlled Grown Carbon Nanotube as Channel
K. Matsumoto, S. Kinoshita, K. Kurachi, Y. Gotoh and Y. Awano*, *AIST and * Fujitsu Labs., Japan*

Room G

G-1: Compound Semiconductor Materials and Devices
- III-V Epitaxial Technology & Electron Device -
Chair: K.Kojima (Mitsubishi)

13:30 G-1-1 # 5014
Mass Production Technology of MOVPE for InP, GaN and Progressed GaAs Related Materials
Y. Otoki, *Hitachi Cable, Japan*

14:00 G-1-2 # 5016
Epitaxial Manufacturing Outlook for Microwave Industry
S.Y. Chen, N. Hayafuji, J.-S. Wu, J.-T. Lai and C.C.K. Pong, *Procomp Informatics, Taiwan*

14:30 G-1-3 # 36
InP-Based HEMTs with a Very Short Gate-Channel Distance
A. Endoh, Y. Yamashita, K. Shinohara*, K. Hikosaka, T. Matsui*, S. Hiyamizu** and T. Mimura, *Fujitsu Labs., *Communications Research Lab. and **Osaka Univ., Japan*

Room A	Room B	Room C	Room D	Room E	Room F	Room G
14:40 A-1-4 # 76 Evaluation of Change in Drain Current due to Strain in 0.13- μ m-Node MOSFETs Y. Kumagai, H. Ohta, H. Miura, F. Ito, K. Maekawa and A. Shimizu*, *Hitachi and *Hitachi ULSI Systems, Japan*	**14:40 B-1-4 # 293** A Theoretical Study of SiO_2-Rich Zr and Hf Silicates as High-k Gate Insulators T. Hamada, T. Maruizumi, Y. Matsui and M. Hiratani, *Hitachi, Japan*	**14:40 C-1-4 # 304** Characterization of Si Surface Stress in Various Dielectric Thin Film/Si Structure by Photoflectance Spectroscopy M. Sohgawa, H. Kanda, T. Kanashima, A. Fujimoto* and M. Okuyama, *Osaka Univ. and *Wakayama National College of Technol., Japan*	**14:50 D-1-4 # 110** Elevated Source/Drain Engineering with 0.22-nm-Rms Smooth Surface Morphology for 90-nm-Node Ultrathin-SOI CMOS K. Sugihara, T. Nakahata, T. Matsumoto, S. Maeda, S. Maegawa, K. Ota, H. Sayama, H. Oda, T. Eimori, Y. Abe, T. Ozeki, Y. Inoue and T. Nishimura, *Mitsubishi Electric, Japan*		**14:30 F-1-4 # 416** Bonding Process for Nano-Scale Wiring Using Carbon Nano-Tube by Scanning Tunneling Microscope Tip N. Aoki, J. Takayama, M. Kida, K. Horiuchi*, S. Yamada**, T. Ida***, K. Ishibashi*** and Y. Ochiai, *Chiba Univ., *Fuji -Xerox, **JAIST and ***RIKEN, Japan*	**14:45 G-1-4 # 138** Comparison of Electrical Characteristics of Metamorphic HEMTs with InP HEMTs and PHEMTs K. Kawada, Y. Ohno, S. Kishimoto, K. Maezawa, T. Mizutani, M. Takakusaki* and H. Nakata*, *Nagoya Univ. and *Nikko Materials, Japan*
15:00 A-1-5 # 142 Multi-Subband Effects on the Performance Limit of Nanoscale MOSFETs K. Natori, T. Shimizu and T. Ikenobe, *Univ. of Tsukuba, Japan*	**15:00 B-1-5 # 209** Study on Densification and Oxidation Mechanism during PDA for Minimum EOT of Ultrathin CVD HfO_2 Y. Harada, M. Niwa and D.-L. Kwong*, *Matsushita Electric, Japan and Univ. of Texas at Austin, USA*	**15:00 C-1-5 # 152** Microscopic Identification of Implantation Damage Centers in Si ULSIs T. Umeda and Y. Mochizuki, *NEC, Japan*	**15:10 D-1-5 # 418** Notable Advantages of High Performance SOI Technology beyond 90nm Generation H.-S. Kang, C.-B. Oh, Y.-W. Kim, K.-S. Kim and K.-P. Suh, *Samsung Electronics, Korea*		**14:45 F-1-5 # 420** Electron Field Emission with Carbon Nanotube on a Si Tip P.N. Minh, L.T.T. Tuyen, T. Ono, H. Mimura and M. Esashi, *Tohoku Univ., Japan*	15:00 G-1-5 # 265 Doping Design and Two-Dimensional Electron Gas Density in AlGaN/GaN Heterostructure Field-Effect Transistors for High-Power Applications N. Maeda, K. Tsubaki, T. Saitoh and N. Kobayashi, *NTT, Japan*
					15:00 F-1-6 # 69 Electrical Conduction Through Poly(dG) Single-Stranded, Poly(dC) Single-Stranded, and Poly(dG)-Poly(dC) Double-Stranded DNA Molecules J.S. Hwang, G.S. Lee*, K.J. Kong, D.J. Ahn*, S.W. Hwang* and D. Ahn, *Univ. of Seoul and *Korea Univ., Korea*	**15:15 G-1-6 # 428** A Study on Bias Dependence of IMD Asymmetry in HBT Using Nonlinear Large-Signal Model H.-M. Park and S. Hong, *KAIST, Korea*
15:20-15:45 Break	15:20-15:45 Break	15:20-15:45 Break	15:30-15:45 Break		15:30-15:45 Break	15:30-15:45 Break
A-2: Advanced Silicon Devices and Device Physics -Statistical Modeling and RF Simulation- Chair: M.Ogawa (Kobe Univ.) A.Hiroki (Kyoto Inst. Tech.)	**B-2: Silicon Process/Materials Technologies**	**C-2: New Materials and Characterization**	**D-2: Silicon-on-Insulator Technologies**		**F-2: Novel Devices, Physics and Fabrication**	**G-2: Compound Semiconductor Materials and Devices**
15:45 A-2-1 # 5003 Simulation of Intrinsic Fluctuations in Decanano MOSFETs: Present Status and Future Challenges A. Asenov, *Univ. of Glasgow, UK*	**15:45 B-2-1 # 5007** Adhesion and Reliability in Thin-Film Structures Containing Cu and Low-k Materials: Experiments and Multi-Scale Simulations R.H. Dauskardt, *Stanford Univ., USA*	**15:45 C-2-1 # 5008** High-Resolution Compositional Profiling of High-k Gate Stack Structures. E. Garfunkel, *Rutgers Univ., USA*	**15:45 D-2-1 # 5032** A High Performance 1T1J MRAM Technology with an Amorphous MTJ Material M. Motoyoshi, K. Moriyama*, H. Moli*, C. Fukumoto*, H. Itoh*, H. Kano, K. Bessho and H. Narisawa, *Sony and *Sony Semiconductor Kyushu, Japan*		**15:45 F-2-1 # 5046** Single Quantum Dot Photodiodes: Coherent Properties of a Two-Level System with Electric Contacts A. Zrenner, E. Beham, S. Stufler, F. Findeis, M. Bichler and G. Abstreiter, *Univ. Paderborn, Germany*	**15:45 G-2-1 # 5015** Progress on GaInNAs Long Wavelength Lasers T. Miyamoto and F. Koyama, *Tokyo Inst. of Technol., Japan*
16:15 A-2-2 # 325 Modeling and Analysis of Gate Line Edge Roughness Effect on CMOS Scaling Towards Deep Nanoscale Gate Length S.-D. Kim, S. Hong, J.-K. Park	**16:15 B-2-2 # 103** Structure Control of Periodic Porous Silica Film for Low-k Application K. Yamada, Y. Oku, N. Hata*, S. Takada* and T. Kikkawa*, *ASET and *AIST, Japan*	**16:15 C-2-2 # 149** Ultrathin Zr Silicate Gate Dielectrics with Compositional Gradation H. Watanabe, *NEC. Japan*	**16:15 D-2-2 # 5033** A 0.25um 1MB to 32MB FeRAM Module Family T. Ho, *IOTA Technol., USA*		**16:15 F-2-2 # 79** Impedance Analysis of a Radio-Frequency Single Electron Transistor H.D. Cheong, T. Fujisawa, T. Hayashi, Y.H. Jeong* and Y. Hirayama, *NTT, Japan and*	**16:15 G-2-2 # 5013** Metal-Semiconductor Hybrid Granular Films Designed for High-Sensitive Magnetic Field Sensors H. Akinaga, *AIST, Japan*

and J.C.S. Woo, *Univ. of California, Los Angeles, USA*

16:35 A-2-3 # 22
Statistical Modeling of MOS Devices for Parametric Yield Prediction
J.J. Liou, Q. Zhang, J. McMacken*, J.R. Thomson*, K. Stiles* and P. Layman*, *Univ. of Central Florida and *Agere Systems, USA*

16:35 B-2-3 # 197
Effect of TEOS Treatment on the Properties of Periodic Nanoporous Silica Low-k Film
Y. Oku, K. Yamada, N. Nishiyama*, S. Tanaka*, K. Ueyama*, N. Hata** and T. Kikkawa**, *ASET, *Osaka Univ. and ** AIST, Japan*

16:35 C-2-3 # 98
Water Absorption into ALD-Al_2O_3 Films as Revealed by Physical Analysis and Electrical Characterization
M. Kadoshima, M. Nishizawa*, T. Yasuda*, T. Nabatame and A. Toriumi*, *ASET and *AIST, Japan*

16:45 D-2-3 # 92
Highly Stable Etch Stopper Technology for 0.25 μm 1T1C 32Mb FRAM
N.W. Jang, Y.J. Song, S.H. Joo, K.M. Lee, H.H. Kim, H.J. Joo, J.H. Park, S.W. Lee, S.Y. Lee and K. Kim, *Samsung Electronics, Korea*

**Pohang Univ. of Science and Technol., Korea*

16:30 F-2-3 # 192
Tunneling Mode Dependence of Current-Voltage Characteristics in Si/SiO_2 Resonant Tunneling Diodes
M. Iwasaki, Y. Ishikawa, H. Ikeda and M. Tabe, *Shizuoka Univ., Japan*

16:45 G-2-3 # 306
Room-Temperature 1.54 μm Light Emission from Er, O-Codoped GaAs/GaInP LEDs Grown by Low-Pressure Organometallic Vapor Phase Epitaxy
A. Koizumi, K. Inoue, Y. Fujiwara, T. Yoshikane, A. Urakami and Y. Takeda, *Nagoya Univ., Japan*

16:55 A-2-4 # 129
Modeling and Simple Simulation Method of Stacked Spiral Inductors
H. Shima, T. Matsuoka and K. Taniguchi, *Osaka Univ., Japan*

16:55 B-2-4 # 318
Low-Cost Cu Interconnects Using Direct Patterning Process (DPP) of Photo-Sensitive MSZ with Low-k, Bottom Anti-Reflective Layer
M. Tada, T. Ogura and Y. Hayashi, *NEC, Japan*

16:55 C-2-4 # 99
Comparison Studies on Oxygen Diffusion Coefficients for ALD-Al_3O_3 and PLD-HfO_2 Films Using ^{18}O Isotope
T. Nabatame, T. Yasuda*, M. Nishizawa*, M. Ikeda, T. Horikawa and A. Toriumi*, *ASET and *AIST, Japan*

17:05 D-2-4 # 360
New Multi Layer Top Electrode of SRO/IrOx for 0.35 μm FRAM
Y. Horii, J.S. Cross*, N. Sato, S. Ozawa, K. Matsuura, M. Fujiki, T. Saito, S. Mihara, T. Eshita, S. Sun**, F. Chu**, G. Fox**, R. Baily**, T. Davenport ** and T. Yamazaki, *Fujitsu, *Fujitsu Labs., Japan and **Ramtron International, USA*

16:45 F-2-4 # 100
Programmable Conductivity of Silicon Nanowires with Side Gates by Surface Charging
T. Matsukawa, S. Kanemaru, M. Masahara, M. Nagao, H. Tanoue and J. Itoh, *AIST, Japan*

17:00 G-2-4 # 178
Self-Assembly of Thin Disk-Shaped GaAs Blocks on Si Substrates
I. Soga, Y. Ohno, S. Kishimoto, K. Maezawa and T. Mizutani, *Nagoya Univ., Japan*

17:15 A-2-5 # 349
Analysis of Non-Quasistatic Contribution to Small-Signal Response for Deep Sub- μm MOSFET Technologies
S. Jinbou, H. Ueno, H. Kawano, K. Morikawa, N. Nakayama, M. Miura-Mattausch and H.J. Mattausch, *Hiroshima Univ., Japan*

17:15 B-2-5 # 430
Influence of Surface Oxide of Sputtered TaN Film on Displacement Plating of Cu
Z. Wang, H. Sakaue, S. Shingubara and T. Takahagi, *Hiroshima Univ., Japan*

17:15 C-2-5 # 332
New Method for Characterizing Dielectric Properties of High-k Films Using Time-Dependent Open-Circuit Potential Measurement
K. Kita, M. Sasagawa, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

17:25 D-2-5 # 371
Orientation Control of $(Bi,La)_4Ti_3O_{12}$ Films by Addition of Various Silicates and Germanates
Y. Kawashima, T. Kijima* and H. Ishiwara, *Tokyo Inst. of Technol. and *Seiko Epson, Japan*

17:00 F-2-5 # 333
Tunneling Barrier Structure in Room-Temperature Operating Silicon Single-Electron and Single-Hole Transistors
M. Saitoh, H. Majima and H. Hiramoto, *Univ. of Tokyo, Japan*

17:15 G-2-5 # 361
Control of Order Parameter during Growth of $In_{0.5}Ga_{0.5}P/GaAs$ Heterostructures by GSMBE Using Tertiarybutylphosphine (TBP)
T. Kakumu, F. Ishikawa, S. Kasai, T. Hashizume and H. Hasegawa, *Hokkaido Univ., Japan*

17:15 F-2-6 # 125
Threshold Voltage of Si Single-Electron Transistor
A. Fujiwara, S. Horiguchi, M. Nagase and Y. Takahashi, *NTT, Japan*

17:30 G-2-6 # 339
Fabrication of Sub-Micron Y-Gate InP MESFETs Using Crystallographically Defined Contact Technology
M. Yoon and K. Yang, *KAIST, Korea*

Wednesday, September 18

Room A	Room B	Room C	Room D	Room E	Room F	Room G
9:00 A-3-1 # 5005 Ultra-Thin Silicon Channel Single- and Double-Gate MOSFETs M. Ieong, *IBM, USA*	**9:00 B-3-1 # 5049** Integrated High-k and Metal Gate Processing Using RTP and ALCVDTM C. Werkhoven, H. de Waard, C. Pomarede, E. Shero, M. Givens, S. Haukka, M. Tuominen and J. W. Maes, *ASM America, USA*	**9:00 C-3-1 # 5044** High Performance Organic Non-Volatile Memory Device - a Direct Challenge to the Si Technology L.P. Ma, S. Pyo, J. Liu and Y. Yang, *UCLA, USA*	**9:00 D-3-1 # 5002** Digital Pixel Image Sensors A.E. Gamal, *Stanford Univ., USA*	**9:15 E-1-1 # 5036** InP HBT Device and Design Technologies for Ultrahigh Speed Electronics M. Rodwell, *UCSB, USA*	**9:30 F-3-1 # 5042** Chip-on-Chip Technology for High Performance Mobile Systems A. Matsuzawa, *Matsushita Electric, Japan*	**9:00 G-3-1 # 5017** Single Transverse Mode Operation of 1.55-mm Buried Heterostructure VCSELs Y. Ohiso, H. Okamoto, R. Iga, K. Kishi and C. Amano, *NTT, Japan*
9:30 A-3-2 # 300 Corrugated-Channel Transistor (CCT) for Area-Conscious	**9:30 B-3-2 # 17** Suppression of Silicidation in ZrO_2/SiOx/Si Structure by Helium Annealing	**9:30 C-3-2 # 387** Organic Thin-Film Transistors for Driving Organic Light Emitting	**9:30 D-3-2 # 90** A New Sampling Scheme for High Sensitive, Extended Dynamic Range	**9:45 E-1-2 # 7** InP Double-Heterojunction Bipolar Transistors with a Carbon-Doped Graded Base	**10:00 F-3-2 # 425** On-Chip Variable Inductor Using MEMS Technology Y. Yokoyama, T. Fukushige,	**9:30 G-3-2 # 5018** High Performance Wavelength Tunable DBR Lasers for DWDM Network

Applications
T. Furukawa, H. Yamashita and H. Sunami, *Hiroshima Univ., Japan*

K. Muraoka, *Toshiba, Japan*

Diode
M. Kitamura, T. Imada and Y. Arakawa, *Univ. of Tokyo, Japan*

CMOS Imaging Pixel Sensors
S.-R. Li and Y.C. King, *National Tsing-Hua Univ., Taiwan*

K. Kurishima, M. Ida and N. Watanabe, *NTT, Japan*

S. Hata, K. Masu and A. Shimokohbe, *Tokyo Inst. of Technol., Japan*

Applications
D.J. Robbins, *Bookham Technologies, UK*

9:50 A-3-3 # 322
Reduction of Gate -Induced Drain Leakage (GIDL) Current in Single-Gate Ultra-Thin Body and Double-Gate FinFET Devices
Y.-K. Choi, D. Ha, T.-J. King and J. Bokor, *Univ. of California at Berkeley, USA*

9:50 B-3-3 # 48
Improvement of Electrical Properties for High-k Dielectrics Grown by MOCVD via Cyclic Remote Plasma Oxidation
S. Horii, M. Asai, H. Miya, K. Yamamoto* and M. Niwa*, *Hitachi Kokusai Electric and *Matsushita Electric, Japan*

9:45 C-3-3 # 331
Performance and Time-Dependent Degradation in a Single Grain-Size Pentacene TFTs
T. Komoda, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

9:50 D-3-3 # 250
Simple-Architecture Motion-Detection Analog VLSI Based on Quasi-Two-Dimensional Processing
H. Kimura and T. Shibata, *Univ. of Tokyo, Japan*

10:00 E-1-3 # 120
The Effect of Emitter Size Scaling on f_{max} in InP/InGaAs HBTs
Y. Ikenaga, A. Fujihara and S. Tanaka, *NEC, Japan*

10:15 F-3-3 # 132
Behavior of Plated Micro-Bumps during Ultrasonic Flip-Chip Bonding Determined from Dynamic Strain Measurement
N. Watanabe and T. Asano, *Kyushu Inst. of Technol., Japan*

10:00 G-3-3 # 156
1.3 μ m GaInNAsSb Lasers with Low Threshold Current Density
C. Setiagung, H. Shimizu, K. Kumada and A. Kasukawa, *Furukawa Electric, Japan*

10:10 A-3-4 # 25
An Electrostatic-Discharge(ESD) Protection Device with Low Parasitic Capacitance Utilizing a Depletion-Layer-Extended Transistor (DET) for RF-CMOS IC's
T. Ohnakado, S. Yamakawa, A. Furukawa, K. Nishikawa, T. Murakami, Y. Hashizume, K. Sugahara, N. Suematsu and Oomori, *Mitsubishi Electric, Japan*

10:10 B-3-4 # 172
Materials and Electrical Characterization of Metal Gate Electrodes on Hig-k Dielectrics for Advanced CMOS Technologies
J.C. Hooker, R.J.P. Lander, Z.M. Rittersma, T. Schram*, G.S. Lujan*, J. van Zijl**, E. van den Heuvel** and F. Roozeboom**, *Philips Research Leuven, *IMEC, Belgium and **Philips Research Labs., The Netherlands*

10:00 C-3-4 # 395
Mechanism of Low-Voltage Operation in the Organic FET with the Top-and-Bottom Contact (TBC) Structure
M. Yoshida, S. Uemura, S. Hoshino, T. Kodzasa and T. Kamata, *AIST, Japan*

10:10 D-3-4 # 352
Low-Complexity, Highly-Parallel Color Motion-Picture Segmentation Architecture for Compact Digital CMOS Implementation
T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, *Hiroshima Univ., Japan*

10:15 E-1-4 # 242
Evaluation of Base-Collector Capacitance in Submicron Buried Metal Heterojunction Bipolar Transistors
Y. Miyamoto, T. Arai, S. Yamagami, K. Matsuda and K. Furuya, *Tokyo Inst. of Technol., Japan*

10:15 G-3-4 # 14
Thermal Rollover around 460-mW Observation in Single-Lateral Mode 780-nm Laser Diodes with Window-Mirror Structure
T. Yagi, Y. Tashiro, Y. Ohkura, S. Abe, H. Nishiguchi and Y. Mitsui, *Mitsubishi Electric., Japan*

10:15 C-3-5 # 239
Modification of Surface States of Gate Insulator for the Enhanced Performance of Pentacene TFT
C.K. Song, M.W. Lee, K.H. Kim, Y.X. Xu and S.B. Lee, *Dong-A Univ., Korea*

10:30 E-1-5 # 193
High Speed and Uniform Self-Aligned InGaAs/InP HBTs for 40 Gb/s Fiber Optic Communications Applications
K. Kotani, R. Yamabi, T. Kawasaki, M. Yanagisawa, S. Yaegassi and H. Yano, *Sumitomo Electric, Japan*

10:30-10:45 Break

10:30-10:45 Break

10:30-10:45 Break

10:30-10:45 Break

10:15-11:00 Break

10:30-15:45 Break

10:30-10:45 Break

10:45 A-4-1 # 5009
MOSFET Channel Engineering Using Strained Si, SiGe, and Ge Channels
E.A. Fitzgerald, *MIT, USA*

10:45 B-4-1 # 384
Etching of Organic Low k Dielectric, Their Gas Phase and Subsurface Reactions in Ultra High Frequency Plasma
H. Nagai, M. Hiramatsu*, M. Hori and T. Goto, *Nagoya Univ. and *Meijo Univ., Japan*

10:45 C-4-1 # 382
Fabrication of TTF-TCNQ Molecular Wires Using Applied Electric Field Deposition
M. Iizuka, M. Sakai, M. Nakamura and K. Kudo, *Chiba Univ., Japan*

10:45 D-4-1 # 244
Design of a Tiny Microprocessor Based on the Single-Flux-Quantum Circuit Technology
N. Yoshikawa, F. Matsuzaki, N. Nakajima, K. Fujiwara, K. Yoda and K. Kawasaki, *Yokohama National Univ., Japan*

11:00 E-2-1 # 5038
GaAs on Si Technology and Its Application to PA Amplifier
T. Hierl, *IQE, USA*

10:45 F-4-1 # 5043
High Performance, Low Power Three-Dimensional Integrated Circuits for Next Generation Technologies
L. McIlrath, *R3 Logic, USA*

10:45 G-4-1 # 5021
Ultrafast SOA-Based SMZ-Type All-Optical Regenerators and Wavelength Converters
Y. Ueno, S. Nakamura* and K. Tajima*, *Univ. of Electro-Commun. and *NEC, Japan*

11:15 A-4-2 # 368
Experimental Evidence of Low Dislocation Density of SiGe-on-Insulator Substrates Fabricated by Oxidizing SiGe/SOI Structures
N. Sugiyama, Y. Moriyama, T. Tezuka, T. Mizuno, S. Nakaharai, K. Usuda and T. Takagi, *ASET, Japan*

11:05 B-4-2 # 422
Stress -Induced Migration and Microstructural Features in Cu Metallization
J. Koike, A. Sekiguchi, M. Wada, R. Kainuma, K. Ishida and K. Maruyama, *Tohoku Univ., Japan*

11:00 C-4-2 # 243
Molecular Enamel Wires for Electronic Device: Theoretical Study
R.V. Belosludov, H. Sato, A.A. Farajian, H. Mizuseki and Y. Kawazoe, *Tohoku Univ., Japan*

11:05 D-4-2 # 101
High-Speed Operation of a Single-Flux-Quantum (SFQ) Cross/Bar Switch up to 35 GHz
Y. Kameda, S. Yorozu, H. Terai* and A. Fumijaki**, *NEC, *CRL and **Nagoya Univ., Japan*

11:30 E-2-2 # 5039
Device Scaling and Prospect of GaN FET
Y. Ohno and J.-P. Ao, *Univ. of Tokushima, Japan*

11:15 F-4-2 # 5041
Genuine Technologies for Three-Dimensional Integration and Packaging
K. Okumura, *Univ. of Tokyo, Japan*

11:15 G-4-2 # 415
Correlation between Fe-ZN Inter-Diffusion Observed by Scanning Capacitance Microscopy and Device Characteristics of Electro-Absorption Modulators
M. Ogasawara, R. Iga, S. Kondo* and Y. Kondo, *NTT and *Niigata Univ., Japan*

11:35 A-4-3 # 188
Realization of Dislocation-Free Relaxed SiGe-on-Insulator Substrates by Mesa Isolation
T. Tezuka, N. Sugiyama and S. Takagi, *ASET, Japan*

11:25 B-4-3 # 317
Chemical Structural Control of Plasma-Polymerized, Divinylsiloxane Benzocyclobutene Films for Sub 100nm-Node ULSI Devices
Y. Harada, M. Tada, J. Kawahara and Y. Hayashi, *NEC, Japan*

11:15 C-4-3 # 50
Influence of Oxygen on Photocurrent Multiplication Phenomenon at Organic/Metal Interface
K. Suemori, M. Hiramoto and M. Yokoyama, *Osaka Univ., Japan*

11:25 D-4-3 # 196
A Fine-Grained Programmable Logic Module with Small Amount of Configuration Data for Dynamically Reconfigurable Field Programmable Gate Array (FPGA)
N. Miyamoto, K. Leo, K. Kotani and T. Ohmi, *Tohoku Univ., Japan*

12:00 E-2-3 # 294
Drain-Current Collapse in AlGaN/GaN HEMTs on Sapphire and Semi-Insulating SiC Substrates
S. Arulkumaran, T. Egawa, H. Ishikawa and T. Jimbo, *Nagoya Inst. of Technol., Japan*

11:45 F-4-3 # 408
Parallel Image Processing LSI Fabricated Using Three-Dimensional Integration Technology
D. Kawae, T. Nakamura, Y. Yamada, T. Morooka, Y. Igarashi, J.C. Shim, H. Kurino and M. Koyanagi, *Tohoku Univ., Japan*

11:30 G-4-3 # 307
40 GHz Pulse Generation by Passively Mode-Locked Semiconductor Laser with Distributed Bragg Reflector for Oscillating Mode Selection
T, Nishimura, Y. Nomura, K. Akiyama, N. Tomita and T. Isu, *Mitsubishi Electric, Japan*

11:55 A-4-4 # 15
Low-Temperature Electrical Characteristics of Strained-Si MOSFETs
N. Sugii and K. Washio, *Hitachi, Japan*

11:45 B-4-4 # 273
Implementation of Electrically Programmable Fuse (eFUSE) in CMOS Technologies Using Electromigration
S.S.K. Iyer, C. Kothandaraman*, N. Robson*, D. Shum* J.P. Rice and S.S. Iyer, *IBM and *Infineon Technols., USA*

11:30 C-4-4 # 83
Studies on Dark and Photoconductivity of MEH-PPV:C_{60} Thin Films
L. Damodare, T. Soga* and T. Mieno, *Shizuoka Univ. and *Nagoya Inst. of Technol., Japan*

11:45 D-4-4 # 198
Novel Random Number Generator Using MOS Gate after Soft-Breakdown
S. Yasuda, T. Tanamoto, H. Satake and S. Fujita, *Toshiba, Japan*

12:00 F-4-4 # 411
Thermal Analysis of Self-Heating Effect in Three Dimensional LSI
T. Nakamura, Y. Yamada, T. Morooka, Y. Igarashi, J.C. Shim, H. Kurino and M. Koyanagi, *Tohoku Univ., Japan*

11:45 G-4-4 # 263
Femtosecond Response of Diffraction Efficiency in GaAs/AlGaAs Photorefractive Multiple Quantum Well
H. Tanaka, K. Terawaki, K. Kou, S. Tsuboi, S. Nagahara, T. Kita, O. Wada, K. Nakagawa* and D.D. Nolte**, *Kobe Univ., *Kagawa Univ., Japan and **Purdue Univ., USA*

11:45 C-4-5 # 223
Fabrication of Porphyrin-Gold Nanoparticle Multistructures for Photoelectric Conversion
S. Yamada, T. Tasaki, S. Nitahara, N. Terasaki and T. Akiyama, *Kyushu Univ., Japan*

12:00 G-4-5 # 343
Broadband All-Optical Flip-Flop Using Integrated SOA/DFB-SOA
Y.-I. Kim, S. Lee, D.H. Woo and T.-H. Yoon*, *KIST and *Pusan National Univ, Korea*

12:00 C-4-6 # 261
Theoretical Study on Chlorin-Fullerene Supramolecular Complex for Photovoltaic Device
H. Mizuseki, N. Igarashi, R.V. Belosludov, A.A. Farajian and Y. Kawazoe, *Tohoku Univ., Japan*

13:15 A-5-1 # 5035
Nonvolatile Memory Challenges toward Gigabit and Nanoscaling Era
S. Pan, R. Liu and C.Y. Lu, *Macronix International, Taiwan*

13:15 B-5-1 # 173
Novel Binary Alloy Gate Electrodes for Metal Gate MOS Devices
C.-F. Huang and B.-Y. Tsui, *National Chiao Tung Univ., Taiwan*

13:30 C-5-1 # 5045
Ultrafast Molecular Photonics for All-Optical Data Processing
T. Nagamura, *Shizuoka Univ., Japan*

13:15 D-5-1 # 5001
Gigabit-Throughput CMOS ICs for Optical Interconnection Applications
H.-J. Yoo, *KAIST, Korea*

13:30 E-3-1 # 5037
SiGe BiCMOS Technologies for Communication Systems
M. Racanelli, *SpecialtySemi, USA*

13:15 F-5-1 # 5047
Microfabricated Nanotools for Detection and Manipulation down to the Molecular Level
U. Staufer, L. Aeschimann, T. Akiyama, S. Gautsch and N. F. de Rooij, *Univ. of Neuchatel, Switzerland*

13:15 G-5-1 # 5019
Photonic Crystals and Their Applications
S. Noda and T. Asano, *Kyoto Univ., Japan*

13:45 A-5-2 # 369
Enhanced Tunneling Current Effect for Nonvolatile Memory Applications
B. Govoreanu, P. Blomme, J. van Houdt and K.De Meyer, *IMEC, Belgium*

13:35 B-5-2 # 77
First-Principles Calculation of High Strain-Induced Leakage Current in Silicon Dioxide Used for Gate Dielectrics
H. Moriya, T. Iwasaki and H. Miura, *Hitachi, Japan*

14:00 C-5-2 # 187
Fabrication and Surface Plasmon Excitation Properties of Polystyrene Submicron Sphere Thin Films
K. Shinbo, S. Miyabayashi, K. Kato, F. Kaneko, T. Kawakami, M. Tanaka and R.C. Advincula*, *Niigata Univ., Japan and *Univ. of Alabama at Birmingham, USA*

13:45 D-5-2 # 351
Fully Parallel Nearest Manhattan-Distance-Search Memory with Large Reference-Pattern Number
Y. Yano, T. Koide and H.J. Mattausch, *Hiroshima Univ. Japan*

14:00 E-3-2 # 421
Suppression of B Outdiffusion by C Incorporation in Ultra-High-Speed SiGeC HBTs
K. Oda, I. Suzumura, M. Miura, E. Ohue, R. Hayama, A. Kodama*, H. Shimamoto* and K. Washio, *Hitachi and *Hitachi Device Eng., Japan*

13:45 F-5-2 # 146
STP Sealing Technique for Surface Micromachined MEMS Stacked on a CMOS LSI
N. Sato, H. Ishii, S. Shigematsu, H. Morimura, K. Kudou*, M. Yano* and K. Machida, *NTT and *NTT Advanced Technol., Japan*

13:45 G-5-2 # 5020
2D Semiconductor-Based Photonic Crystals for Nano-Integrated Optics
Y. Sugimoto and K. Asakawa, *FESTA, Japan*

14:05 A-5-3 # 335
Flash Memory Reliability: an Improvement against Erratic Erase Phenomena Using the Constant Charge Erasing Scheme
A. Chimenton and P. Olivo, *Univ. of Ferrara, Italy*

14:25 A-5-4 # 357
Low Voltage Low Current Flash Memory Using Source Induced Band-to-Band Tunneling Hot Electron Injection to Perform Programming
L. Pan, J. Zhu, K. Liu, J. Liu, Y. Zeng and L. Sun, *Tsinghua Univ., China*

14:45-15:00 Break

15:00 A-6-1 # 5034
Embedded MONOS Nonvolatile Semiconductor Memory Technology
S. Minami, *Hitachi, Japan*

15:30 A-6-2 # 71
A Novel Structure of SiO_2/SiN/High k Dielectrics, Al_2O_3 for SONOS Type Flash Memory
C. Lee, S. Hur, Y. Shin, J. Choi, D. Park and K. Kim, *Samsung Electronics, Korea*

15:50 A-6-3 # 89
Hot Carrier Enhanced Read Disturb and Scaling Effects in a Localized Trapping Storage SONOS Type Flash Memory Cell
W.J. Tsai, C.C. Yeh, N.K. Zous*, C.C. Liu, S.K. Cho, C.H. Chen, T. Wang*, S. Pan and C.-Y. Lu, *Macronix International and *National Chaio-Tung Univ., Taiwan*

16:10 A-6-4 # 367
Characterization of microFLASH® Memory Using "Dummy" GOX Structures

13:55 B-5-3 # 258
Negative-Bias-Temperature Instability in Ultra Thin Nitride/Oxide Stack Gate Dielectric
D.-Y. Lee, H.-C. Lin*, W.-J. Chiang, C.-C. Chen**, C.-Y. Lin**, T.-Y. Huang, T. Wang and M.S. Liang**, *National Chiao Tung Univ., *National Nano Device Labs. and *TSMC, Taiwan*

14:15 B-5-4 # 121
Low Temperature Oxidation of Si(100) with Ozone Radicals: Chemical Reaction Mechanism and Surface Stress
T. Narushima, A.N. Itakura*, M. Kitajima* and K. Miki, *AIST and *NIMS, Japan*

14:35-15:00 Break

15:00 B-6-1 # 18
Drastic Leakage Suppression by Through-Oxide Arsenic Pre-SALICIDE Implantation for $CoSi_2$ Formation on Shallow n+/p Junctions
M. Tsuchiaki, A. Murakoshi and C. Hongo, *Toshiba, Japan*

15:20 B-6-2 # 211
Influence of Ge and C for Reaction in Ni/p^+-$Si_{1-x-y}Ge_xC_y$/Si(100) Contacts
Y. Tsuchiya, O. Nakatsuka, A. Sakai, S. Zaima, J. Murota* and Y. Yasuda, *Nagoya Univ. and *Tohoku Univ., Japan*

15:40 B-6-3 # 113
A New Plasma Dry Cleaning Method Applied to Contact and Gate Pre Cleaning
K. Miyatani, K. Nishizawa, Y. Kobayashi and Y. Tada, *Tokyo Electron, Japan*

14:15 C-5-3 # 186
Emission Light and Multiple Surface Plasmon Excitations at Prism/Ag/Merocyanine LB Films
F. Kaneko, T. Sato, M. Terakado, T. Nakano, K. Shinbo, K. Kato, T. Wakamatsu* and R.C. Advincula**, *Niigata Univ., *Ibaraki National College of Technol., Japan and **Univ. of Alabama at Birmingham, USA*

14:30 C-5-4 # 308
Study of SHG from CuttbPc LB Film/Metal Interface
C.-Q. Li, T. Manaka, X.-M. Cheng and M. Iwamoto, *Tokyo Inst. of Technol., Japan*

14:45-15:00 Break

15:00 C-6-1 # 319
Fast Response of Organic Photo Detectors Utilizing Multi-Layered Metal-Phthalocyanine Thin Films
M. Kaneko, T. Taneda, T. Tsukagawa, H. Kajii and Y. Ohmori, *Osaka Univ., Japan*

15:15 C-6-2 # 185
Organic Light Emitting Diodes with a Nanostructured Fullerene Layer at the Interface between Aiq_3 and TPD Layers
K. Kato, K. Suzuki K. Shinbo, F. Kaneko, N. Tsuboi, S. Kobayashi, T. Todokoro* and S. Ohta*, *Niigata Univ. and * Nippon Seiki, Japan*

15:30 C-6-3 # 183
Organic Electroluminescent Diode Fabricated on ITO-Coated Polyimide Substrate as an Electro-Optical Conversion Device for Polymeric Waveguides
H. Kajii, T. Taneda, M. Kaneko and Y. Ohmori, *Osaka Univ., Japan*

15:45 C-6-4 # 49
Light Emitting Device of Organic-Inorganic Layered Perovskite Prepared by Dual-Source Vapor

14:05 D-5-3 # 254
Design and Implementation of Read-Compare-Write Circuits for Low Power Multi-Gigabit DRAM
S. Choi, Y.-H. Park and H.-J. Yoo, *KAIST, Korea*

14:25 D-5-4 # 414
Optimum Device Consideration for Standby Power Reduction Scheme Using Drain Induced Barrier Lowering (DIBL)
Q, Liu, T. Sakurai and T. Hiramoto, *Univ. of Tokyo, Japan*

14:45-15:00 Break

15:00 D-6-1 # 5023
Spin Polarized Electron Injection through Tunneling Junctions and Its Application for SP-STM
K. Sueoka, A. Subagyo and K. Mukasa, *Hokkaido Univ., Japan*

15:30 D-6-2 # 364
Structural Analysis of Bismuth Nanowire by X-Ray Standing Wave Method
A. Saito, K. Matoba, J. Maruyama, Y. Kuwahara and K. Miki*, *Osaka Univ. and *National Inst. of Materials Science, Japan*

15:45 D-6-3 # 305
Reproducible Current Switching in Copper Sulfide Films
T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa*, T. Nakayama* and M. Aono*, *NEC and *JST, Japan*

16:00 D-6-4 # 419
Aluminum Nanodot Array Formed by Anodic Oxidation and Its Conduction Properties

14:15 E-3-3 # 412
Sub 100 nm Gate Technologies for Si/SiGe Buried Channel RF Devices
M. Zeuner, T. Hackbarth, M. Enciso-Aguilar*, F. Aniel* and H. von Känel**, *Daimler Chrysler, Germany, *Paris-Sud Univ., France and **ETH-Zürich, Switzerland*

14:30 E-3-4 # 268
Influence of SiGe Channel Position and Fowler-Nordheim Stress on 1/f Noise in SiGe pMOSFETs
Y.-J. Song, S.-H. Kim, J.-H. Kim*, J.-I. Song* and K.-H. Shim, *ETRI and *KJST, Korea*

14:45-15:00 Break

15:00 E-4-1 # 5040
HEMT Technologies and Ics for over-40-Gbit/s Optical Communications Systems
Y. Nakasha, T. Suzuki, H. Kano, S. Yamaura, K. Makiyama, T. Takahashi, T. Hirose, and M. Takikawa, *Fujitsu Labs., Japan*

15:30 E-4-2 # 31
Data Limiting-Amplifier, Data Distributor, and Clock Distributor ICs for 40-Gbit/s-class Optical Communication Systems Using InP HEMTs
K. Sano, K. Murata, S. Sugitani, H. Sugahara and T. Enoki, *NTT, Japan*

15:45 E-4-3 # 147
Double-Recessed 0.1-μm-Gate InP HEMTs for 40-Gb/s Optical Communication Systems
S. Hoshi, H. Moriguchi, M. Itoh, T. Ohshima, I. Matsuyama, M. Tsunotani and T. Ichioka, *Oki Electric, Japan*

16:00 E-4-4 # 21
2.2 W/mm GaAs HFET with Field-Modulating Plate Operated at 32 V
K. Ota, A. Wakejima, K.

14:00 F-5-3 # 431
Electrostatically Levitated Ring-Shaped Rotational-Gyro/Accelerometer
T. Murakoshi, K. Fukatsu, Y. Endo, S. Nakamura and M. Esashi*, *TOKIMEC and *Tohoku Univ., Jpan*

14:15 F-5-4 # 280
Multichannel 5 x 5-site 3D Si Micro-Probe Electrode Array for Neural Activity Recording System
T, Kawano, H. Takao, K. Sawada and M. Ishida, *Toyohashi Univ, of Technol., Japan*

14:30-15:00 Break

15:00 F-6-1 # 5048
Therapeutic Applications of Biodegradable and Bioactive Forms of Silicon
L. Canham, *Univ. of Birmingham, UK*

15:30 F-6-2 # 426
γ-GTP Colorimetric Measurement on a Microcapillary Chip for Testing Liver
A. Oki, H. Ogawa and Y. Horiike, *Univ. of Tokyo, Japan*

15:45 F-6-3 # 437
SNP Detection Using Thermal Gradient DNA Chip
Y. Miyahara, T. Kajiyama, L.J. Kricka*, D.J. Graves*, S. Surrey** and P. Fortina***, *Hitachi High-Technols., Japan, *Univ. of Pennsylvania, **Thomas Jefferson Univ. and ***Children's Hospital of Philadelphia, USA*

16:00 F-6-4 # 435
Fast DNA Analysis by Novel Separation Media Based on Nanoparticles on a Microfabricated Chip

14:15 G-5-3 # 5
Surface Micromachining in Optical Isolator Employing Nonreciprocal Radiation Mode Conversion
H. Yokoi, T. Mizumoto, T. Sakai, H. Sano, T. Ohtsuka* and Y. Nakano*, *Tokyo Inst. of Technol. And *Univ. of Tokyo, Japan*

14:30 G-5-4 # 309
Formation of Small Size Polarization Domain Inversion for High-Efficient QPM-SHG Device - Proposal of Full Cover Electrode Method -
S. Nagano, M. Konishi, T. Shiomi and M. Minakata, *Shizuoka Univ., Japan*

14:45-15:00 Break

15:15 G-6-1 # 5010
Growth and Characterization of p-type ZnO Thin Films by MBE
D.B. Eason, G. Cantwell, D.C. Look*, D.C. Reynolds*, C.W. Litton** and R.L. Jones**, *Eagle-Picher Technologies, *Wright-State Univ. and **Air Force Research Lab., USA*

15:45 G-6-2 # 88
Effect of Chemical Doping with Ga and N on Electrical and Optical Properties of ZnO Thin Films
H. Matsui, H. Tabata and T. Kawai, *Osaka Univ., Japan*

16:00 G-6-3 # 12
Zinc Beam Flux Dependence of MBE-ZnO Growth
H. Kato, M. Sano, K. Miyamoto and T. Tao*, *Stanley Electric and *Tohoku Univ., Japan*

16:15 G-6-4 # 208
Impact of SiC Structural Crystal Defects on the Electrical Performance of Bipolar PN Junction Diode

Y. Roizin, M. Gutman, E. Aloni, V. Kairys and P. Zisman, *Tower Semiconductor, Israel*

Deposition
T. Matsushima, K. Fujita and T. Tsutsui, *Kyushu Univ., Japan*

S. Shingubara, Y. Murakami, K. Morimoto, W.G. Ri and T. Takahagi, *Hiroshima Univ., Japan*

Matsunaga and M. Kuzuhara, *NEC, Japan*

M. Tabuchi, N. Kaji, Y. Nagasaki*, K. Kataoka** and Y. Baba, *Univ. of Tokushima, *Science Univ. of Tokyo and **Univ. of Tokyo, Japan*

R.K, Malhan, H. Nakamura, S. Onda, D. Nakamura* and K. Hara, *Denso and * Toyota Central R&D Labs., Japan*

16:15 D-6-5 # 276
The Characteristics of Light Emission by Ballistic Electron Excitation in Nanocrystalline Silicon Device Formed on a p-Type Substrate
Y. Nakajima, H. Toyama, A. Kojima and N. Koshida, *Tokyo Univ. of Agriculture and Technol., Japan*

16:15 E-4-5 # 359
60-GHz Single-Chip Receiver 3-D MMIC Using Commercial GaAS pHEMT Technology
K. Nishikawa, B. Piernas*, T. Nakagawa, K. Araki and K. Cho, *NTT and *Fujitsu Compound Semiconductor, Japan*

Thursday, September 19

Room A

9:00 A-7-1 # 241
Modified Gate Re-Oxidation Technology for High Performance Embedded DRAM by Self-Adjusted Gate Bird's Beak
Y. Nishida, S. Ueno, T. Uchida, T. Terauchi, T. Tsunomura, M. Takeuchi, M. Shirahata, T. Eimori and Y. Inoue, *Mitsubishi Electric, Japan*

9:20 A-7-2 # 255
Improvement of Disturbance/Pause Retention Time by Redusing Edge Channel Effect of Cell in Gigabit Density DRAMs and Beyond
I.-G. Kim, N.-S. Kim, Y.-W. Kwon, S.-K. Choi, J.-S. Kwon, Y.-I. Chun, H.-S. Yang and J. Park, *Hynix Semiconductor, Korea*

9:40 A-7-3 # 295
Impact of Burn-In Stress on Reliability of High Density DRAMs
I.-G. Kim, J.-H. Chun, N.-S. Kim, Y.-W. Kwon, S.-K. Choi and J.-S. Park, *Hynix Semiconductor, Korea*

Room B

9:00 B-7-1 # 381
Electrical Characterization of Aluminum-Oxynitride Stacked Gate Dielectrics Prepared by a Layer-by-Layer Process of Chemical Vapor Deposition and Rapid Thermal Nitridation
H. Murakami, W. Mizubayashi, H. Yokoi, A. Suyama and S. Miyazaki, *Hiroshima Univ., Japan*

9:20 B-7-2 # 154
Characterization of Ultra Thin Oxynitride Formed by Radical Nitridation with Slot Plane Antenna Plasma
T. Sugawara, T. Nakanishi, M. Sasaki, S. Ozaki and Y. Tada, *Tokyo Electron, Japan*

9:40 B-7-3 # 35
Effect of CF_4 Plasma Pretreatment on TiO_2 High-k Dielectric Film
T.Y. Chang, H.W. Chen, T.F. Lei, T.S. Chao and C.J. Wu*, *National Chiao Tung Univ. and *National Nano Device Labs., Taiwan*

Room C

9:00 C-7-1 # 189
Methodology for Accurate C-V Measurement of Gate Insulators below 1.5nm EOT
H. Suto, Y. Okawa*, M. Takayanagi, H. Norimatsu* and Y. Toyoshima, *Toshiba and *Agilent Technols. Japan, Japan*

9:20 C-7-2 # 427
Mechanisms of Nitrogen Segregation and Hole Trap Generation at the Inter face of SiO_2/Si (100)
T. Yamasaki and C. Kaneta, *Fujitsu Labs., Japan*

9:40 C-7-3 # 97
Impact of Nitrogen Profile on Negative-Bias Temperature Instability and CMOS Performance
M. Terai, T. Yamamoto, K. Watanabe, M. Togo, K. Masuzaki, M. Ikezawa, T. Tatsumi and T. Mogami, *NEC, Japan*

Room D

9:00 D-7-1 # 5030
Future Electron Devices and SOI Technology
T. Hiramoto, *Univ. of Tokyo*

9:30 D-7-2 # 201
Ultra Thin Body Silicon-on-Insulator (UTB SOI) MOSFET with Metal Gate Work-Function Engineering for Sub-70 nm Technology Node
D. Ha, P. Ranade, Y.-K. Choi, J.-S. Lee, T.-J. King and C. Hu, *Univ. of California at Berkeley, USA*

9:50 D-7-3 # 190
Body Potential Design Using Narrow and Shallow Halo to Reduce the Floating Body Effect of SOI-MOSFET
R. Koh, Y. Saito, H. Takemura, K. Arai, M. Narihiro, H. Wakabayashi, K. Takeuchi and T. Mogami, *NEC, Japan*

Room E

Room F

9:00 F-7-1 # 5024
Self Size-Limiting Growth of Uniform InAs Quantum Dots by Molecular Beam Epitaxy
K. Yamaguchi, T. Kaizu, R. Ohtsubo and S. Iwasaki, *Univ. of Electro-Communications, Japan*

9:30 F-7-2 # 40
Fabrication of One- or Double- Row Aligned Self-Organized Quantum Dots by Utilizing SiO_2-Patterned Vicinal(001) GaAs Substrates
H.J. Kim, J. Motohisa and T. Fukui, *Hokkaido Univ., Japan*

9:45 F-7-3 # 302
Fabrication of AlGaN/GaN Quantum Wires by ECR-RIBE Process and Their Electrical Properties
T. Muranaka, Z. Jin, M. Endo, T. Hashizume and H. Hasegawa, *Hokkaido Univ., Japan*

Room G

9:00 G-7-1 # 5011
Gallium Nitride for Wireless Infrastructure
B. Lynch, *Nitronex, USA*

9:30 G-7-2 # 81
Device Temperature Measurement of High-Biased AlGaN/GaN High-Electron-Mobility Transistors
N. Shigekawa, K. Onodera and K. Shiojima, *NTT, Japan*

9:45 G-7-3 # 179
Characterization of Electrical Properties of Micro-Schottky Contacts on ELO GaN
K. Kumada, T. Murata, Y. Ohno, S. Kishimoto, K. Maezawa, T. Mizutani and N. Sawaki, *Nagoya Univ., Japan*

10:00 A-7-4 # 299
Field-Shield Trench Isolation with Self-Aligned Field Oxide
A. Takase, T. Kidera and H. Sunami, *Hiroshima Univ., Japan*

10:00 B-7-4 # 222
Electrical Characteristics of Rare Earth Gate Oxides Improved by Chemical Oxide and Long Low Temperature Annealing
S. Ohmi, I. Kashiwagi, C. Ohshima, J. Taguchi, H. Yamamoto, J. Tonotani, H. Ishiwara and H. Iwai, *Tokyo Inst. of Technol., Japan*

10:00 C-7-4 # 257
Bias and Temperature Dependent Reliability Issues in a 0.18um Generation CMOS Multi-Oxide SoC Technology
S.-J. Chen, C.-C. Lin, S.S. Chung, J.-C. Lin and C-H. Chu*, *National Chiao Tung Univ. and *UMC, Taiwan*

10:10 D-7-4 # 133
High Performance Poly-Si CMOS Circuits Fabricated Using Metal Imprint Technology
K. Makihira, M. Yoshii and T. Asano, *Kyushu Inst. of Technol., Japan*

10:00 F-7-4 # 91
Size and Interface State Dependence of the Luminescence Properties in Si Nano-Crystals
C.-G. Ahn, T.-S. Jang, K.-H. Kim* Y.-K. Kwon** and B. Kang, *Pohang Univ. of Science and Technol., *Kyungpook National Univ. and **Uiduk Univ., Korea*

10:00 G-7-4 # 28
Ohmic Contact to p-GaN Using a Strained InGaN Contact Layer and Its Thermal Stability
K. Kumakura, T. Makimoto and N. Kobayashi, *NTT, Japan*

10:15 F-7-5 # 264
Novel Nonvolatile Random Access Memory with Si Nanocrystals for Ultra Low Power Scheme
A. Shibata, H. Kotaki, T. Ogura, N. Arai, K. Adachi., S. Kakimoto, A. Kito, A. Sakai*, S. Zaima* and Y. Yasuda*, *Sharp and *Nagoya Univ., Japan*

10:15 G-7-5 # 356
GaN Metal-Semiconductor-Meta l Visible-Blind Photodetectors with Transparent Indium-Tin-Oxide Contact Electrode
Y.K. Su, F.S. Juang* and M.-H. Chen, *National Cheng Kung Univ. and *National Huwei Inst. of Technol., Taiwan*

10:20-10:45 Break

10:20-10:45 Break

10:20-10:45 Break

10:30-10:45 Break

10:30-10:45 Break

10:30-15:45 Break

10:45 A-8-1 # 130
Voltage Acceleration of Ultra-Thin Gate Degradation before and after Soft Breakdown
T. Hosoi, S. Uno, Y. Kamakura and K. Taniguchi, *Osaka Univ., Japan*

10:45 B-8-1 # 217
High Selective Etching Using HF/H_2SO_4 Solution
M. Saito, H. Tomita, K. Miyazaki and S. Nadahara, *Toshiba, Japan*

10:45 C-8-1 # 248
Band Offset Energies in Zirconium Silicate Alloys
G. Lucovsky, B. Rayner, Y. Zhang, G. Appel and J. Whitten, *North Carolina State Univ., USA*

10:45 D-8-1 # 5031
Characterization and Challenges of SOI Wafer Material at Present and Its Perspective
C. Maleville, *SOITEC, France*

10:45 F-8-1 # 5025
Investigations towards Semiconductor/Ferromagne t Spin Transistors: Rashba Effect, Local Hall Effect and Spin Injection
Th. Schäpers, *Forschungszentrum Juelich, Germany*

10:45 G-8-1 # 5012
ZrB2 Substrate for Nitride Semiconductor
H. Kinoshita, S. Otani*, S. Kamiyama**, H. Amano**, I. Akasaki**, J. Suda*** and H. Matsunami***, *Kyocera, *AML/NIMS, **Meijo Univ. and ***Kyoto Univ., Japan*

11:05 A-8-2 # 390
Oxide Soft Breakdown Effects on Drain Current Flicker Noise in Ultra-Thin Oxide CMOS Devices
J.-W. Wu, H.-C. Chang and T. Wang, *National Chiao-Tung Univ., Taiwan*

11:05 B-8-2 # 44
Dose Dependent Etching Selectivity SiO_2 by Focused Ion Beam
T. Sadoh, H. Eguchi, A. Kenjo and M. Miyao, *Kyushu Univ., Japan*

11:05 C-8-2 # 204
Depth Profiling of High-K Dielectric/Si Interfacial Transition Layer
T. Shiraishi, T. Nakamura, K. Takahashi, I. Kashiwagi*, C. Ohshima*, H. Nohira, S. Ohmi*, H. Iwai* and T. Hattori, *Musashi Inst. of Technol. and *Tokyo Inst. of Technol., Japan*

11:15 D-8-2 # 150
Reduction of Pattern-Edge Defects in Partial SOI by LII(Light-Ion Implantation) Technique
A. Ogura, *NEC, Japan*

11:15 F-8-2 # 158
(0.5xn)($2e^2$/h) Conductance Steps Observed in Side-Gated Constriction Made at $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ Heterojunction under Zero-Field
S. Yamada, T. Kita, M. Yoshitake, H. Sato and Y. Sato, *JAIST, Japan*

11:15 G-8-2 # 109
Thin GaN on Sapphire with Reduced Bowing by Large Area Laser Lift-Off Technique
M. Ishida, T. Ueda and M. Yuri, *Matsushita Electric, Japan*

11:25 A-8-3 # 374
Novel Deuterated Highly Reliable SiO_2 by SiD_4 Poly-Si Gate Electrode
Y. Mitani and H. Satake, *Toshiba, Japan*

11:25 B-8-3 # 366
Evaluation of Surface Contamination by Noncontact Capacitance Method under UV Irradiation
M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama*, *Dainippon Screen Manufacturing and *Hiroshima Univ., Japan*

11:25 C-8-3 # 380
Photoemission Study of Aluminum Oxynitride/Si (100) Heterostructures - Chemical Bonding Features and Energy Band Lineup -
A. Suyama, H. Yokoi, M. Narasaki, W. Mizubayashi, H. Murakami and S. Miyazaki, *Hiroshima Univ., Japan*

11:35 D-8-3 # 424
Effective Metal Gettering Technique Using Polysilicon Substrate Contact Structure for SOI Devices
H. Naruoka, T. Iwamatsu, T. Ipposhi, N. Hattori, Y. Inoue and Y. Mashiko, *Mitsubishi Electric, Japan*

11:30 F-8-3 # 219
Pulsed-Mode Manipulation of Nuclear Spin Polarization in Integer Quantum Hall Devices
T. Yamazaki, T. Machida, K. Ikushima and S. Komiyama, *Univ. of Tokyo, Japan*

11:30 G-8-3 # 43
Structural Properties on GaN Film through the Introduction of AlN Buffer Layers with Variable Growth Temperatures by Plasma-Assisted Molecular Beam Epitaxy
B.-R. Shim, H. Okita*, K. Jeganathan, M. Shimizu and H. Okumura, *AIST and *Science Univ. of Tokyo, Japan*

11:45 A-8-4 # 199
A Technology of Reducing Flicker Noise for ULSI Applications
K. Tanaka, K. Watanabe, H. Ishino, S. Sugawa, A. Teramoto, M. Hirayama and T. Ohmi, *Tohoku Univ., Japan*

11:45 B-8-4 # 346
Quantum Chemical Molecular Dynamics Simulation on the Plasma Etching Processes
K. Sasata, T. Yokosuka, H. Kurokawa, S. Takami, M. Kubo, A. Imamura*, T. Shinmura**, M. Kanoh** and

11:45 C-8-4 # 227
Direct Evidence of Localized States in High-k Materials for Gate Insulator - Cathode Luminescence Study of HfO_2 Films -
S. Yamasaki and J.-W. Park*, *AIST and *ASET, Japan*

11:55 D-8-4 # 409
Silicon-On-Low-K Substrate (SOLK) Technology for High-Speed and Low-Power Devices
Y. Yamada, Y. Igarashi, T. Morooka, T. Nakamura, J.C. Shim, H. Kurino and M. Koyanagi, *Tohoku Univ., Japan*

11:45 F-8-4 # 262
Enhanced Magneto-Optical Interaction in CdTe/CdMnTe Quantum Wires
S. Nagahara, T. Kita, O. Wada, L. Marsal* and H. Mariette*, *Kobe Univ., Japan and *Univ. J. Fourier, France*

11:45 G-8-4 # 37
GaN-Based Light-Emitting Diodes with Si-Doped $In_{0.23}Ga_{0.77}N$/GaN Short-Period Superlattice Tunneling Contact Layer
C.H. Kuo, S.J. Chang, Y.K. Su, L.W. Wu, J.K. Sheu* and M. Tsai**, *National Cheng-Kung*

A. Miyamoto, *Tohoku Univ., *Hiroshima Kokusai Gakuin Univ. and **Toshiba, Japan*

*Univ., *National Central Univ. and **South Epitaxy, Taiwan*

12:00 G-8-5 # 29
Highly Transparent Structure for Nitride Ultraviolet Light Emitting Diodes
T. Nishida, T. Ban* and N. Kobayashi, *NTT and *NEL, Japan*

13:15 A-9-1 # 200
Mobility Reduction due to Remote Charge Scattering in Al_2O_3/SiO_2 Gate-Stacked MISFETs
S. Saito, Y. Shimamoto, K. Torii, Y. Manabe*, M. Caymax*, J.W. Maes**, M. Hiratani and S. Kimura, *Hitachi, Japan, *IMEC, Belgium and **ASM International, The Netherlands*

13:15 B-9-1 # 296
Suppression of Short Channel Hump of nMOSFET Using NF_3-Added ILD HDP Process
J.-S. Park, S.-K. Choi, M.-J. Bong, S.-C. Chung, H.-C. Jung, N.-S. Kim, T.-U. Youn, Y.-W. Kwon and I.-G. Kim, *Hynix Semiconductor, Korea*

13:15 C-9-1 # 328
0.1 μm pMOSFETs with SiGe-Channel and B-Doped SiGe Source/Drain Layers
D. Lee, M. Sakuraba, J. Murota and T. Tsuchiya*, *Tohoku Univ. and *Simane Univ., Japan*

13:15 D-9-1 # 311
Dynamic Floating Body Effects in Fully Depleted SOI MOSFET's
K. Nagase, K. Fujimoto, M. Yamazaki, S. Suzuki, T. Shinohara and K. Hoshino, *Sharp, Japan*

13:15 F-9-1 # 5026
Generation of Transform-Limited Single Photons from a Quantum Dot
Y. Yamamoto, C. Santori, D. Fattal, J. Olant, J. Vuckovic and B. Zhang, *Stanford Univ., USA*

13:35 A-9-2 # 13
Influences of Gate-Edge Structure on Electric Field Strength in MISFETs with High-k Gate Dielectrics
M. Ono and A. Nishiyama, *Toshiba, Japan*

13:35 B-9-2 # 338
Investigation of the Ti-Doped Ta_2O_5 Films from PET and TET Cocktail Source for DRAM Capacitor
K.J. Nam, K.C. Kim, J.S. Lim, K.V. Lim, Y.S. Kim, S.T. Kim, U.I. Chung and J.T. Moon, *Samsung Electronics, Korea*

13:35 C-9-2 # 42
Metal-Induced Solid-Phase Crystallization of Amorphous SiGe Films on Insulator
H. Kanno, I. Tsunoda, A. Kenjo, T. Sadoh, S. Yamaguchi* and M. Miyao, *Kyushu Univ. and *Hitachi, Japan*

13:35 D-9-2 # 392
Current Drive Improvement by Enhanced Body Effect Factor Due to Finite Inversion Layer Thickness in Variable Threshold Voltage CMOS
T. Nagumo and T. Hiramoto, *Univ. of Tokyo, Japan*

13:45 F-9-2 # 386
Optical Characteristics of Two-Dimensional Photonic Crystal Slab Nanocavities with Self-Assembled InAs Quantum Dots Emitting at Over 1.3-μm
J. Tatebayashi, S. Iwamoto, S. Kako, S. Ishida and Y. Arakawa, *Univ. of Tokyo, Japan*

13:55 A-9-3 # 315
SiO_2/Si Suboxide Characteristics of Ultra-Thin Gate Oxides Prepared by Room Temperature Anodic Oxidation and Rapid Thermal Oxidation
Y.-P. Lin, Z.-H. Chen and J.-G. Hwu, *National Taiwan Univ., Taiwan*

13:55 B-9-3 # 275
Impact of Thermal Budget Reduction on MOSFET Performance to Achieve High-Speed and High-Density DRAM-Based System LSI
E. Yoshida, T. Miyashita, H. Nitta*, M. Tanaka*, K. Ishii*, Y. Akasaka*, P.H. Chou**, K. Hashimoto, Y, Kohyama*, T. Tanaka and Y. Nara, *Fujitsu Labs., *Toshiba, Japan and Winbond Electronics, Taiwan*

13:55 C-9-3 # 191
Boron Doped Polycrystalline $Si_{1-x}Ge_x$ Resistors for High Precision Analog ICs
H. Watanabe, M. Tamura*, M. Dainin, M. Seto, T. Shohbu, Y. Ohsako, Y. Takimoto, Y. Ishimoto, H. Ino, E. Imanishi, M. Satoh, H. Satoh, K. Yamashita and K. Taniguchi*, *Ricoh and *Osaka Univ., Japan*

13:55 D-9-3 # 417
FD-SOI MOSFET with Self-Aligned Gate Formed on Recessed Channel
Y. Soutome, K. Isaji, H. Aoki, A. Kawamura, H. Komiya and K. Iguchi, *Sharp, Japan*

14:00 F-9-3 # 373
Ultrafast Exciton Dynamics in GaAs Crescent-Shaped Quantum Wires
T. Yasuhira, K. Komori, R. Akimoto, X.L. Wang, M. Watanabe and M. Ogura, *AIST, Japan*

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Effects of Metal Concentration Nonuniformity in Gate Dielectric Silicates on Propagation Delay Time of CMIS Inverters
M. Ono, T. Ino, M. Koyama, A. Takashima and A. Nishiyama, *Toshiba, Japan*

14:15 B-9-4 # 234
Performance of DRAM Cell Transistor with TDSE (Thermal Desorption Silicon Etching) and Selective Si Channel Epi Techniques
C.S. Kim, B.C. Lee, J.R. Ryu, D.-H. Lee, J.-H. Ku, S. Choi, U.I. Chung and J.T. Moon, *Samsung Electronics, Korea*

14:15 C-9-4 # 221
Control of 2 type Dielectric Relaxation Current of Ta_2O_5 Metal-Insulator-Metal [MIM] Capacitors
M. Kiyotoshi, K. Hieda, Y. Fukuzumi, Y. Kohyama, T. Suzuki*, D. Matsunaga* and K. Hashimoto*, *Toshiba and * Fujitsu, Japan*

14:15 D-9-4 # 70
Hot-Carrier-Induced Degradation on 0.1 μm Partially Depleted SOI CMOSFET with Thin Oxide
W.-K. Yeh, W.-H. Wang*, Y.-K. Fang* and F.-L. Yang**, *National Univ. of Kaohsiung, *National Cheng Kung Univ. and **TSMC, Taiwan*

14:15 F-9-4 # 5027
Quantum Mechanical Time-Evolution of Exciton States in Semiconductor Quantum Dots: Quantum Gate Operation of Exciton Qubits
H. Kamada, H. Ando*, T. Takagahara** and J. Temmyo***, *NTT, *Konan Univ., **Kyoto Inst. of Technol. and ***Shizuoka Univ., Japan*

14:35 B-9-5 # 274
Highly Reliable DRAM Technology for ASM with Dual Nitrogen Concentration Gate Oxynitrides Using Selective Nitrogen Implantation
T. Sugizaki, A. Murakoshi*, T. Tanaka, R. Katsumata*, T. Nakanishi and Y. Nara, *Fujitsu Labs. and *Toshiba, Japan*

14:55 B-9-6 # 235
Investigation of the Contact Resistance between Ru and Ti/TiN in M1/Plate Contacts of RIS(Ruthenium Insulator Silicon) Capacitor
J.Y. Yun, B.H. Kim, S.G. Park, J.H. Seo, J.M. Lee, S.B. Kang, J.H. Chung, G.H. Choi, U.I. Chung and J.T. Moon, *Samsung Electronics, Korea*

14:35 C-9-5 # 205
Electrical Properties of High-k MIM Interlevel Capacitors Prepared for RF-CMOS Device Applications
M. Tarutani, K. Shintani, T. Mori, K. Nishikawa, Y. Hashizume, S. Yamakawa, H. Takada and T. Oomori, *Mitsubishi Electric, Japan*

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Grain-Boundary Related Hot Carrier Degradation Mechanism in Low-Temperature Poly-Si Thin-Film-Transistors
T. Yoshida, Y. Ebiko*, M. Takei*, N. Sasaki* and T. Tsuchiya, *Shimane Univ. and * Fujitsu Labs., Japan*