

SSDM 2003 Condensed Program

Tuesday, September 16							
EMINENCE HALL							
9:30 - 12:30 PL: Opening Session							
Room A	Room B	Room C	Room D	Room E	Room F	Room G	
14:00-15:50 A-1: Advanced Silicon Devices and Device Physics -Gate Stack Technologies- (5 papers)	14:00-16:00 B-1: Non-Volatile Memory Technologies -Non-Volatile Memory I- (5 papers)	14:00-15:50 C-1: Silicon Process / Materials Technologies -High-k Gate Dielectric I- (5 papers)	14:00-16:00 D-1: New Characterization -Oxide Reliability Characterization- (6 papers)	Materials and Surface	14:00-16:00 E-1: Quantum Nanostructure Materials and Physics -Fabrication and Micromechanics- (7 papers)	14:00-16:00 F-1: Compound Semiconductor Materials and Devices -III-V and Nitride Electron Devices- (7 papers)	14:00-15:50 G-1: Advanced Silicon Circuits and Systems -Advanced CMOS Circuits and Systems- (5 papers)
16:15-18:15 A-2: Advanced Silicon Devices and Device Physics -Advanced CMOS Technology I- (6 papers)	16:15-17:35 B-2: Non-Volatile Memory Technologies -Non-Volatile Memory II- (4 papers)	16:15-17:55 C-2: Silicon Process / Materials Technologies -High-k Gate Dielectric II- (5 papers)	16:15-18:15 D-2: New Characterization -Low k and Characterization- (6 papers)	Materials and Silicide	16:15-18:00 E-2: Quantum Nanostructure Devices and Physics -Nanostructured Optical Devices- (6 papers)	16:15-18:00 F-2: Compound Semiconductor Materials and Devices -Nitride Electron Devices- (6 papers)	16:15-17:45 G-2: Advanced Silicon Circuits and Systems -Collaboration of Circuits and Devices- (4 papers)
18:30-20:30 Banquet, Eminence Hall							
Wednesday, September 17							
Room A	Room B	Room C	Room D	Room E	Room F	Room G	
9:00-10:30 A-3: Advanced Silicon Devices and Device Physics -High-k Technology I- (4 papers)	9:00-10:20 B-3: Non-Volatile Memory Technologies -Non-Volatile Memory III- (3 papers)	9:00-10:30 C-3: Silicon Process / Materials Technologies -Memory Technology- (4 papers)	9:00-10:30 D-3: Silicon-Technologies -SOI Novel (4 papers)	on-Insulator Devices-	9:00-10:15 E-3: Quantum Nanostructure Devices and Physics -Characterization and Nanoprobing- (5 papers)	9:00-10:15 F-3: Compound Semiconductor Materials and Devices -Novel Compound Semiconductors Devices- (3 papers)	9:00-10:30 G-3: Advanced Silicon Circuits and Systems -Circuit Technologies for Emerging Technologies- (4 papers)
10:45-12:00 A-4: Optoelectronic Devices and Photonic Crystal Devices -VCSELs and Visible Lasers- (4 papers)	10:45-12:05 B-4: Non-Volatile Memory Technologies -Non-Volatile Memory IV- (4 papers)	10:45-12:05 C-4: Silicon Process / Materials Technologies -DRAM- (4 papers)	10:45-12:05 D-4: Silicon-Technologies -SOI Device (4 papers)	on-Insulator Physics-	10:45-12:15 E-4: Quantum Nanostructure Devices and Physics -Spin-related Phenomena- (5 papers)	10:45-12:15 F-4: Compound Semiconductor Materials and Devices -Optical Devices- (5 papers)	10:45-11:45 G-4: System-Level Integration and Packaging Technologies -System-Level Integration and Packaging Technologies I- (3 papers)
13:00-15:00 Poster Session (OHGI)							
15:15-16:45 A-5: Optoelectronic Devices and Photonic Crystal Devices -Optoelectronic Integrated Devices- (5 papers)	15:15-16:30 B-5: Organic Semiconductor Devices and Materials -Preparation and Characterization- (5 papers)	15:15-16:45 C-5: Silicon Process / Materials Technologies -Interconnect- (4 papers)	15:15-16:45 D-5: Silicon-Technologies -Fin FET (4 papers)	on-Insulator Technologies-	15:15-16:30 E-5: Quantum Nanostructure Devices and Physics -Single Electron Transport- (4 papers)	15:15-16:45 F-5: Micro-Nano Electromechanical Devices for Bio- and Chemical Applications -Micro-Nano Electro Mechanical Devices for Bio-and Chemical Applications I- (5 papers)	15:15-16:45 G-5: System-Level Integration and Packaging Technologies -System-Level Integration and Packaging Technologies II- (4 papers)
17:00-18:15 A-6: Optoelectronic Devices and Photonic Crystal Devices -Lasers for Optical Communication- (4 papers)	17:00-17:40 B-6: Non-Volatile Memory Technologies -Non-Volatile Memory V- (2 papers)	17:00-18:20 C-6: Silicon Process / Materials Technologies -Interconnect- (4 papers)	17:00-18:30 D-6: New Characterization -Si/SiGe Materials- (4 papers)	Materials and Devices and	17:00-18:30 E-6: Novel Devices, Physics, and Fabrication -Nanoprocess and Nanodevices- (5 papers)	17:00-18:00 F-6: Micro-Nano Electromechanical Devices for Bio- and Chemical Applications -Micro-Nano Electro Mechanical Devices for Bio-and Chemical Applications II- (3 papers)	17:00-18:15 G-6: System-Level Integration and Packaging Technologies -System-Level Integration and Packaging Technologies III- (4 papers)
18:45-20:45 Rump Session Room A "Can channel material/structure engineering become a guiding principle for future CMOS device technology?" Room B "What paradigm can nanoelectronic devices bring about?"							
Thursday, September 18							
Room A	Room B	Room C	Room D	Room E	Room F	Room G	
9:00-10:30 A-7: Advanced Silicon Devices and Device Physics -High-k Technology II- (4 papers)	9:00-10:20 B-7: Silicon Process / Materials Technologies -Metal Gate, Gate Oxide- (4 papers)	9:15-10:30 C-7: Organic Semiconductor Devices and Materials -Organic Thin Film Transistor- (4 papers)	9:20-10:30 D-7: New Characterization -Carbon Devices and (3 papers)	Materials and Nanotube Materials-	9:30-10:30 E-7: Novel Devices, Physics, and Fabrication -Novel Materials and Devices- (4 papers)	9:00-10:30 F-7: Optoelectronic Devices and Photonic Crystal Devices -Photonic Crystal Devices I- (5 papers)	9:00-10:30 G-7: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -III-V Devices & Circuits- (5 papers)
10:45-12:05 A-8: Advanced Silicon Devices and Device Physics -Advanced CMOS Technology II- (4 papers)	10:45-12:05 B-8: Silicon Process / Materials Technologies -Si Process- (4 papers)	10:45-12:00 C-8: Organic Semiconductor Devices and Materials -Organic Optics- (5 papers)	10:45-11:25 D-8: New Characterization -High-k (2 papers)	Materials and Dielectrics I-	10:45-12:00 E-8: Novel Devices, Physics, and Fabrication -Carbon Nanotubess- (4 papers)	10:45-11:45 F-8: Optoelectronic Devices and Photonic Crystal Devices II- (3 papers)	10:45-11:45 G-8: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -SiGe Technologies- (3 papers)
13:30-14:50 A-9: Advanced Silicon Devices and Device Physics -Electron Mobility Characteristics- (4 papers)	13:30-14:40 B-9: Silicon-on-Insulator Technologies -SOI Low Power Applications- (3 papers)	13:30-14:45 C-9: Organic Semiconductor Devices and Materials -Molecular Devices and Materials- (4 papers)	13:30-14:30 D-9: New Characterization -High-k (3 papers)	Materials and Dielectrics II-	13:30-14:30 E-9: Novel Devices, Physics, and Fabrication -Si Nanowire and Dots- (3 papers)	13:30-14:45 F-9: Optoelectronic Devices and Photonic Crystal Devices -Ultrafast Photonic Devices- (4 papers)	13:30-14:45 G-9: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -GaN Devices- (4 papers)
15:00-16:00 A-10: Advanced Silicon Devices and Device Physics -Poly-Si Device and Sensor- (3 papers)	15:00-16:30 B-10: Silicon-on-Insulator Technologies -SOI CMOS Technologies- (4 papers)	15:00-16:00 C-10: Organic Semiconductor Devices and Materials -Electroluminescent Devices and Materials- (4 papers)	15:00-16:20 D-10: New Characterization -High-k (4 papers)	Materials and Dielectrics III-	15:00-16:15 E-10: Novel Devices, Physics, and Fabrication -Quantum Computing Devices- (4 papers)	15:00-16:00 F-10: Optoelectronic Devices and Photonic Crystal Devices -New Photonic Materials- (4 papers)	15:00-16:00 G-10: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -High Voltage Devices- (3 papers)

SSDM 2003 Advance Program

General Information

DATE

Conference: **September 16-18, 2003**

Short Course: **September 19, 2003 (in Japanese)**

LOCATION

Keio Plaza Inter-Continental Tokyo (Keio Plaza Hotel)

2-2-1 Nishi-Shinjuku, Shinjuku-Ku, Tokyo 160-8330

TEL +81-3-3344-0111 FAX +81-3-3345-8269

Keio Plaza Inter-Continental Tokyo is approximately 120 minutes by Airport Bus from New Tokyo International Airport (Narita), and only 5 minutes by walking from JR Shinjuku Station.

Web site: <http://www.keioplaza.com/index.html>

REGISTRATION

The registration desk will be open from September 15th to 19th. The registration hours are as follows:

September 15	17:00-19:00	MITAKE, 42F
16	8:00-12:00	front of EMINENCE HALL, 5F
	13:00-17:00	front of TSUKUI, 42F
17	8:00-15:30	"
18	8:00-15:30	"
19	8:00-13:30	(Short Course) "

Pre-registration is accepted only through the conference website before September 1, 2003. After that date, registration can be made at the conference site. Early registration is recommended due to the expected large number of participants.

	Registration Fee		Short Courses in Japanese	Banquet
	On or before August 1	After August 1		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanying person(s)				¥4,000/person

- 1) The registration fee includes one copy of the abstract book, a CD-ROM and coffee breaks. However, it does not include the Banquet, and extra payment of 7,000 yen or 4,000 yen is required to attend the Banquet for regular participants and student participants, respectively.
- 2) Those who register as students are required to fax a copy of their current student ID to the secretariat at the time of registration, and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of online registration of individual information.
- 3) Registration is complete only with full payment.

Payment of the registration fee is to be made by one of the following methods. Please note that we do not accept personal checks.

1. Bank Transfer

A direct bank transfer can be made to the account below. A copy of the receipt for the bank remittance should be sent to the secretariat by fax. The registration ID must be written on the fax sheet. Please

note that the bank service charge must be borne by the applicant.

- Name of Bank: Bank of Tokyo-Mitsubishi, Akasaka Branch
- Account Name: SSDM2003
- Account No: 1528425 (ordinary deposit)

2. Credit Card

Amex, VISA, MasterCard, Diners Club and JCB are acceptable.

Confirmation of Pre-Registration

The Secretariat will e-mail a confirmation to you after verifying payment in early September. Please print the confirmation slip out, bringing it with you to the conference and present it at the registration desk.

REGISTRATION CANCELLATION

Conference:

Cancellation fee of ¥3,000 will be deducted from the refund. Cancellation should be made in writing to the SSDM 2003 Secretariat. No cancellation will be accepted after August 19, 2003. Extended Abstracts will be sent to absent registrants after the Conference.

Short Course:

Cancellation fee of ¥2,000 will be deducted from the refund. Cancellations should be made in writing to the SSDM 2003 Secretariat. No cancellation will be accepted after August 19. A text will be sent to the absent registrants after the Conference.

BANQUET

Banquet will be held at "Eminence Hall" of the Keio Plaza Inter Continental Tokyo (5F) on September 16 from 18:30-20:30. Tickets (Regular ¥7,000 / Student ¥4,000) can be purchased at the registration desk.

LATE NEWS PAPERS

Late News Paper Deadline is July 25, 2003.

Late news papers describing important new developments may be submitted. A 2-page paper must be sent in the camera-ready format as required for the regular papers. The accepted papers will be included in the extended abstracts.

The abstract must be submitted through the conference Web site: <http://www.intergroup.co.jp/ssdm>. Notice of acceptance will be e-mailed by the middle of August.

EXTENDED ABSTRACTS AND PUBLICATION

Authors of papers accepted for SSDM 2003 are encouraged to submit the original and significant part of the papers to the Special Issue of the Japanese Journal of Applied Physics. The special issue will be published in April 2004. Please refer to the conference website for details.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

Submission of an abstract for review and subsequent acceptance is considered by the committee as an agreement that the work will not be published by the author prior to the presentation at the conference. This policy will be enforced by the automatic withdrawal of the paper by the conference committee.

AWARDS

"SSDM Awards" will be given to excellent papers presented in the previous conferences.

SSDM Award

For the paper, which made an outstanding contribution to the field of solid state devices and materials, among the papers presented prior to 1997.

SSDM Paper Award

For the best paper presented at the last conference.

SSDM Young Researcher Award

For a few excellent papers by young researchers presented at the last conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter.

VISA REQUIREMENT

All foreign participants must have valid passport. Participants from countries where a visa is required to enter Japan are recommended to apply at the nearest Japanese embassy in their countries as soon as possible.

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT) has been appointed as the official travel agent for the conference and will handle accommodations.

Kinki Nippon Tourist Co., Ltd.
Event, Convention and Congress Department
6F, Kyodo Bldg., 2-2 Kanda-Jinbocho, Chiyoda-ku, Tokyo 101-0051 Japan
Phone:+81-3-3263-5581, Fax:+81-3-3263-5961
E-mail:SSDM2003@knt-tokyo.gr.jp

HOTEL ACCOMMODATIONS

Hotel accommodations for the nights of September 15(in) - 19(out) are now available **through the conference website**. Early reservation is recommended due to the expected large number of participants.

#	Hotel Name	Single W/bath	Twin W/bath	Location	Grade
①	<i>Keio Plaza Inter-Continental Tokyo</i>	¥19,100	¥25,400	Shinjuku Station (walk 5 min)	Deluxe
②	<i>Hotel SunRouteTokyo</i>	¥11,860	¥16,170	Shinjuku Station (walk 3 min)	Superior
③	<i>Shinjuku Washington Hotel</i>	¥12,700	¥15,750	Shinjuku Station (walk 7 min)	Superior

All room rates include breakfast, service charge and consumption tax.

APPLICATION AND PAYMENT OF DEPOSIT

1. Participants wishing to make reservations for accommodations should submit your reservation form by the "Online Reservation button" at the conference website. Then your application form is transmitted to KNT. Reservation will close at August 15, 2003. Reservation should be proceeded on first come first served basis. Applications for hotel reservations should be accompanied by a deposit of 10,000 yen. Please pay for the balance at the hotel.
2. Payments must be made by either one of the following:
 - a. Credit cards (Visa, MasterCard, American Express, JCB); Please fill in the Credit Card Authorization in the application form.
 - b. Bank transfer; Please remit the deposit plus a handling charge to the following account.

Name of bank: **Sumitomo Mitsui Banking Corp., Chuo Branch**
Name of Account: **Kinki Nippon Tourist Co., Ltd.**
Account Number: **1855682**

NOTE: Personal checks are not acceptable. We would appreciate your kindly sending us a photocopy of the bank's receipt for your remittance.

CANCELLATION

In case of changes or cancellations, please inform KNT by FAX or E-mail. KNT accepts only written notification. The following cancellation fees apply according to the date of your notification.

5 to 2 days prior to the first night	¥1,000
1 day prior to the first night	50% of daily room charge
The first night or no notice given	100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

The temperature in Tokyo during the period of the conference ranges between 18 and 30 degrees centigrade.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

RUMP SESSIONS - September 17 (Wednesday) 18:45-20:45

Rump session 1 (Room A, FUJI, 42F)

“Can channel material/structure engineering become a guiding principle for future CMOS device technology?”

The simple device scaling rule has been facing to several physical and fundamental limitations, leading to severe trade-off relationships among device performance, short channel effects and power consumption. As one possible solution to avoid this difficulty, new channel structures different from conventional planar Si channel are currently stirring a strong interest. This channel engineering mainly includes two directions; one is new channel materials with high carrier mobility, such as strained-Si, SiGe and Ge, and the other is 3-dimensional channel structures to enhance gate control over channel potential, such as FinFET, double gate MOS, Gate-all-around (GAA) MOS and vertical MOS. However, a scenario for continuously improving the device characteristics under these many engineering options has not been clarified yet. Thus, it is a good timing to examine possibilities, realities and major roles of these non-classical MOSFETs for future technology nodes.

In this rump session, we would like to discuss following issues. (1) Can further and continuous improvements of CMOS characteristics be really achieved by channel material/structure engineering? (2) What is a guiding principle for CMOS device technologies in the future nodes, still smaller size, channel materials, channel geometrical structures or anything else? (3) What are critical issues in the competition between classical vs. non-classical CMOS?

Organizer	Panelists	
S. Takagi (Toshiba, MIRAI-ASET, Japan)	T.-J. King (UCB, USA) T. Skotnicki (STMicro, France) K. Rim (IBM, USA) K. Ishimaru (Toshiba, Japan) T. Takagi (Matsushita, Japan) T. Sugii (Fujitsu, Japan)	FinFET, UTB SOI, Ge MOS SON, GAA MOS, Si/SiGeC MOS strained-Si/Strained-SOI CMOS Advanced CMOS, Bulk CMOS SiGe Analog Devices, SiGe/SiGeC HBT From the viewpoint of ITRS

Rump session 2 (Room B, TAKAO, 42F)

“ What paradigm can nanoelectronic devices bring about? ”

Nanotechnology is expected to be a key technology in the 21st century bringing innovations for materials and devices. What kind of innovations are expected in the electronic devices by reducing the device feature sizes to nanometer-scale or even controlling molecular and atomic structures? Are the nanoelectronic devices positioned as a post-Si CMOS in the miniaturization limit, or will they co-exist with Si-CMOS devices by realizing new functions which are hardly provided solely by present Si devices? What paradigm can the nanoelectronic devices bring about in the future information society? From those standpoints, we would like to discuss future prospect of the nanoelectronic devices in the rump session, mainly by focusing on carbon nanotube devices, molecular/atomic and organic electronic devices, spin-electronic devices, and ultra small-scaled Si devices.

Moderators	Panelists	
J. Sone (NEC, Japan) Y. Wada (Waseda Univ., Japan)	H.-S. P. Wong (IBM, USA) Y. Awano (Fujitsu, Japan) K. Kudo (Chiba Univ., Japan)	Carbon nanotube electronics Carbon nanotube electronics Organic semiconductor devices
Organizer J. Sone (NEC, Japan)	M. Tanaka (Univ. of Tokyo, Japan) T. Hiramoto (Univ. of Tokyo, Japan)	Spin electronics Nanostructured Si MOS

SHORT COURSES

Two short courses will be held on September 19 (Friday) for young engineers and students. All lectures are given in Japanese. Please refer to the attached information for details.

SSDM 2003 INSTRUCTION for SPEAKERS

<Oral Presentation>

Presentation Time

	Session Time	Presentation Time	Discussion
Plenary	45 min.	40 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of the presentation time, Third: End of the discussion time.

Audio-Visual Equipment

The meeting room will contain the following audiovisual equipment:

- Overhead projector
- LCD data projector (PC is not provided)
- Microphone
- Projection laser pointer

It is strongly recommended that you use the Overhead projector for your presentation.

Authors wishing to present their paper using LCD projector are requested to bring overhead transparencies preparing for an unforeseen accident.

<Poster Presentation>

Poster Sessions are scheduled as follows:

13:00-15:00 on Wednesday, September 17

Authors must remain in the vicinity of the bulletin board for the duration of the session to answer questions.

900mm(W) x 2,100mm(H) poster board, a sign indicating your paper number and push pins will be provided at the poster room, OHGI, 4F. Presenters should display, on their poster, the paper title, authors and affiliation.

Authors are requested to prepare their poster materials during:

9:00 to 12:00 of September 17.

Please put their poster materials off by:

17:00 on September 17.

PL: Opening Session (9:30 - 12:30)

Chairpersons: S. Kawamura, AIST and M. Koyanagi, Tohoku Univ.

9:30 PL-0

Welcome Address and Award Presentation
M. Nakamura, Hitachi

9:45 PL-1 (Plenary)

Research and Development Strategy for Creation of Corporate Value
T. Ikoma, Hitotsubashi Univ., Japan

10:30 PL-2 (Plenary)

Role and Strategy of IMEC as a European Player in a Globalized Research Era
G.J. Declerck, IMEC, Belgium

11:15 PL-3 (Plenary)

Progress and Perspective of Nanostructure Devices for Ubiquitous Information Network
Y. Arakawa, Univ. of Tokyo, Japan

12:30-14:00 Lunch

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>A-1: Advanced Silicon Devices and Device Physics -Gate Stack Technologies- (14:00-15:50) Chairs: T. Mogami (NEC) K. Shibahara (Hiroshima Univ.)</p>	<p>B-1: Non-Volatile Memory Technologies -Non-Volatile Memory I- (14:00-16:00) Chairs: T. Nakamura (Rohm) Y. Shimada (Matsushita Electric)</p>	<p>C-1: Silicon Process / Materials Technologies -High-k Gate Dielectric I- (14:00-15:50) Chairs: Y. Tsunashima (Toshiba) H. Kitajima (Selete)</p>	<p>D-1: New Materials and Characterization -Oxide Reliability and Surface Characterization- (14:00-16:00) Chairs: H. Satake (Toshiba) T. Maruizumi (Hitachi)</p>	<p>E-1: Quantum Nanostructure Devices and Physics -Fabrication and Micromechanics- (14:00-16:00) Chairs: Y. Hirayama (NTT) J. Motohisa (Hokkaido Univ.)</p>	<p>F-1: Compound Semiconductor Materials and Devices -III-V and Nitride Electron Devices- (14:00-16:00) Chairs: T. Mizutani (Nagoya Univ.) M. Kuzuhara (FED)</p>	<p>G-1: Advanced Silicon Circuits and Systems -Advanced CMOS Circuits and Systems- (14:00-15:50) Chairs: T. Kuroda (Keio Univ.) M. Fujishima (Univ. of Tokyo)</p>
<p>14:00 A-1-1 (Invited) Dual workfunction metal-gate FinFET devices fabricated using total gate silicidation J. Kedzierski¹, E. Nowak², M. Jeong³, T. Kanarski², and D. Boyd⁴, ¹SRDC, IBM, ²Microelectronics Division, USA</p>	<p>14:00 B-1-1 (Invited) Current FeRAM Technology Developments and Scaling towards 3-D Capacitor Cells D.J. Wouters¹, ¹IMEC, Belgium</p>	<p>14:00 C-1-1 (Invited) Mobility in high-kdielectric based field effect transistors L-A Ragnarsson¹, W. Tsai², A. Kerber³, P.J. Chen⁴, E. Cartier⁵, L. Pantisano⁶, S. De Gendt¹, and M. Heyns¹, ¹IMEC, Belgium, ²Intel Corp., ³Infineon, ⁴Texas Instruments, USA, and ⁵IBM</p>	<p>14:00 D-1-1 The Effect of Boron and Fluorine Incorporation in SiON Gate Insulator on NBTI T. Sasaki¹, F. Ootsuka¹, H. Ozaki¹, M. Tomikawa¹, M. Yasuhira¹ and T. Arikado¹, ¹SELETE, Japan</p>	<p>14:00 E-1-1 (Invited) Electronic and photonic devices via one-dimensional stacking of quantum structures L. Samuelson¹, ¹Lund Univ., ²Solid State Physics/the Nanometer Consortium</p>	<p>14:00 F-1-1 (Invited) Ultrahigh Performance InP HEMTs A. Endoh¹, Y. Yamashita¹, K. Shinohara², K. Hikosaka¹, T. Matsui³, S. Hiyamizu⁴, and T. Mimura¹, ¹Fujitsu Labs Ltd., ²Osaka Univ., Japan</p>	<p>14:00 G-1-1 (Invited) Silicon Integration of UWB: Choices and Challenges S.G. Narendra ¹Circuit Research - Intel Labs, USA</p>
<p>14:30 A-1-2 Influences of Gate-Poly Impurity Concentration on Inversion-Layer Mobility in MOSFETs with Ultrathin Gate Oxide Film J. Koga¹, T. Ishihara¹ and S. Takagi¹, ¹Toshiba Corp., Japan</p>	<p>14:30 B-1-2 (Invited) 32Mb Chain FeRAM -An Overview D. Takashima¹ and T. Rohr², ¹Toshiba Corp., and ²Infineon Technologies Japan K.K., Japan</p>	<p>14:30 C-1-2 Effect of the Film Composition of HfAlON Gate Dielectric on the Structural Transformation and the Electrical Properties through High-temperature Annealing M. Koyama¹, Y. Kamimuta¹, M. Koike¹, M. Suzuki¹ and A. Nishiyama¹, ¹Toshiba Corp., Japan</p>	<p>14:20 D-1-2 New insights into dynamic negative bias temperature instabilities of pMOSFETs S.S. Tan¹, T.P. Chen¹, C.H. Ang², W.Y. Teo² and L. Chan³, ¹Nanyang Technological Univ. of Singapore and ²Chartered Semiconductor Manu. Ltd., Singapore</p>	<p>14:30 E-1-2 Formation of 1μm-period GaAs Kagome Lattice Structure by Selective Area Metalorganic Vapor Phase Epitaxy P. Mohan¹, J. Motohisa¹ and T. Fukui¹, ¹Hokkaido Univ., Japan</p>	<p>14:30 F-1-2 High fr 30nm In_{0.7}GaAs HEMT fabricated with SiO₂/SiN_x sidewall Process and BCB Planarization D.-H. Kim¹, S.-J. Yeon¹, S.-S. Song¹ and K.-S. Seo¹, ¹Seoul National Univ., Korea</p>	<p>14:30 G-1-2 Low-Power Real-Time Region-Growing Image-Segmentation in 0.35μm CMOS due to BAO-Scheme and Subdivided-Image Approach T. Morimoto¹, Y. Harada¹, T. Koide¹ and H.J. Mattausch¹, ¹Hiroshima Univ., Japan</p>

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>14:50 A-1-3 New Self-aligned Metal-gate MOSFETs Using Aluminum Substitution Technology S. Nakamura¹, H. Shido¹, T. Kurahashi¹, S. Kishii¹, T. Nagata¹, B. Kumasaka¹, T. Usuki¹, S. Sato¹ and Y. Mishima¹, ¹<i>Fujitsu Labs Ltd., Japan</i></p>	<p>15:00 B-1-3 A proposal of new ferroelectric gate field effect transistor memory based on ferroelectric-insulator interface conduction G. Hirooka¹, M. Noda¹ and M. Okuyama¹, ¹<i>Osaka Univ., Japan</i></p>	<p>14:50 C-1-3 Projection of Mobility Degradation in HfAlO₂/SiO₂ nMOSFET towards the Reduction of Interfacial Oxide Thickness N. Yasuda¹, H. Hisamatsu¹, H. Ota², K. Iwamoto², K. Tominaga¹, K. Yamamoto¹, W. Mizubayashi², N. Yamagishi², M. Ohno³, S. Migita², Y. Morita², T. Horikawa², T. Nabatame¹ and T. Toriumi^{2,3}, ¹<i>MIRAI-ASET</i>, ²<i>MIRAI-ASRC</i> and ³<i>The Univ. of Tokyo, Japan</i></p>	<p>14:40 D-1-3 Neighboring effect in nitrogen-enhanced negative bias temperature instability S.S. Tan¹, T.P. Chen¹, J.M. Soon², K.P. Loh², C.H. Ang¹, W.Y. Teo¹ and L. Chan¹, ¹<i>Nanyang Technological Univ. of Singapore</i>, ²<i>National Univ. of Singapore</i> and ³<i>Chartered Semiconductor Manu. Ltd., Singapore</i></p>	<p>14:45 E-1-3 Selective MBE Growth of GaAs Hexagonal Nano-wire Networks on (111)B Patterned Substrates S. Yoshida¹, I. Tamai¹, T. Sato¹ and H. Hasegawa¹, ¹<i>Hokkaido Univ., Japan</i></p>	<p>14:45 F-1-3 Observation of Thermal Reliability of BCB Passivated InAlAs/InGaAs HEMTs M. Yoon¹, T. Kim¹, D. Kim¹ and K. Yang¹, ¹<i>KAIST, Korea</i></p>	<p>14:50 G-1-3 Butterfly-Unit Based Programmable Computation Element Using Merged Module of Multiplication, Division and Square Root L. Karnan¹, N. Miyamoto¹, K. Maruo¹, K. Kotani¹ and T. Ohmi², ¹<i>Tohoku Univ.</i> and ²<i>NICHE, Tohoku Univ., Japan</i></p>
<p>15:10 A-1-4 Screening Effect on Remote Coulomb Scattering due to impurities in Polysilicon Gate of MOSFET T. Ishihara¹, J. Koga¹, S. Takagi¹ and K. Matsuzawa¹, ¹<i>Toshiba Corporation, Japan</i></p>	<p>15:20 B-1-4 Long-Term Stabilization of Sense Signals in a Non-Destructive Readout FeRAM by Intentional Modification of the Polarization Hysteresis Curve for Low Voltage Applications T. Yamada¹, Y. Kato¹, S. Koyama¹ and Y. Shimada¹, ¹<i>Matsushita Electric Industrial Co., Ltd., Japan</i></p>	<p>15:10 C-1-4 Ultra-thin (EOT<1.0nm) Amorphous HfSiON Gate Insulator with High Hf Concentration for High-performance Logic Applications M. Koike¹, T. Ino¹, M. Koyama¹, Y. Kamata¹, Y. Kamimuta¹, M. Suzuki¹, A. Takashima¹, Y. Mitani¹, A. Nishiyama¹ and Y. Tsunashima¹, ¹<i>Toshiba Corporation, Japan</i></p>	<p>15:00 D-1-4 Conductive Atomic Force Microscopy Analysis for Local Electric Characteristic in Stressed SiO₂ Gate Films Y. Watanabe¹, A. Seko², H. Kondo², A. Sakai², S. Zaima² and Y. Yasuda², ¹<i>Toyota Central R&D Labs., Inc.</i>, ²<i>Nagoya Univ., Japan</i></p>	<p>15:00 E-1-4 Migration-induced Ge Dot Formation S. Kaechi¹, D. Kitayama¹ and Y. Suda¹, ¹<i>Tokyo Univ. of Agriculture & Technology, Japan</i></p>	<p>15:00 F-1-4 High f_{max} 0.1 μm Γ-gate InGaAs/InAlAs/GaAs Metamorphic HEMT B.H. Lee¹, B.O. Lim¹, M.R. Kim¹, S.D. Kim¹, J.K. Rhee¹ and H.S. Yoon², ¹<i>MINT</i> and ²<i>Electronics and Telecommunications Research Inst., Korea</i></p>	<p>15:10 G-1-4 A Hierarchical 512-Kbit SRAM with 8 ports in 130nm CMOS S. Fukae¹, N. Omori¹, T. Koide¹, H. J. Mattausch¹ and T. Hironaka¹, ¹<i>RCNS, Hiroshima Univ.</i> and ²<i>Hiroshima City Univ., Japan</i></p>
<p>15:30 A-1-5 Direct evaluation of an interfacial layer in high-k gate dielectrics by 1/f noise measurements T. Ishikawa¹, S. Tsujikawa¹, S. Saito¹, D. Hisamoto¹ and S. Kimura¹, ¹<i>Hitachi, Ltd., Japan</i></p>	<p>15:40 B-1-5 A Low Dielectric Constant Sr₂(Ta_{1-x}Nb_x)₂O₇ Thin Film Controlling the Crystal Orientation on IrO₂ Substrate for One Transistor Type Ferroelectric Memory Device I. Takahashi¹, H. Sakurai¹, A. Yamada², T. Goto¹, M. Hirayama¹, A. Teramoto¹, S. Sugawa¹ and T. Ohmi¹, ¹<i>NICHE, Tohoku Univ.</i> and ²<i>Tohoku Univ., Japan</i></p>	<p>15:30 C-1-5 Hafnium Content Dependence of Bottom Interfacial Layer and Its Impact on Hf:Al_{1-x}O₂ High-k nMOSCAPs and nMOSFETs Characteristics Y. Tamura¹, Y. Sugiyama¹, M. Yamaguchi¹, H. Minakata¹, Y. Tanida¹, T. Sakoda¹, M. Nakamura¹ and Y. Nara¹, ¹<i>Fujitsu Labs Ltd., Japan</i></p>	<p>15:20 D-1-5 Measurement of extension structures in deep sub-micron MOSFETs by scanning capacitance microscopy based on frequency modulation control Y. Naitou¹ and N. Ookubo¹, ¹<i>Silicon Systems Research Labs, NEC Corporation, Japan</i></p>	<p>15:15 E-1-5 Demonstration of MEMS-Controlled Electronic States in Single Quantum Dots T. Nakaoka¹, T. Kakitsuka², T. Saito¹ and Y. Arakawa^{2,3}, ¹<i>RCAST, IIS, and CCR, Univ. of Tokyo</i> and ²<i>NTT Photonics Labs, NTT Corporation, Japan</i></p>	<p>15:15 F-1-5 Reduction of Turn-on Voltage in GaInNAs and InGaAs Base Double Heterojunction Bipolar Transistors C.-H. Wu¹, Y.-K. Su¹, S.-C. Wei¹ and S.-J. Chang¹, ¹<i>National Cheng Kung Univ., Taiwan</i></p>	<p>15:30 G-1-5 Combined Data/Instruction Cache with Bank-Based Multi-Port Architecture K. Johguchi¹, Z. Zhu¹, T. Hirakawa², T. Koide¹, T. Hironaka² and H.J. Mattausch¹, ¹<i>Hiroshima Univ. RCNS</i> and ²<i>Hiroshima City Univ., Japan</i></p>
			<p>15:40 D-1-6 Valence-Mended Si(100) for Nanoelectronic Applications M. Tao¹, W. P. Kirk¹, D. Udeshi¹, S. Agarwal¹, E. Maldonado¹ and N. Basit¹, ¹<i>Univ. of Texas at Arlington, USA</i></p>	<p>15:30 E-1-6 Displacement Sensing using Quantum Mechanical Interference H. Yamaguchi¹, S. Miyashita² and Y. Hirayama², ¹<i>NTT Basic Research Labs</i>, ²<i>NTT Advanced Technology</i> and ³<i>CREST-JST, Japan</i></p>	<p>15:30 F-1-6 InP/InGaAs Tunneling Emitter Bipolar Transistor (TEBT) C.-Y. Chen¹, H.-M. Chuang¹, S.-I. Fu¹, P.-H. Lai¹, Y.-Y. Tsai¹, C.-I. Kao¹ and W.-C. Liu¹, ¹<i>National Cheng-Kung Univ., Taiwan</i></p>	
				<p>15:45 E-1-7 ZnO Metal-Insulator-Semiconductor Field-Effect-Transistor J. Nishii¹, A. Ohtomo¹, T. Fukumura¹, K. Ohtani², F. Matsukura², Y. Ohno², H. Ohno² and M. Kawasaki¹, ¹<i>Tohoku Univ.</i> and ²<i>RIEC, Tohoku Univ., Japan</i></p>	<p>15:45 F-1-7 High-Quality Two-Dimensional Electron Gas at Large Scale GaN/AlGaIn Wafer Interface Prepared by Mass Production MOCVD Systems S. Yamada¹, T. Ohnishi¹, T. Kakegawa¹, M. Akabiri¹, T. Suzuki¹, H. Sugiura², F. Nakamura², E. Yamaguchi² and H. Kawai², ¹<i>CNMT, JAIST</i> and ²<i>Powdec K.K., Japan</i></p>	

Break

Break

Room A	Room B	Room C	Room D	Room E	Room F	Room G
A-2: Advanced Silicon Devices and Device Physics -Advanced CMOS Technology I-(16:15-18:15) Chairs: A. Hiroki (Kyoto Inst. of Technol.), S. Inaba (Toshiba)	B-2: Non-Volatile Memory Technologies -Non-Volatile Memory II-(16:15-17:35) Chairs: Y. Shimada (Matsushita Electric), T. Nakamura (Rohm)	C-2: Silicon Process / Materials Technologies -High-k Gate Dielectric II-(16:15-17:55) Chairs: M. Kubota (Matsushita Electric), J. Yugami (Renesas)	D-2: New Materials and Characterization -Low k and Silicicide Characterization-(16:15-18:15) Chairs: K. Kikuta (NEC), S. Zaima (Nagoya Univ.)	E-2: Quantum Nanostructure Devices and Physics -Nanostructured Optical Devices-(16:15-18:00) Chairs: K. Hirakawa (Univ. of Tokyo), L. Samuelson (Lund Univ.)	F-2: Compound Semiconductor Materials and Devices -Nitride Electron Devices-(16:15-18:00) Chairs: T. Kikkawa (Fujitsu Labs.), N. Maeda (NTT)	G-2: Advanced Silicon Circuits and Systems -Collaboration of Circuits and Devices-(16:15-17:45) Chairs: M. Fujishima (Univ. of Tokyo), T. Kuroda (Keio Univ.)
16:15 A-2-1 Enhancement of V_{th} Degradation under NBT Stress due to Hole Capturing Y. Mitani ¹ , M. Nagamine ¹ , H. Satake ¹ and A. Toriumi ² , ¹ Toshiba Corporation and ² The Univ. of Tokyo, Japan	16:15 B-2-1 Novel Capacitor Structure Using Sidewall Spacer for Highly Reliable FRAM Device H.H. Kim ¹ , J.H. Park ¹ , Y.J. Song ¹ , N.W. Jang ¹ , H.J. Joo ¹ , S.K. Kang ¹ , S.H. Joo ¹ , S.Y. Lee ¹ and K. Kim ¹ , ¹ Samsung Electronics Co. Ltd., Korea	16:15 C-2-1 Flatband Voltage Shift Caused by Dopants Diffused from Poly-Si Gate Electrode in Poly-Si/HfSiO ₂ /SiO ₂ /Si A. Kaneko ¹ , S. Inumiya ¹ , K. Sekine ¹ , M. Sato ¹ , Y. Kamimuta ¹ , K. Eguchi ¹ and Y. Tsunashima ¹ , ¹ Toshiba Corporation, Japan	16:15 D-2-1 Nondestructive Characterization of Pore Size Distributions in Porous Low-k Films by in-situ Spectroscopic Ellipsometry in Vapor Cell C. Negoro ¹ , N. Hata ^{1,2} and T. Kikkawa ^{2,3} , ¹ ASRC, AIST, ² MIRAI-ASRC, AIST and ³ RCNS, Hiroshima Univ., Japan	16:15 E-2-1 (Invited) A Light Emitting Diode for Single Photons A.J. Shields ¹ , Z. Yuan ¹ , M.B. Ward ¹ , R.M. Stevenson ¹ , B.E. Kardynal ¹ , P. See ¹ , C. Lobo ² , P. Atkinson ² and D.A. Ritchie ² , ¹ Toshiba Research Europe Ltd., Cambridge Research Lab and ² Cavendish Lab., Univ. of Cambridge, UK	16:15 F-2-1 (Invited) MOVPE Growth of Wurtzite InN and its Characteristics T. Matsuoka ¹ , H. Okamoto ² , M. Nakao ³ , H. Harima ¹ , H. Takahata ⁴ , H. Mitate ⁴ , S. Mizuno ⁴ , Y. Uchiyama ⁴ , T. Makimoto ¹ , ¹ NTT Basic Research Labs., ² NTT Photonics Labs., ³ Kyoto Inst. of Technology, ⁴ NTT Advanced Technology and ⁵ Meiji Univ., Japan	16:15 G-2-1 (Invited) Performance of Deeply-Scaled, Power-Constrained Circuits B. Nikolic ¹ , L. Chang ¹ , T.-J. King ¹ , ¹ Univ. of California, USA
16:35 A-2-2 New Mechanism for Negative-Bias-Temperature Instability and Its Impact on Scaling of pMOSFETs D.-Y. Lee ¹ , H.-C. Lin ² , C.-C. Chen ¹ , C.-H. Chien ¹ , T.-Y. Huang ¹ , T. Wang ¹ , T.-L. Lee ¹ , S.-C. Chen ¹ and M.-S. Liang ¹ , ¹ National Chiao-Tung Univ., ² National Nano Device Labs and ³ Taiwan Semiconductor Manufacturing Company, Taiwan	16:35 B-2-2 High performance PZT capacitor using highly crystalline SRO bottom electrode for Mbit FeRAM devices H. Itokawa ¹ , K. Natori ¹ , S. Yamazaki ¹ , G. Beitel ² and K. Yamakawa ¹ , ¹ Toshiba Corp. and ² Infineon Technologies Japan., Japan	16:35 C-2-2 Controlled Nitrogen Incorporation into HfAlO ₂ by Layer-by-Layer Deposition and Annealing (LL-D&A) Process and Its Impact on Electrical Properties of MOSCAPs and nMOSFETs K. Tominaga ¹ , K. Iwamoto ¹ , H. Hisamatsu ¹ , T. Yasuda ¹ , H. Ota ² , N. Yasuda ¹ , T. Nabatame ¹ and A. Toriumi ^{2,3} , ¹ MIRAI-ASET, ² MIRAI-ASRC, AIST and ³ the Univ. of Tokyo, Japan	16:35 D-2-2 Accurate measurement of mechanical properties of nanoporous silica ultra-low-k films Y. Seino ¹ , R. Ichikawa ² , H. Tanaka ¹ and T. Kikkawa ¹ , ¹ MIRAI Project, ASRC, AIST, ² ASRC, AIST, ³ MIRAI Project, ASET and ⁴ RCNS, Hiroshima Univ., Japan	16:45 E-2-2 Coherent control of exciton in a single quantum dot using a high-resolution Michelson interferometer T. Okada ^{1,2,3} , K. Komori ^{2,3} , K. Goshima ^{2,3} , S. Yamauchi ^{2,3} , T. Sugaya ^{2,3} , O. Yamazaki ³ and T. Hattori ⁴ , ¹ Tokai University Junior College, ² AIST, ³ CREST-JST, Japan and ⁴ Univ. of Tsukuba, Japan	16:45 F-2-2 Extrinsic Base Regrowth of p-InGaN for Npn-type GaN/InGaN Heterojunction Bipolar Transistor T. Makimoto ¹ , K. Kumakura ¹ and N. Kobayashi ¹ , ¹ NTT Basic Research Labs., NTT Corporation and ² The Univ. of Electro-Communications, Japan	16:45 G-2-2 ESD Circuit Simulation Technology Using Protection Device Model with Generated-Hole-Dependent Base Resistance Y. Tosaka ¹ , H. Anzai ¹ , K. Suzuki ¹ and H. Oka ¹ , ¹ Fujitsu Labs Ltd., Japan
16:55 A-2-3 Origin of Enhanced Thermal Noise for 100nm-TMOSFETs S. Hosokawa ¹ , Y. Shiraga ¹ , H. Ueno ¹ , M. Miura-Mattausch ¹ , H. J. Mattausch ¹ , T. Ohguro ² , S. Kumashiro ² , M. Taguchi ² , H. Masuda ² and S. Miyamoto ² , ¹ Hiroshima Univ. and ² STARC, Japan	16:55 B-2-3 A novel chemical solution deposition method suitable for high-yield fabrication of 50 nm-thick SrBi ₂ Ta ₂ O ₇ capacitors Y. Kawashima ¹ and H. Ishiwara ¹ , ¹ Tokyo Inst. of Technology, Japan	16:55 C-2-3 Suppression of Silicidation in Poly-Si/ZrO ₂ /SiO ₂ /Si Structure by Helium Through Process K. Muraoka ¹ , ¹ Advanced LSI Technology Lab, Toshiba Corporation, Japan	16:55 D-2-3 Mechanical Property and Skeletal Silicate Structure of Periodic Porous Silica Films S. Takada ¹ , N. Hata ^{1,2} , Y. Seino ^{1,2} , K. Yamada ¹ , Y. Oku ¹ and T. Kikkawa ^{2,3} , ¹ ASRC, AIST, ² MIRAI-ASRC, AIST, ³ MIRAI-ASET and ⁴ RCNS, Hiroshima Univ., Japan	17:00 E-2-3 Voltage-controlled Emission Wavelength Switching in a Pseudomorphic Si _{1-x} Ge _x /Si Double Quantum Well N. Yasuhara ¹ and S. Fukatsu ^{1,2} , ¹ The Univ. of Tokyo and ² PRESTO-JST, Japan	17:00 F-2-3 Improvement of DC and RF characteristics of AlGaIn/GaN HEMTs by thermally annealed Ni/Pt/Au Schottky gate T. Nanjo ¹ , N. Miura ¹ , T. Oishi ¹ , M. Suita ¹ , Y. Abe ¹ , T. Ozeki ¹ , S. Nakatsuka ¹ , A. Inoue ¹ , T. Ishikawa ¹ and Y. Matsuda ¹ , H. Ishikawa ² and T. Egawa ² , ¹ Mitsubishi Electric Corporation and ² Nagoya Inst. of Technology, Japan	17:05 G-2-3 A New Protection Circuit of IGBT (Insulated Gate Bipolar Transistor) for Short-Circuit Withstanding Capability B.-C. Jeon ¹ , I.-H. Ji ¹ , M.-K. Han ¹ and Y.-I. Choi ² , ¹ Seoul National Univ. and ² Ajou Univ., Korea
17:15 A-2-4 Comparison of the Interconnect Capacitances for Various SRAM Cell Layouts To Achieve High Speed, Low Power SRAM Cells Y. Tsukamoto ¹ , K. Nii ¹ , Y. Yamagami ² , T. Yoshizawa ¹ , S. Imaoka ¹ , T. Suzuki ¹ , A. Shibayama ¹ and H. Makino ¹ , ¹ Renesas Technology Corporation, ² Matsushita Electric Industrial Corporation and ³ Renesas Device Design Corporation, Japan	17:15 B-2-4 Two-Mode Behavior in Time and Temperature Dependence of Imprint-Induced Charge Loss in Integrated SrBi ₂ (Ta,Nb):O ₇ Capacitors A. Noma ¹ , T. Mikawa ¹ , Y. Nagano ¹ , Y. Judai ¹ and E. Fujii ¹ , ¹ Matsushita Electric Industrial Co., Ltd., Japan	17:15 C-2-4 Reliability characteristics of an HfO ₂ /SiO ₂ stack gate dielectric annealed in a deuterium ambient H. Park ¹ , H. Yang ¹ , H. Sim ¹ and H. Hwang ¹ , ¹ Kwangju Inst. of Science and Technology, Korea	17:15 D-2-4 Determination of the Mechanical Properties of Thin Periodic Porous Silica Films by Laser-Generated Surface Acoustic Wave Technique X. Xiao ¹ , N. Hata ¹ , K. Yamada ¹ , H. Tanaka ¹ and T. Kikkawa ² , ¹ ASRC, AIST, ² MIRAI-ASRC, AIST, ³ MIRAI-ASET and ⁴ RCNS, Hiroshima Univ., Japan	17:15 E-2-4 A Solid-State Multicolor Light-Emitting Device Based on Ballistic Electron Excitations Y. Nakajima ¹ , T. Uchida ¹ , A. Kojima ¹ , B. Gelloz ¹ and N. Koshida ¹ , ¹ Tokyo Univ. of Agri. & Tech., Japan	17:15 F-2-4 The improvement of DC performance in AlGaIn/GaN HFET with isoelectronic Al doped channel C.M. Jeon ¹ , J.-H. Lee ² , J.-H. Lee ² and J.-L. Lee ¹ , ¹ POSTECH, and ² Kyungpook National Univ., Korea	17:25 G-2-4 Dynamic Holding Voltage SCR (DHVSCR) Device for ESD Protection with high Latch-up Immunity Z.-P. Chen ¹ and M.-D. Ker ¹ , ¹ Industrial Technology Research Inst., Hsinchu, and ² Inst. of Electronics, National Chiao-Tung Univ., Taiwan

Room A	Room B	Room C
<p>17:35 A-2-5 Eliminating Threshold Voltage Offset of PMOSFETs in High-Density DRAM N. Takaura¹, R. Takemura¹, H. Matsuoka¹, R. Nagai², S. Yamada², H. Asakura¹ and S. Kimura¹, ¹Hitachi, Ltd. and ²Elpida Memory Inc., Japan</p> <p>17:55 A-2-6 Gate Engineering to prevent NMOS Dopant Channeling for Nano-Scale CMOSFET Technology S.-H. Park¹ and H.-D. Lee², ¹Hynix Semiconductor Inc. and ²Chuggiak National Univ., Korea</p>		<p>17:35 C-2-5 Enhancement of dielectric constant due to expansion of lattice spacing in CeO₂ directly grown on Si (111) D. Matsushita¹, Y. Nishikawa¹, N. Satou², M. Yoshiki², T. Shimizu¹, T. Yamaguchi¹, H. Satake¹ and N. Fukushima¹, ¹Toshiba Corporation and ²Toshiba Nanoanalysis Corporation, Japan</p>

18:30-20:30 Banquet (Eminence Hall)

Room D	Room E	Room F	Room G
<p>17:35 D-2-5 HRTEM and EELS Analyses of Interfacial Nanostructures in Ti/Si_{1-x}Ge_x/Si(100) J. Yamasaki¹, N. Tanaka¹, O. Nakatsuka¹, A. Sakai², S. Zaima² and Y. Yasuda², ¹CIRSE, Nagoya Univ., ²Nagoya Univ. and ³CCRAST, Nagoya Univ., Japan</p> <p>17:55 D-2-6 Impact of NiSi Thermal Instability on Junction Shallowing Characterized with Damage-free n+/p Silicon Diodes M. Tsuchiaki¹, K. Ohuchi¹ and C. Hongo¹, ¹Toshiba Corporation, Japan</p>	<p>17:30 E-2-5 High Brightness Si-based Quantum Dot Light Emitting Diode M. Jo¹, N. Yasuhara¹, K. Kawamoto¹ and S. Fukatsu^{1,2}, ¹The Univ. of Tokyo and ²PRESTO, JST, Japan</p> <p>17:45 E-2-6 Generation of Radiation Pressure in Thermally Induced Ultrasonic Emitter Based on Nanocrystalline Silicon J. Hirota¹, H. Shinoda² and N. Koshida¹, ¹Tokyo Univ. of A & T and ²Univ. of Tokyo, Japan</p>	<p>17:30 F-2-5 Drain Current DLTS of AlGaIn/GaN MIS-HEMTs T. Okino¹, M. Ochiai¹, Y. Ohno¹, S. Kisimoto¹, K. Maezawa¹ and T. Mizutani¹, ¹Nagoya Univ., Japan</p> <p>17:45 F-2-6 Low damage, high selectivity Ar/Cl₂/CH₄/O₂ gate recess etching for AlGaIn/GaN HEMT fabrication W.-K. Wang¹, Y.-J. Li¹, C.-K. Lin¹, Y.-J. Chan¹, G.-T. Chen¹ and J.-I. Chyi¹, ¹National Central Univ., Taiwan</p>	

18:30-20:30 Banquet (Eminence Hall)

Wednesday, September 17

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>A-3: Advanced Silicon Devices and Device Physics -High-k Technology I- (9:00-10:30) Chairs: M. Ogawa (Kobe Univ.) T. Mogami (NEC)</p>	<p>B-3: Non-Volatile Memory Technologies -Non-Volatile Memory III- (9:00-10:20) Chairs: K. Takasaki (Fujitsu Labs.) H. Takada (Mitsubishi Electric)</p>	<p>C-3: Silicon Process / Materials Technologies -Memory Technology- (9:00-10:30) Chairs: T. Kobayashi (Sony) I. Asano (Elpida)</p>	<p>D-3: Silicon-on-Insulator Technologies -SOI Novel Devices- (9:00-10:30) Chairs: A. Ogura (NEC) T. Nakai (SUMCO)</p>	<p>E-3:Quantum Nanostructure Devices and Physics -Characterization and Nanoprobng- (9:00-10:15) Chairs: H. Akinaga (AIST) M. Sugawara (Univ. of Tokyo)</p>	<p>F-3:Compound Semiconductor Materials and Devices -Novel Compound Semiconductors Devices- (9:00-10:15) Chairs: K. Akimoto (Tsukuba Univ.) N. Kobayashi (The Univ. of Electro-Communications)</p>	<p>G-3:Advanced Silicon Circuits and Systems -Circuit Techniques for Emerging Technologies- (9:00-10:30) Chairs: K. Kotani (Tohoku Univ.) M. Takamiya (NEC)</p>
<p>9:00 A-3-1 (Invited) Integration Issues of HfO₂-Al₂O₃ Laminate for Gate and Capacitor Dielectric J.-H. Lee¹, ¹Samsung Electronics Co., Ltd., Korea</p>	<p>9:00 B-3-1 (Invited) Floating gate type nonvolatile memory reliability issues G. Tempel¹, ¹Infineon Technologies, Germany</p>	<p>9:00 C-3-1 (Invited) 0.18 μm Embedded FRAM Fabrication Process and its Consistency with Conventional Logic LSI Process Y. Horii and T. Eshita¹, ¹Fujitsu Limited, Japan</p>	<p>9:00 D-3-1 (Invited) Strained Si MOSFETs on SiGe-on-Insulator (SGOI) for High Performance CMOS Technology K. Rim¹, B.H. Lee¹, A. Mocuta¹, K. Jenkins¹, S. Bedell¹, H. Chen¹, D. Sadana¹, M. Gribelyuk¹, J. Ott¹, K. Chan¹, L. Shi¹, J. Chu¹, D. Boyd¹, P. Mooney¹, P. O'Neil¹, E. Leobandung¹, and J.J. Welsler¹, ¹SRDC, IBM, USA</p>	<p>9:00 E-3-1 Optical characteristics of InAs/GaAs double quantum dots grown by MBE with Indium-Flush method S. Yamauchi^{1,2}, K. Komori^{1,2}, T. Sugaya^{1,2} and K. Goshima^{1,2}, ¹AIST and ²CREST-JST, Japan</p>	<p>9:00 F-3-1 (Invited) Optical and Electrical Control of Ferromagnetism in II-VI Quantum Wells T. Dietl¹, ¹Inst. of Physics, Polish Academy of Science, Poland</p>	<p>9:00 G-3-1 (Invited) The challenge of analog mix-mode integrated circuit design for brain computer interface Z. Wang¹, C. Zhang¹, and D. Li¹, ¹Tsinghua Univ., P.R. China</p>
<p>9:30 A-3-2 Influence of Carrier Velocity Related Parameters on the Propagation Delay Time of CMOS Inverters with High-k Gate Dielectrics M. Ono¹ and A.Nishiyama¹, ¹Toshiba Corporation, Japan</p>	<p>9:30 B-3-2 (Invited) The Prospect of New Emerging Memories H. Jeong¹ and K. Kim¹, ¹Samsung Electronics, Korea</p>	<p>9:30 C-3-2 W-Polymer Gate with Low W/Poly-Si Interface Resistance for High-Speed/High-Density Embedded Memory T. Yamashita¹, Y. Nishida¹, K. Hayashi¹, T. Eimori¹, M. Inuishi¹ and Y. Ohji¹, ¹Renesas Technology Corp., Japan</p>	<p>9:30 D-3-2 Fabrication of Ultra-Thin Strained Ge-on-Insulator Substrate by Ge-Condensation Technique S. Nakaharai¹, T. Tezuka¹, N. Sugiyama¹, Y. Moriyama¹ and S. Takagi¹, ¹MIRAI ASET, Japan</p>	<p>9:15 E-3-2 Molecular States of Coupled Zero-Dimensional Structures Imaged Using Low-Temperature Scanning Tunneling Spectroscopy K. Kanisawa¹, S. Perraud^{1,2}, H. Yamaguchi¹ and Y. Hirayama^{1,3}, ¹NTT Basic Research Labs, ²ESPCI and ³CREST-JST, Japan</p>	<p>9:30 F-3-2 (Invited) Type-II InAs-based Quantum Cascade Lasers K. Ohtani¹ and H. Ohno¹, ¹RIEC, Tohoku Univ., Japan</p>	<p>9:30 G-3-2 The Vision Chip with Electrical Fovea Motion Y. Nakagawa¹, J. Deguchi¹, J.-C. Shim¹, H. Kurino¹ and M. Koyanagi¹, ¹Tohoku Univ., Japan</p>
<p>9:50 A-3-3 A HfAlO_x Gate Dielectric FET Technology Compatible with a Conventional Poly-Si Gate CMOS Process H. Ohji¹, A. Mutoh¹, K. Torii¹, R. Mitsuhashi¹, A. Horiuchi¹, T. Maeda¹, H. Itoh¹, T. Kawahara¹, K. Hayashi¹, T. Sasaki¹, N. Kasai¹, H. Kitajima¹, M. Yasuhira¹, and T. Arikado¹, ¹SELETE, Japan</p>	<p>10:00 B-3-3 Proposal of New Non-Volatile Memory with Magnetic Nano-Dots T. Sakaguchi¹, M. Kobayashi¹, M. Takata², H. Choi¹, Y.G. Hong¹, J.-C. Shim¹, H. Kurino¹ and M. Koyanagi¹, ¹Tohoku Univ. and ²Asahi Glass Co.</p>	<p>9:50 C-3-3 Silicon Selective Epitaxial Growth for Self-Aligned Cell Contact Featuring High Performance Sub-100nm DRAM Cell Transistors T. Kim¹, Y.P. Kim¹, B.C. Lee¹, S. Choi¹, U.I. Chung¹ and J.T. Moon¹, ¹Samsung Electronics, Korea</p>	<p>9:50 D-3-3 Impact Ionization in Uniaxially Strained-Si MOSFET N. Watanabe¹, Y. Maeda¹, M. Nishisaka¹ and T. Asano¹, ¹CMS, Kyushu Inst. of Technology, Japan</p>	<p>9:30 E-3-3 Electronic Charged States of Single Si Quantum Dots with Ge Core as Detected by AFM/Kelvin Probe Technique Y. Darma¹, K. Takeuchi¹ and S. Miyazaki¹, ¹Hiroshima Univ., Japan</p>	<p>10:00 F-3-3 Fabrication of GaN/Alumina/GaN Structure to Reduce Dislocations in GaN M. Hiroki¹, K. Kumakura¹, T. Makimoto¹, N. Kobayashi¹ and T. Kobayashi¹, ¹NTT Corporation and ²Univ. of Electro Communications, Japan</p>	<p>9:50 G-3-3 A Periodic Comparator Operating at 80GHz Based on Single-Flux-Quantum Technology with High Temperature Superconductor H. Sugiyama^{1,2}, H. Wakana¹, S. Adachi¹, Y. Tarutani¹ and K. Tanabe², ¹Toshiba Corporation and ²Superconductivity Research Lab, Japan</p>
<p>10:10 A-3-4 A Novel Approach for Determination of Tunneling Mass, m_{eff}-Conduction Band Offset Energy, E_b Products for Advanced Gate Dielectrics C.L. Hinkle¹, C. Fulton¹, R.J. Nemanich¹ and G. Lucovsky¹, ¹North Carolina State Univ., USA</p>		<p>10:10 C-3-4 Optimum TiSi₂ Ohmic Contact Process for Sub-100nm Devices H.S. Park¹, J.M. Lee¹, S.W. Lee¹, J.H. Park¹, K.J. Moon¹, S.B. Kang¹, G.H. Choi¹, U.I. Chung¹ and J.T. Moon¹, ¹Samsung Electronics, Korea</p>	<p>10:10 D-3-4 Quantum Confinement Effect of Ultrathin-SOI on double-gate-nMOSFETs H. Watanabe¹, K. Uchida¹ and A. Kinoshita¹, ¹Toshiba Corp., Japan</p>	<p>9:45 E-3-4 Magneto-luminescence of Interdiffused Self-Assembled Quantum Dots S. Awirothananon^{1,2}, W. Sheng¹, A. Babinski³, S. Studenikin¹, S. Raymond¹, P. Hawrylak¹, A. Sachrajda¹, M. Potemski¹, G. Ortner³ and M. Bayer³, ¹National Research Council of Canada, ²The Univ. of Ottawa, Canada, ³MPI/FKF and CNRS, France and ⁴Universitat Dortmund, Germany</p>		
Break			Break			Break

Room A	Room B	Room C	Room D	Room E	Room F	Room G
					<p>10:00 E-3-5 Optical Time-of-Flight Study of Lateral Exciton Transport in a Strained Si_{1-x}Ge_x/Si Multiple Quantum Well K. Sawada¹, N. Yasuhara¹ and S. Fukatsu^{1,2}, ¹The Univ. of Tokyo, Graduate School of Arts and Sciences and ²PRESTO, JST, Japan</p>	
Break						
<p>A-4: Optoelectronic Devices and Photonic Crystal Devices -VCSELs and Visible Lasers- (10:45-12:00) Chairs: T. Matsuo (NTT) L.A. Coldren (Agility Communications)</p>	<p>B-4: Non-Volatile Memory Technologies -Non-Volatile Memory IV- (10:45-12:05) Chairs: K. Yoshikawa (Toshiba) T. Kobayashi (Hitachi)</p>	<p>C-4: Silicon Process / Materials Technologies -DRAM- (10:45-12:05) Chairs: M. Okuyama (Osaka Univ.) K. Hieda (Toshiba)</p>	<p>D-4: Silicon-on-Insulator Technologies -SOI Device Physics- (10:45-12:05) Chairs: O. Nishio (Sharp) T.-J. King (UCB)</p>	<p>E-4: Quantum Nanostructure Devices and Physics -Spin-related Phenomena- (10:45-12:15) Chairs: A. Takeuchi (Waseda Univ.) T. Dietl (Polish Academy of Science)</p>	<p>F-4: Compound Semiconductor Materials and Devices -Optical Devices- (10:45-12:15) Chair: T. Matsuoka (NTT) M. Ikeda (Sony)</p>	<p>G-4: System-Level Integration and Packaging Technologies -System-Level Integration and Packaging Technologies I- (10:45-11:45) Chairs: K. Fujimoto (Osaka Univ.) M. Kada (Sharp)</p>
<p>10:45 A-4-1 (Invited) 1300nm-Range GaInNAsSb VCSELs A. Kasukawa¹, H. Shimizu¹, C. Setiagung¹, M. Ariga¹, Y. Ikenaga¹, K. Kumada¹, T. Hama and N. Iwai¹, ¹The Furukawa Electric Co., Ltd., Yokohama R&D Labs, Japan</p>	<p>10:45 B-4-1 A 0.18-μm Embedded MNOS-Type Non-volatile Memory for High-Frequency and Low-Voltage Operation N. Matsuzaki¹, T. Ishimaru¹, Y. Okuyama¹, T. Mine¹, H. Kume¹, T. Hashimoto², Y. Kanamaru², T. Sakai², Y. Kawashima² and F. Ito², ¹Hitachi, Ltd. and ²Renesas Technology Corp., Japan</p>	<p>10:45 C-4-1 Pt/BST/Pt Capacitor Technology for 0.15μm Embedded DRAM Y. Tsunenimine¹, T. Okudaira¹, K. Kashiwara¹, A. Yutani¹, H. Shinkawata¹, M. K. Mazumder¹, M. Yoneda¹, Y. Okuno², A. Tsuzumitani² and Y. Mori², ¹Mitsubishi Electric Corp. and ²Matsushita Electronics Corp., Japan</p>	<p>10:45 D-4-1 Variable Body Effect Factor FD SOI MOSFET for Ultra-Low Power VTCMOS Applications T. Ohtou¹, T. Nagumo¹ and T. Hiramoto¹, ¹Univ. of Tokyo, Japan</p>	<p>10:45 E-4-1 (Invited) Control of ferromagnetic order in selectively p-doped GaMnAs-based heterostructures M. Tanaka^{1,2}, and A. M. Nazmul^{1,2}, ¹Univ. of Tokyo, Department of Electronic Engineering, ²PRESTO-JST, Japan</p>	<p>10:45 F-4-1 (Invited) Developments of High Efficiency In GaN-Based Light-Emitting Diodes J.-I. Chyi¹, C.-C. Pan¹, C.-M. Lee¹, W.-J. Hsu¹, and C.-S. Fang¹, ¹National Central Univ., Taiwan</p>	<p>10:45 G-4-1 (Invited) 3D System Integration by Chip-to-Wafer Stacking Technologies P. Ramm¹, A. Klumpp¹, R. Merkel¹, J. Weber¹, R. Wieland¹, G. Elst² ¹Fraunhofer Inst., Germany</p>
<p>11:15 A-4-2 Improvement of High-Speed Oxide-Confined Vertical-Cavity Surface-Emitting Lasers H.-C. Yu^{1,2}, S.-J. Chang¹, Y.-K. Su¹, C.-P. Sung¹, H.-P. Yang¹, C.-Y. Huang³, Y.-W. Lin², J.-M. Wang², F.-I. Lai¹ and H.-C. Kuo⁴, ¹National Cheng Kung Univ., ²Industrial Technology Research Inst., ³National Tsing Hua Univ. and ⁴National Chiao Tung Univ., Taiwan</p>	<p>11:05 B-4-2 70 nm SONOS Nonvolatile Memory Devices using FN Programming and Hot Hole Erase Method S.D. Chae¹, C.J. Lee², J.H. Kim¹, S.K. Sung¹, J.S. Sim², M.K. Kim¹, S.W. Yoon¹, B.-G. Park², J.W. Lee and C.W. Kim¹, ¹Samsung and ²Seoul National Univ., Korea</p>	<p>11:05 C-4-2 Low Resistive Contacts of TiN-Barrier and Ru-Electrode Using PCM Sputtering for MIM-Ta₂O₅ Capacitors in Giga-Bit DRAMs Y. Nakamura¹, T. Kawagoe¹, H. Sakuma¹, H. Yamaguchi¹, I. Asano¹, M. Horikawa¹, K. Kuroki¹, K. Tanaka¹, Y. Ueda¹ and H. Goto¹, ¹Elpida Memory, Inc., Japan</p>	<p>11:05 D-4-2 Novel SOI MOSFET with Buried Back-Gate H. Oh¹, H. Choi¹, T. Sakaguchi¹, J. C. Shim¹, H. Kurino¹ and M. Koyanagi¹, ¹Tohoku Univ., Japan</p>	<p>11:15 E-4-2 Effect of Internal Exchange Coupling on the Curie Temperature in Ga_{1-x}Mn_xAs Trilayer Structures S. Yuldashev¹, Y. Kim¹, N. Kim¹, H. Im¹, T. W. Kang¹, S. Lee², Y. Sasaki³, X. Liu¹ and J. Furdyna³, ¹Dongguk Univ., Korea, ²Korea Univ., Korea and ³Univ. of Notre Dame, USA</p>	<p>11:15 F-4-2 InGaN-based horizontal cavity surface emitting laser diode with selectively grown cavity and outer micromirrors T. Akasaka¹, T. Nishida¹, T. Makimoto¹ and N. Kobayashi¹, ¹NTT Basic Research Labs, NTT Corporation, Japan</p>	<p>11:15 G-4-2 Micro Cu Bump Interconnection on 3D Chip Stacking Technology K. Tanida¹, M. Memoto¹, N. Tanaka¹, Y. Tomita¹ and K. Takahashi¹, ¹ASET, Japan</p>
<p>11:30 A-4-3 High-Power 200-mW 660-nm AlGaInP Laser Diodes with a Low Operating Current R. Hiroshima¹, D. Inoue¹, S. Kameyama¹, A. Tajiri¹, M. Shono¹, M. Sawada² and A. Ibaraki¹, ¹Sanyo electric Co., Ltd. and ²Tottori Sanyo electric Co., Ltd., Japan</p>	<p>11:25 B-4-3 Excellent Electrical Characteristics of SONOS-type Flash Memory with High-k; Dielectric as Trapping Layer and Blocking Layer M. Cho¹, S. Choi¹, H. Hwang¹ and J.W. Kim², ¹Kwangju Inst. of Science and Technology and ²Samsung Advanced Inst. of Technology, Korea</p>	<p>11:25 C-4-3 A Noble SiON/AIO Structure at High-k/poly-Si Interface for Storage Capacitors of High Density DRAMs O. Tononuma¹ and H. Miki¹, ¹Hitachi, Ltd., Japan</p>	<p>11:25 D-4-3 Modeling of Fully-depleted SOI Device Variation H. Komatsubara¹, K. Kishiro¹, Y. Kawai², N. Miura¹ and K. Fukuda¹, ¹Oki Electric Industry Co., Ltd. and ²Miyagi Oki Electric Industry Co., Ltd., Japan</p>	<p>11:30 E-4-3 Magnetic Properties of Submicron-sized p-In_{0.97}Mn_{0.03}As Ferromagnetic Semiconductor Y. Sekine¹, J. Nitta^{1,2}, T. Koga^{1,3}, A. Oiwa^{3,4}, S. Yanagi¹, T. Slupinski³ and H. Munekata¹, ¹NTT-CREST ²PRESTO-JST ³Tokyo Inst. of Technology, Japan and ⁴Warsaw University, Poland</p>	<p>11:30 F-4-3 Sub-mW Operation of 308 nm Deep UV LED using quaternary InAlGaIn H. Hirayama¹ and Y. Aoyagi², ¹RIKEN and ²Tokyo Inst. of Technology, Japan</p>	<p>11:30 G-4-3 Copper Electrodeposition of High-Aspect-Ratio Vias for Three Dimensional Packaging K. Kondo¹, T. Yonezawa¹, M. Tomisaka², H. Yonemura², M. Hoshino², Y. Taguchi² and K. Takahashi², ¹Okayama Univ. and ²ASET, Japan</p>

Room A	Room B	Room C
11:45 A-4-4 High power and high temperature operation of 660 nm AlGaInP laser diodes for DVD-R/RW Y. Yoshida, H. Nishiguchi, M. Sasaki, S. Abe, A. Ohno, K. Ono, M. Takemi, J. Horie, T. Yagi and E. Omura, ¹ Mitsubishi Electric Corporation, Japan	11:45 B-4-4 Data retention improvement of MONOS memories by using silicon-tetrachloride-based silicon nitride with ultra-low Si-H bond density K. Nomoto ¹ , G. Asayama ¹ and T. Kobayashi ¹ , ¹ Sony Corporation, Japan	11:45 C-4-4 A Highly Reliable TiN/Al ₂ O ₃ /TiN MIM Technology for Embedded DRAMs L.-L. Chao ¹ , C.D. Wu ¹ , H.L. Lin ¹ , Y.L. Tu ¹ , K.Y. Lin ¹ , C.Y. Yu ¹ , C.Y. Chen ¹ , F.J. Shiu ¹ , C.T. Ho ¹ , C.S. Tsai ¹ , S.-G. Wu ¹ and C. Wang ¹ , ¹ Taiwan Semiconductor Manufacturing Company, Ltd, Taiwan

Lunch

13:00-15:00 Poster Session (Ohgi)

Room D	Room E	Room F	Room G
11:45 D-4-4 Temperature Dependence of Threshold Voltage and Hot Carrier Degradation of Dynamic Threshold SOI-pMOSFET Y.-J. Lee ¹ , T.-S. Chao ^{1,2} , C.-Y. Huang ¹ , H.-C. Lin ² and T.-Y. Huang ¹ , ¹ National Chiao Tung Univ., Taiwan and ² National Nano Device Labs., Taiwan	11:45 E-4-4 Analysis and Control of Rashba Spin-Splitting in One-Dimensional Conductors at Narrow-Gap Single Heterojunctions T. Kakegawa ¹ , T. Kita ² , T. Sato ¹ , M. Akabori ¹ and S. Yamada ¹ , ¹ CNMT, JAIST and ² RIEC, Tohoku Univ., Japan	11:45 F-4-4 Low Temperature p-GaN rough layer on In _{0.25} Ga _{0.75} N/GaN MQW LEDs L.W. Wu ¹ , S.J. Chang ¹ , Y.K. Su ¹ , W.C. Lai ^{1,2} and J.K. Sheu ¹ , ¹ National Cheng Kung Univ., ² South Epitaxy Corporation and ³ National Central Univ., Taiwan	

12:00 E-4-5
 Au/GaAs magnetoresistive-switch-effect devices fabricated by wet etching
 Z.G. Sun¹, M. Mizuguchi¹ and H. Akinaga¹, ¹SYNAF, AIST, Japan

12:00 F-4-5
 Improvement of AlGaInP MQW Light Emitting Diodes by Modification of Ohmic Contact Layer
 H.-C. Wang¹, Y.-K. Su¹, C.-L. Lin¹, S.-M. Chen² and W.-L. Li², ¹Inst. of Microelectronics and Department of Electrical Engineering and ²Epitech Technology Corporation, Taiwan

Lunch

13:00-15:00 Poster Session (Ohgi)

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>A-5: Optoelectronic Devices and Photonic Crystal Devices and Photonic Crystal Devices -Optoelectronic Integrated Devices- (15:15-16:45) Chairs: T. Nishimura (Mitsubishi Electric) S. Lee (KIST)</p>	<p>B-5: Organic Semiconductor Devices and Materials -Preparation and Characterization- (15:15-16:30) Chairs: F. Kaneko (Niigata Univ.) O. Sugihara (Tohoku Univ.)</p>	<p>C-5: Silicon Process / Materials Technologies -Interconnect- (15:15-16:45) Chairs: N. Kobayashi (Selete) T. Nakamura (Fujitsu Labs.)</p>	<p>D-5: Silicon-on-Insulator Technologies -Fin FET Technologies- (15:15-16:45) Chairs: H. Matsuhashi (Oki Electric) K. Rim (IBM)</p>	<p>E-5: Quantum Nanostructure Devices and Physics -Single Electron Transport- (15:15-16:30) Chairs: Y. Ohno (Tohoku Univ.) A. Shields (Toshiba Cambridge)</p>	<p>F-5: Micro-Nano Electromechanical Devices for Bio- and Chemical Applications -Micro-Nano Electro Mechanical Devices for Bio- and Chemical Applications - I- (15:15-16:45) Chair: Y. Miyahara (NIMS) M. Kamahori (Hitachi)</p>	<p>G-5: System-Level Integration and Packaging Technologies -System-Level Integration and Packaging Technologies II- (15:15-16:45) Chairs: K. Takahashi (ASET.) M. Kimura (Mitsubishi Electric)</p>
<p>15:15 A-5-1 (Invited) Monolithic PD-EAM Optical Gates for Ultrafast Signal Processing S. Kodama¹, T. Yoshimatsu¹ and H. Ito¹, ¹NTT Corporation, Japan</p>	<p>15:15 B-5-1 Controlling the Morphology of Nanostructured Poly(floureneethynylene) Film by a Simple Method K. Tada¹ and M. Onoda¹, ¹Himeji Inst. of Technol, Japan</p>	<p>15:15 C-5-1 (Invited) Stress Migration Phenomena of Cu Interconnects T. Oshima¹, K. Ishikawa¹, T. Saito¹, H. Aoki¹ and K. Hinode¹, ¹Hitachi, Ltd., Japan</p>	<p>15:15 D-5-1 (Invited) FinFET Promise and Challenges T.-J. King¹, ¹Univ. of California, USA</p>	<p>15:15 E-5-1 (Invited) Nuclear spin dependent transport in quantum dots K. Ono¹, and S. Tarucha^{1,2,3}, ¹Univ. of Tokyo, ²NTT Basic Research Labs, ³ERATO-JST, Japan</p>	<p>15:15 F-5-1 (Invited) DNA Chips and Their Medical Applications P. Fortina¹, L.J. Kricka², and S. Surrey¹, ¹Thomas Jefferson Univ., USA ²Hospital of the Univ. of Pennsylvania</p>	<p>15:15 G-5-1 (Invited) Design, Manufacturing and Infrastructure for All-in-One SiP Solution T. Fujitsu¹, ¹J-SiP Walton, Japan</p>
<p>15:45 A-5-2 InP-based OEIC Photoreceivers Using Shared Layer Integration Technology of Heterojunction Bipolar Transistors and Refracting-Facet Photodiodes B. Lee¹, Y. Song¹ and K. Yang¹, ¹KAIST, Korea</p>	<p>15:30 B-5-2 Anomalous Growth Temperature Dependence of the Surface Roughness of Pentacene Thin Films M. Tejima¹, T. Komoda¹, K. Kita¹, K. Kyuno¹ and A. Toriumi¹, ¹The Univ. of Tokyo, Japan</p>	<p>15:45 C-5-2 Mechanical property control of Low-k Dielectrics for Diminishing CMP-related Defects in Cu-damascene Interconnects K. Hijioka¹, F. Ito¹, M. Tagami¹, H. Ohtake¹, T. Takeuchi¹, S. Saitoh¹ and Y. Hayashi¹, ¹NEC Corporation, Japan</p>	<p>15:45 D-5-2 High-Aspect Ratio Gate Formation of Beam-Channel MOS Transistor with Impurity-Enhanced Oxidation of Silicon Gate A. Katakami¹, K. Kobayashi² and H. Sunami², ¹Fujitsu Labs Limited and ²Hiroshima Univ., Japan</p>	<p>15:45 E-5-2 Single Electron Transport through Single InAs Quantum Dots Probed by Nanogap Electrodes M. Jung¹ and K. Hirakawa^{1,2}, ¹Univ. of Tokyo and ²CREST-JST, Japan</p>	<p>15:45 F-5-2 Bioluminometry by CMOS-based active pixel photodiode array with accurate background noise compensation Y. Yazawa¹, M. Kamahori¹ and H. Kambara¹, ¹Hitachi, Ltd., Japan</p>	<p>15:45 G-5-2 (Invited) System Packaging and Embedded WLP Technologies for Mobile Products T. Wakabayashi¹, ¹Casio, Japan</p>
<p>16:00 A-5-3 Solid-State Optical Routing Device Utilizing Minority Carrier Drift H. Tsukamoto¹, T.D. Boone¹ and J.M. Woodall¹, ¹Yale Univ., USA</p>	<p>15:45 B-5-3 Fabrication and Photoelectrochemical Properties of Polythiophene-Porphyrin Composite Films T. Akiyama¹, K. Kakutani¹ and S. Yamada¹, ¹Kyushu Univ., Japan</p>	<p>16:05 C-5-3 The Delamination Mechanism of Porous Low-k Film during the Cu-CMP Process S. Kondo¹, T. Nasuno¹, S. Ogawa¹, S. Tokitou¹, B. U. Yoon¹, A. Namiki², Y. Sone², K. Misawa¹, T. Yoshie¹, K. Yoneda¹, M. Shimada¹, S. Sone¹, H.J. Shin¹, N. Ohashi¹, I. Matsumoto¹ and N. Kobayashi¹, ¹SELETE and ²Novellus Systems Japan, Inc., Japan</p>	<p>16:05 D-5-3 An Experimental Study of The Cross-Sectional Channel Shape Dependence of Short-Channel Effects in Fin-Type Double-Gate MOSFETs Y. Liu¹, K. Ishii¹, M. Masahara¹, T. Tsutsumi¹, H. Takashima¹ and E. Suzuki¹, ¹AIST and ²Meiji Univ., Japan</p>	<p>16:00 E-5-3 Investigation of Electron Transition Energy for Vertically Coupled InAs/GaAs Semiconductor Quantum Dots and Rings Y. Li^{1,2} and H.-M. Lu¹, ¹National Nano Device Labs, ²National Chiao Tung University and ³Univ. of Illinois at Chicago, USA</p>	<p>16:00 F-5-3 Detection of DNA Molecules Using Insulated Gate Field Effect Transistor and Intercalator T. Sakata¹, H. Otsuka¹ and Y. Miyahara¹, ¹Biomaterials Research Center, National Inst. for Materials Science, Japan</p>	<p>16:15 G-5-3 Evaluation of Hot-Carrier Hardness and Thick-Film Formation with STP Technique for Seamless Integration Technology N. Sato¹, N. Shimoyama¹, T. Kamei¹, K. Kudou², M. Yano², H. Ishii² and K. Machida¹, ¹NTT Corporation and ²NTT Advanced Technology Corporation, Japan</p>
<p>16:15 A-5-4 Analysis of AlGaAs/GaAs Heterojunction Photodetector with a Two-Dimensional Channel Modulated by Gate Voltage H. Song and H. Kim, ¹Korea Electronics Technology Inst., Korea</p>	<p>16:00 B-5-4 High Resolution Pattern Recording on Photosensitive Urethane-Urea Copolymer Film Surface by Laser Irradiation through Photo-mask Y. Che¹, O. Sugihara¹, N. Okamoto¹, M. Tomiki¹, M. Tsuchimori² and O. Watanabe², ¹Shizuoka Univ. and ²Toyota Central Research and Development Labs Inc., Japan</p>	<p>16:25 C-5-4 In-situ Measurement of Friction Force during Cu Chemical Mechanical Polishing H. Matsuo¹, A. Ishikawa¹ and T. Kikkawa^{1,2}, ¹MIRAI-ASET, ²MIRAI-ASRC, AIST and ³RCNS, Hiroshima Univ., Japan</p>	<p>16:25 D-5-4 P-channel Vertical Double-Gate MOSFET Fabrication by Ion-Bombardment-Retarded Etching M. Masahara¹, T. Matsukawa¹, S. Hosokawa¹, K. Ishii¹, Y. Liu¹, H. Tanoue¹, K. Sakamoto¹, H. Yamauchi¹, S. Kanemaru¹ and E. Suzuki¹, ¹AIST, Japan</p>	<p>16:15 E-5-4 1-bit BDD full adder circuit using single electron transistors by selective area metalorganic vapor phase epitaxy Y. Miyoshi¹, F. Nakajima¹, J. Motohisa¹ and T. Fukui¹, ¹Hokkaido Univ. and ²NTT, Japan</p>	<p>16:15 F-5-4 Electrostatic Immobilization of Biomolecules using Nano-Electrode Array T. Yamamoto¹ and T. Fujii¹, ¹The Univ. of Tokyo, Japan</p>	<p>16:30 G-5-4 New Process of Self-organized Interconnection in Packaging by Conductive Adhesive with Low Melting Point Filler K. Yasuda¹, J.-M. Kim¹, M. Yasuda¹ and K. Fujimoto¹, ¹Osaka Univ., Japan</p>

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>16:30 A-5-5 Enhancement of Magneto-Optic Effect in Magneto-Optic Waveguide with Low Refractive Index Undercladding Layer Y. Shoji^{1,2}, H. Yokoi^{1,2} and T. Mizumoto³, ¹Tokyo Inst. of Technology and ²OITDA, Japan</p> <p>A-6: Optoelectronic Devices and Photonic Crystal Devices -Lasers for Optical Communication- (17:00-18:15) Chairs: H. Shimizu (The Furukawa Electric) M. Nielsen (Denmark Tech. Univ.)</p>	<p>16:15 B-5-5 Electrical Properties and Gas Response in Alternate Layer-by-Layer Films of Copper Phthalocyanine Dyes K. Kato¹, N. Watanabe¹, S. Katagiri¹, K. Shinbo¹, F. Kaneko¹ and R.C. Advincula², ¹Niigata Univ. and ²Univ. of Houston, Japan</p> <p>B-6: Non-Volatile Memory Technologies -Non-Volatile Memory V- (17:00-17:40) Chairs: K. Saito (NEC) H. Takada (Mitsubishi Electric)</p>	<p>C-6: Silicon Process / Materials Technologies -Interconnect- (17:00-18:20) Chairs: S. Saito (NEC) J. Koike (Tohoku Univ.)</p>	<p>D-6: New Materials and Characterization -Si/SiGe Devices and Materials- (17:00-18:30) Chairs: J. Murota (Tohoku Univ.) A. Sakai (Nagoya Univ.)</p>	<p>E-6: Novel Devices, Physics, and Fabrication -Nanoprocess and Nanodevices- (17:00-18:30) Chairs: M. Tabe (Sizuoka Univ.) Y. Takahashi (NTT)</p>	<p>16:30 F-5-5 Microfluidic Devices Integrated with Parmalloy Micropatterns for Manipulating Magnetic Beads N. Ichikawa¹, F. Omasu², Y. Nagasaki³ and T. Ichiki^{1,2}, ¹Toyo Univ., ²PRESTO and ³Tokyo Univ. of Science, Japan</p> <p>F-6: Micro-Nano Electromechanical Devices for Bio- and Chemical Applications -Micro-Nano Electro Mechanical Devices for Bio- and Chemical Applications - II- (17:00-18:00) Chairs: H. Tabata (Osaka Univ.) K. Shimoide (Asahi Kasei)</p>	<p>G-6: System-Level Integration and Packaging Technologies -System-Level Integration and Packaging Technologies III- (17:00-18:15) Chairs: M. Aoyagi (AIST) H. Ezawa (Toshiba)</p>
<p>17:00 A-6-1 (Invited) Advances in Widely-Tunable Optical Transmitters L.A. Coldren¹, ¹Agility Communications and UC-Santa Barbara, USA</p>	<p>17:00 B-6-1 Hot Carrier Injection / Fowler Nordheim Erase Silicon Nanocrystal Memory Cell Rajesh Rao¹, Robert Steimle¹, M. Sadt¹, C. Swift¹, R. Muralidhar¹, B. Hradsky¹, S. Straub¹, E. Prinz¹, J. Yater¹ and B. White¹, ¹Motorola SPS, USA</p>	<p>17:00 C-6-1 High-modulus Porous MSQ Films for Cu/Low-k Integration (keff<2.7) K. Misawa¹, S. Sone¹, H. Shin¹, K. Inukai¹, Y. Sudo¹, S. Kondo¹, B.U. Yoon¹, S. Tokitoh¹, K. Yoneda¹, T. Yoshie¹, N. Ohashi¹ and N. Kobayashi¹, ¹SELETE, Japan</p>	<p>17:00 D-6-1 (Invited) SiGe in Advanced CMOS Devices- an unique material equally helpful when present or absent T. Skotnicki¹, ¹STMicroelectronics, Crolled, France</p>	<p>17:00 E-6-1 (Invited) Nanoimprint Lithography-Enabling Engine to Nanotechnology S.Y. Chou¹, ¹Princeton Univ., USA</p>	<p>17:00 F-6-1 (Invited) Development of an integrated a-Si:H photodiode detector and its evaluation for chemical and biochemical microfluidic analysis T. Kamei^{1,3}, B.M. Paegel¹, E.T. Lagally¹, A.M. Skelley¹, J.R. Scherer¹, R.A. Street², and R.A. Mathies¹, ¹Univ. of California at Berkeley and ²Palo Alto Research Center</p>	<p>17:00 G-6-1 (Invited) AC Coupled Interconnect for High-Density High-Bandwidth Packaging P. Franzon¹, S. Mick¹, J. Wilson¹, L. Luo¹, K. Chandrasakhar¹, ¹NC State Univ., USA</p>
<p>17:30 A-6-2 40 GHz Actively Mode-Locked DBR Laser Diode Module with an Impedance Matching Circuit S. Arahira¹ and Y. Ogawa¹, ¹Okai Electric Industry Co., Ltd., Japan</p>	<p>17:20 B-6-2 A New Investigation on Erase V_t Variation of NOR Flash fabricated with 90 nm Technology T.Y. Kim¹, W.H. Lee¹, J.I. Han¹, S.E. Lee¹, H.G. Lee¹, S.Y. Kim¹, J.H. Park¹, M.K. Cho¹, Y.H. Song¹ and K. Kim¹, ¹Samsung Electronics, Korea</p>	<p>17:20 C-6-2 Control of Pore Size and Porosity in Periodic Porous Silica Low-k Films N. Hata^{1,2}, C. Negoro², K. Yamada¹ and T. Kikkawa^{1,3}, ¹MIRAI-ASRC, AIST, ²ASRC, AIST, ³MIRAI-ASET and ⁴RCNS, Hiroshima Univ., Japan</p>	<p>17:30 D-6-2 Structural Characterization of Strained Silicon Substrates by X-Ray Diffraction and Reflectivity M. Erdtmann¹, T. Langdo¹, C. Vineis¹, H. Badawi¹ and M. Bulsara¹, ¹AmberWave Systems Corp., USA</p>	<p>17:30 E-6-2 Photon-induced effect on single-charge-tunneling in a Si multidot Schottky FET R. Nuryadi¹, H. Ikeda¹, Y. Ishikawa¹ and M. Tabe¹, ¹Shizuoka Univ., Japan</p>	<p>17:30 F-6-2 Resonant Cavity Thin Film Photodiode for Compact Displacement Sensor M. Sasaki¹, F. Nakai, X. Mi, K. Hane, ¹Tohoku Univ., Japan</p>	<p>17:30 G-6-2 Inter-chip Wireless Interconnection using Si Integrated Antenna A.B.M. H.-U. Rashid¹, S. Watanabe¹ and T. Kikkawa¹, ¹RCNS, Hiroshima Univ., Japan</p>
<p>17:45 A-6-3 Very High Frequency Self-Pulsation and Stable Optical Injection Locking for Well-Defined Multi-Electrode DFB Lasers S. Nishikawa^{1,2}, M. Gotoda^{1,2}, T. Nishimura^{1,2}, Y. Tokuda^{1,2} and K. Matsumoto^{1,2}, ¹Mitsubishi Electric Corporation and ²OITDA, Japan</p>	<p>17:40 C-6-3 Off-time Dependence of Pulsed DC Electromigration MTF of Cu Multilevel Interconnection K. Oshima¹, T. Ishida¹, S. Miyazaki¹, T. Takahagi¹ and S. Shingubara¹, ¹Hiroshima Univ., Japan</p>	<p>17:50 D-6-3 Oxidation-Induced Damages on Germanium MIS Capacitors with HfO₂ Gate Dielectrics K. Kita¹, M. Sasagawa¹, K. Tomida¹, K. Kyuno¹ and A. Toriumi¹, ¹The Univ. of Tokyo, Japan</p>	<p>17:45 E-6-3 Room-Temperature Observation of Negative Differential Conductance Due to Large Quantum Level Spacing in Silicon Single-Electron Transistor M. Saitoh¹ and T. Hiramoto¹, ¹Univ. of Tokyo, Japan</p>	<p>17:45 F-6-3 RF Propagation Characteristics and pH Measurement for in vivo Wireless Healthcare Chip T. Yamada¹, H. Uesugi¹, K. Okada¹, K. Masu¹, H. Nakase², T. Kazuo², A. Oki¹ and Y. Horiike¹, ¹Tokyo Inst. of Technology, ²RIEC, Tohoku Univ. and ³National Inst. for Materials Science, Japan</p>	<p>17:45 G-6-3 Magnetic Near-Field Mappings over Fine Circuits by Fiber-Edge Magneto-Optic Probe M. Iwanami¹, S. Hoshino¹, M. Kishi¹ and M. Tsuchiya², ¹ASET and ²Univ. of Tokyo, Japan</p>	

Room A
18:00 A-6-4
 Lasing-Wavelength-Change-Suppression 980 nm Pump Laser Diodes for Metro Applications
 K. Kawasaki¹, K. Shigihara¹, H. Matsuoka¹, Y. Kunitsugu¹, T. Yagi¹, E. Omura¹ and Y. Mitsui¹,
¹Mitsubishi Electric Corporation, Japan

Room B

Room C
18:00 C-6-4
 CVD-Al/Flow-Al Technology for Filling Large Aspect Ratio Contact Holes
 M. Sakamoto¹, T. Aoki¹, K. Masu¹, S.J. Lim², M. Hatanaka², M. Ishikawa² and Y. Furumura¹,
¹Tokyo Inst. of Technology, ²ULVAC Inc. and ³Philbridge Inc., Japan

Room D
18:10 D-6-4
 Enhanced Metal-Induced Lateral Crystallization in Amorphous Ge/Si Layered Structure by Precursor Modulation
 H. Kanno¹, A. Kenjo¹, T. Sadoh¹ and M. Miyao¹, ¹Kyushu Univ., Japan

Room E
18:00 E-6-4
 Analytical SPICE Modeling of Realistic MOS-based Single-Electron Transistors –"MOSETs" with a Unique Distribution Function in the Coulomb Oscillation Region
 K.R. Kim¹, K.-W. Song¹, G. Baek¹, H.H. Kim¹, J.I. Huh¹, J.D. Lee¹ and B.-G. Park¹, ¹Seoul National Univ., Korea

Room F

Room G
18:00 G-6-4
 Variable RF Inductor on Si CMOS Chip
 S. Gomi¹, Y. Yokoyama¹, H. Sugawara¹, H. Ito¹, K. Okada¹, H. Hoshino², H. Onodera² and K. Masu¹, ¹Tokyo Inst. of Technology, and ²Kyoto Univ., Japan

18:45-20:45
Rump Session A
 "Can channel material/structure engineering become a guiding principle for future CMOS device technology?"

18:45-20:45
Rump Session B
 "What paradigm can nanoelectronic devices bring about?"

18:15 E-6-5
 Analysis of Back-Gate Voltage Dependence of Threshold Voltage of Thin SOI MOSFET and Its Application to Si Single-Electron Transistor
 S. Horiguchi¹, A. Fujiwara¹, H. Inokawa¹ and Y. Takahashi¹,
¹NTT Basic Research Labs, Japan

POSTER SESSION (13:00-15:00, OHGI)

P1 Advanced Silicon Circuits and Systems (6 Papers)

P1-1
Bank-Type Multiport Register File for Highly-Parallel Processors
T. Sueyoshi¹, H. Uchida¹, Y. Mitani², K. Hiramatsu³, H.J. Mattausch¹, T. Koide⁴ and T. Hironaka², ¹Hiroshima Univ. and ²Hiroshima City Univ., Japan

P1-2
Three-Dimensionally Stacked Analog Retinal Prosthesis Chip
J. Deguchi¹, T. Watanabe¹, T. Nakamura¹, Y. Nakagawa¹, J.-C. Shim¹, H. Kurino⁴ and M. Koyanagi², ¹Tohoku Univ., Japan

P1-3
Low-Voltage-Triggered PNP for ESD Protection in Mixed-Voltage I/O interface
M.-D. Ker¹, W.-J. Chang¹ and W.-Y. Lo², ¹National Chiao-Tung Univ., and ²Silicon Integrated Systems (SIS) Corp., Taiwan

P1-4
75-qubit Quantum Computing Emulator
M. Fujishima¹, K. Inai¹, T. Kitasho¹ and K. Hoh^{1,2}, ¹The Univ. of Tokyo and ²CREST-JST, Japan

P1-5
Efficient Suppression of Substrate Noise Coupling in CMOS Technology
W.-K. Yeh¹, S.-M. Chen², C.-M. Lai² and Y.-K. Fang², ¹National Univ. of Kaohsiung and ²National Cheng-Kung Univ., Taiwan

P1-6
All Digital One-chip Wireless Modem LSI with Acquisition Circuit
Y. Sakai¹, H. Nakase¹, Y. Isota¹ and K. Tsubouchi¹, ¹Tohoku Univ., Research Inst. of Electorical Communication, Japan

P2 Advanced Silicon Devices and Device Physics (17 Papers)

P2-1
Efficient Improvement of Hot-Carrier-Induced Degradation for Sub-0.1µm CMOSFET
C.-M. Lai¹, C.-C. Hu², J.-C. Lin³, S.-T. Pan⁴ and W.-K. Yeh¹, ¹Inst. of National Cheng Kung Univ., ²Shu-Te Univ., ³National Chiao-Tung Univ. and ⁴National Univ. of Kaohsiung, Taiwan

P2-2
Optimization of STI Stress and Active Geometry Configuration for Advanced CMOS Devices
T. Lin¹, Y. Gong¹, J.T. Tseng¹, L. Yu¹, T. Shen¹, D. Chen¹, T.P. Chen³, C.L. Kuo¹, W.T. Shiau¹ and J.K. Chen¹, S.C. Chien and S.W. Sum, ¹United Microelectronics Corporation, Taiwan

P2-3
Modeling of Pocket Implant Effect on Drain Current Flicker Noise in High Performance Analog CMOS Devices
J.-W. Wu¹, J.C. Guo², K.-L. Chiu¹, C.-C. Cheng¹, W.Y. Lien¹, G.W. Huang³ and T. Wang², ¹National Chiao-Tung Univ., ²Taiwan Semiconductor Manufacturing Company, and ³National Nano Device Labs, Taiwan

P2-4
Novel Substrate Engineering for High Performance CMOSFETs using Channeling Ion Implantation
M. Kitazawa¹, T. Yamashita¹, Y. Kawasaki¹, T. Kuroi¹, T. Eimori¹, M. Inuishi¹ and Y. Ohji¹, ¹Renesas Technology Corp., Japan

P2-5
A New Stable Extraction of Threshold Voltage Using Regularization Method
W.Y. Choi^{1,2}, B.Y. Choi^{1,2}, D.-S. Woo^{1,2}, M.W. Lee^{1,2}, J.D. Lee^{1,2} and B.-G. Park^{1,2}, ¹Inter-univ. Semiconductor Research Center (ISRC) and ²Seoul National Univ., Korea

P2-6
A New Approach to Gate Dielectric Integrity Based on Differences Between i) Strained and ii) Strain-Free Interfacial Regions: Applications to Devices with Alternative High-k Dielectrics
G. Lucovsky¹, J.C. Phillips² and P. Boolchand¹, ¹North Carolina State Univ., ²Rutgers Univ. and ³Univ. of Cincinnati, USA

P2-7
A Variable Channel-Size MOSFET with LDD Structure
N. Nakanose¹, Y. Arima¹, T. Asano¹, Y. Kosasayama², M. Ueno³ and M. Kimata³, ¹Kyushu Inst. of Technology and ²Mitsubishi Electric Corp., Japan

P2-8
Novel ESD Protection Design for Nanoscale CMOS Integrated Circuits
M.-D. Ker¹ and T.-K. Tseng², ¹National Chiao-Tung Univ., Taiwan and ²Industrial Technology Research Inst., Taiwan, Taiwan

P2-9
A New One-Transistor One-Bipolar (1T1B) Capacitor-Less DRAM Cell
J.-K. Park¹ and J. Woo¹, ¹Univ. of California at Los Angeles, USA

P2-10
On-current Modeling of poly-Si TFT
K.C. Moon¹, S.-H. Kang¹ and M.-K. Han¹, ¹Seoul National Univ., Korea

P2-11
Characterization and Modeling of High Q-Factor, High Resonant Frequency Spiral Inductors with 6 µm thick Top-Metal for RF-IC Applications
Y.-S. Lin¹, H.-W. Chiu², S.-H. Wu¹ and S.-S. Lu², ¹National Chi-Nan Univ., ²National Taiwan Univ., Taiwan

P2-12
Design Issues for Sub-100nm Analog CMOS
M. Garg¹, S. Suryagandhi¹ and J. Woo¹, ¹Univ. of California Los Angeles, USA

P2-13
Split Gate Engineering for RF/Analog Application In Sub 50 nm NMOSFET
J. Yuan¹ and J. Woo¹, ¹Univ. of California, Los Angeles, USA

P2-14
A Simple Wide-Band MIM Capacitor Model for RF Applications and the Effect of Substrate Grounded Shields
S.-S. Song¹, S.-W. Lee¹, J. Gil¹ and H. Shin², ¹Korea Advanced Institute of Science and Technology and ²Seoul National Univ., Korea

P2-15
Improvement on Turn-on Speed of Substrate-Triggered SCR Device by Using Dummy-Gate Structure for On-Chip ESD Protection
K.-C. Hsu¹ and M.-D. Ker¹, ¹National Chiao-Tung Univ., Taiwan

P2-16
A new Conductivity Modulated LDMSFET employing Buried P Region and P+ Drain
J.-K. Oh¹, B.-C. Jeon¹, M.-K. Han¹ and Y.-I. Choi², ¹Seoul National Univ. and ²Ajou Univ., Korea

P2-17
Trench IGBT for the Improved Short Circuit Capability by Employing the Curved Junction and Wide Cell Pitch
S.-S. Kim¹, M.-W. Ha¹, Y.-I. Cho² and M.-K. Han¹, ¹Seoul National Univ. and ²Ajou Univ., Korea

P3 Silicon Process / Materials Technologies (19 Papers)

P3-1
Novel Storage-Node Contacts with Stacked PCM-Sp-TiN Barrier for MIM-Ru/Ta₂O₅/Ru Capacitors in Giga-Bit DRAMs
T. Kawagoe¹, Y. Nakamura¹, K. Kuroki¹, I. Asano¹, H. Goto¹ and N. Nakanishi¹, ¹Elpida Memory, Inc., Japan

P3-2
Very High Reliability of Ultrathin Silicon Nitride Gate Dielectric Film for sub-100nm Generation
M. Komura¹, M. Higuchi¹, W. Cheng¹, I. Ohshima², A. Teramoto³, M. Hirayama², S. Sugawa⁴ and T. Ohmi², ¹S.-S. Song¹, S.-W. Lee¹, J. Gil¹ and H. Shin², ¹Korea Advanced Institute of Science and Technology and ²Seoul National Univ., Korea

P3-3
Excellent Contact-Hole Etching with NH₃ Added C.F. Pulse-Modulated Plasma
M. Ooka¹ and S. Yokoyama¹, ¹RCNS, Hiroshima Univ., Japan

P3-4
Electroless Copper Seed Activated by 1nm ICB-Pd Catalytic Layer for Fine Cu Interconnections
Z. Wang¹, O. Yaegashi¹, H. Sakaue¹, T. Takahagi¹ and S. Shingubara¹, ¹Hiroshima Univ., Japan

P3-5
Atomic Order Flattening of Hydrogen-Terminated Si(110) Substrate For Next Generation ULSI Devices
H. Akahori¹, K. Nii¹, A. Teramoto¹, S. Sugawa² and T. Ohmi¹, ¹NICHE, Tohoku Univ. and ²Tohoku Univ., Japan

P3-6
An Integrated Gate Stack Process for Sub-90nm CMOS
S.J. Chang¹, S.Y. Wu¹, C.L. Chen¹, T.L. Lee¹, Y.M. Lin¹, Y.S. Tsai¹, H.D. Su¹, S.B. Chen¹, Y.S. Chen¹, M.S. Liang¹, Y.C. See¹ and Y.C. Sun¹, ¹Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan

P3-7
Precursors for chemical vapor deposition of NiSi
M. Ishikawa¹, T. Kada¹, H. Machida¹, Y. Ohshita² and A. Ogura³, ¹TRI Chemical Labs Inc., ²Toyota Technological Inst. and ³NEC Corp., Japan

P3-8
MOCVD HfAlO₂ Gate Dielectrics Deposited Using Single Cocktail Liquid Source
M.S. Joo¹, B.J. Cho¹, C.C. Yeo¹, S.J. Whoang², S. Matthew³, L.K. Bera¹, N. Balasubramanian¹ and D.-L. Kwong², ¹SNL, National Univ. of Singapore, ²Jusung Engineering Co., Ltd., Korea, ³Inst. of Microelectronics, Singapore and ⁴The Univ. of Texas, Austin, Singapore

P3-9
Tight-Binding Quantum Chemical Molecular Dynamics Simulation on Chemical Mechanical Polishing Process of Cu Surface
N. Isoda¹, K. Sasata¹, T. Yokosuka¹, A. Endou¹, M. Kubo¹, A. Imamura² and A. Miyamoto^{1,3}, ¹Tohoku Univ., ²Hiroshima Kokusai Gakuin Univ. and ³NICHE, Tohoku Univ., Japan

P3-10
A Novel Photosensitive Porous Low-k Interlayer Dielectric Film
S. Kuroki¹, T. Hirota² and T. Kikkawa¹, ¹RCNS, Hiroshima Univ. and ²TAZMO Co., Ltd., Japan

P3-11
Increase of Crystallization Temperatures of Ultrathin Al₂O₃ Films Caused by Si Diffusion during Annealing
S. Migita¹, J.-W. Park², T. Yasuda¹, M. Nishizawa¹, R. Kuse², T. Nabatame² and A. Toriumi³, ¹MIRAI-AIST, ²MIRAI-ASET and ³Univ. of Tokyo, Japan

P3-12
Neutral Beam Etching for Damage-free 50 nm Gate Electrode Patterning
S. Noda^{1,2}, H. Nishimori¹, T. Ida¹, T. Arikado³, K. Ichiki¹ and S. Samukawa¹, ¹Tohoku Univ., ²Semiconductor Leading Edge Technologies, Inc., ³Ebara Research Co., Ltd., Japan

P3-13
Defect Generation in Gate Oxide by Selective Oxidation in Hydrogen-rich Wet Ambient
H.-J. Cho¹, K.-Y. Lim¹, S.-A. Jang¹, J.-H. Lee¹, J.-G. Oh¹, Y.-S. Kim¹, H.-S. Yang¹ and H.-C. Sohn¹, ¹Hynix Semiconductor Inc., Korea

P3-14
Improving Electrical Properties of CVD HfO₂ by Multi-Step Deposition and Annealing in a Gate Cluster Tool
C.C. Yeo¹, B.J. Cho¹, M.S. Joo¹, S.J. Whoang², D.-L. Kwong², L.K. Bera¹, S. Mathew² and N. Balasubramanian¹, ¹National Univ. of Singapore, ²Jusung Engineering Co., Ltd., ³The Univ. of Texas at Austin and ⁴Inst. of Microelectronics, Singapore

P3-15
Influence of Humidity on Electrical Characteristics of Porous Silica Films
S. Sakamoto¹, S. Kuroki¹ and T. Kikkawa¹, ¹RCNS, Hiroshima Univ., Japan

P3-16
Chemical structure of N Atoms in the Transition Region of the SiO(N)/Si Interface -A New Spectroscopic Method with Hydrogenation Reaction in HF Acid-
N. Mizuta¹ and S. Watanabe¹, ¹Fujitsu Labs Ltd, Japan

P3-17
The sheet resistance instability in the sub-100 nm tungsten poly-metal wordline due to an *in-situ* NH₃ pre-annealing during the sealing nitride deposition
K.-Y. Lim¹, J.-H. Lee¹, H.-J. Cho¹, J.-G. Oh¹, B.-S. Hong¹, S.-A. Jang¹, Y.-S. Kim¹, H.-S. Yang¹ and H.-C. Sohn¹, ¹Hynix Semiconductor Inc., Korea

P3-18
Influence of interface layers and bottom electrode on (Ba,Sr)TiO₃ thin film leakage current
M. Yamato¹ and T. Kikkawa¹, ¹RCNS, Hiroshima Univ., Japan

P3-19
Interface Oxidation Mechanism in HfO₂/Silicon System with Post-Deposition Annealing
H. Shimizu¹, M. Sasagawa¹, K. Kita¹, K. Kyuno¹ and A. Toriumi¹, ¹The Univ. of Tokyo, Japan

P4
New Materials and Characterization
(18 Papers)

P4-1
Improving the Accuracy of Modified Shift-and-Ratio Channel Length Extraction Method Using Scanning Capacitance Microscopy
C.W. Eng^{1,2}, W.S. Lau¹, Y.Y. Jiang³, D. Vigar², K.C. Tee¹, L. Chan¹, S.W.V. Lim³ and A. Trigg³,
¹Nanyang Technological Univ. of Singapore, ²Chartered Semiconductor Manufacturing Ltd and ³Inst. of Microelectronics, Singapore

P4-2
Influence of nitrogen profile on metal work function in Mo/SiO₂/Si MOS structure
M. Hino¹, T. Amada¹, N. Maeda¹ and K. Shibahara¹, ¹RCNS, Hiroshima Univ., Japan

P4-3
Compact Electrical Characterization of Nano-CMOS Transistor with 1.2nm Ultrathin Gate Dielectric
H.S. Kang¹, W.-Y. Quan², K.S. Kim¹, C.B. Oh¹, H.J. Ryu¹, C.K. Baek¹, B. Kim¹, Y.W. Kim¹, K.P. Suh¹, and D.M. Kim²,
¹Samsung Electronics, ²Korea Inst. for Advanced Study, Korea

P4-4
Cross-Hatch Related Oxidation and Reliability of Gate Oxide of Strained-Si/SiGe
M. Nishisaka¹ and T. Asano¹,
¹Kyushu Inst. of Technology, Japan

P4-5
Visible Light Irradiation Effects on Atomic-Scale Observations of Hydrogenated Amorphous Silicon Films by Scanning Tunneling Microscopy
K. Arima¹, H. Kakiuchi¹, M. Ikeda¹, K. Endo², M. Morita¹ and Y. Mori², ¹Osaka Univ. and ²Research Center for Ultra-Precision Science and Technology, Osaka Univ., Japan

P4-6
Influence of structural variation of Ni silicide thin films on electrical property for contact materials
K. Okubo¹, Y. Tsuchiya¹, O. Nakatsuka¹, A. Sakai¹, S. Zaima¹ and Y. Yasuda¹,
¹Nagoya Univ., Japan

P4-7
Ultra-shallow Boron Profile Fitting Compensating for Surface Contamination by Utilizing Genetic Algorithms
M. Murakawa¹, K. Shibahara², Y. Oda³, T. Higuchi¹ and K. Nishi¹, ¹AIST, ²Hiroshima Univ. and ³SELETE, Japan

P4-8
Nucleation-Control in Solid-Phase-Crystallization of a-Si/SiO₂ by Local Ge Insertion
I. Tsunoda¹, K. Nagatomo¹, A. Kenjo¹, T. Sadoh¹, S. Yamaguchi² and M. Miyao¹,
¹Kyushu Univ. and ²Hitachi, Japan

P4-9
Atomic-scale Adsorbent Structure of Contaminant Metal on Si(100) Surface and its Effect on Thermal Oxidation
T. Onizawa^{1,2}, T. Narushima^{1,2,3,4}, K. Miki^{1,3} and K. Yamabe¹, ¹NRI, ²AIST, ³Univ. of Tsukuba, ⁴NML, NIMS and ⁵SFIT Trinity Nanoscience Lab, Trinity College Dublin, Japan

P4-10
Effect of Vacuum Annealing on High-k Dy₂O₃ Thin Films Deposited on Si(100)
S. Ohmi¹, H. Yamamoto¹, J. Taguchi¹, K. Tsutsui¹ and H. Iwai¹, ¹Tokyo Inst. of Technology, Japan

P4-11
Formation of Strained β-FeSi₂(Ge) by Ge-Segregation Controlled Solid-Phase Growth of [Amorphous Si/FeSiGe]_n Multi-Layered Structure
T. Sadoh¹, M. Owatari¹, A. Kenjo¹, T. Yoshitake¹, M. Itakura¹ and M. Miyao¹,
¹Kyushu Univ., Japan

P4-12
Electrical properties of crystalline γ-Al₂O₃ films using conductive-AFM and MISFETs with Aluminum gates
T. Okada¹, R. Ito¹, M. Shahjahan¹, K. Sawada¹ and M. Ishida¹, ¹Toyohashi Univ. of Technology, Japan

P4-13
Wet Etching Characteristics of both As-deposited and Annealed Al₂O₃ and HfAlO₃ Films
T. Nishimura¹, R. Kuse², K. Tominaga², T. Nabatame² and A. Toriumi^{1,3}, ¹MIRAI project, ASRC, AIST, ²MIRAI ASET and ³The Univ. of Tokyo, Japan

P4-14
Impact of Ti/TiN Formation on Ultra-thin Gate Oxide Reliability (HCI and NBTI) for Deep Sub-micron CMOS Transistors
C. Liu¹, M.G. Chen¹, Y.R. Yang¹ and Y.T. Loh¹, ¹UMC, Taiwan

P4-15
Characterization and Comparison of Strained Si_{0.7}C_{0.3} MOSFET Grown by Gas Source MBE and Hot Wire Cell Method
T. Watahiki¹, K. Abe², A. Yamada² and M. Konagai¹,
¹Tokyo Inst. of Technology, ²Shinshu Univ., Japan

P4-16
Effect of Nitrogen Annealing on the Electrical Properties of Ultrathin Crystalline γ-Al₂O₃ High-κ Dielectric Films Deposited on Si(111) Substrates
M. Shahjahan¹, T. Okada¹, K. Sawada¹ and M. Ishida¹,
¹Toyohashi Univ. of Technology, Japan

P4-17
Electrical properties and conduction mechanism of ZrO₂ films on Si_{1-x}C_x
G.K. Dalapati¹, S.K. Samanta², S. Chatterjee¹, P.K. Bose¹, S. Varma¹, S. Patil³ and C.K. Maiti², ¹IIT Kharagpur, ²Jadavpur Univ., ³Inst. of Physics, Bhubaneswar, India

P4-18
Failure Mechanism of Nano-crystalline VN barrier in Cu/VN/SiO₂/Si system
T. Itoi¹, O. Yanada¹, K. Satoh¹, B.M. Takeyama¹ and A. Noya¹,
¹Kitami Inst. of Technology, ²Chiba Univ., ³SEC Ltd. and ⁴Hitachi Kokusai Electric Inc., Japan

P5
Compound Semiconductor Materials and Devices
(12 Papers)

P5-1
Metal-Semiconductor-Metal UV Photodetector Based on AlGaIn/GaN Heterostructure
H. Jiang¹, T. Egawa¹, H. Ishikawa¹, Y. Dou¹, C. Shao¹ and T. Jimbo¹, ¹Nagoya Inst. of Technology, Japan

P5-2
Low Frequency Noise Caused by Substrate Current in AlGaAs/InGaAs HEMTs
M. Wada¹, S. Nishiyama¹, T. Nakamoto¹ and K. Higuchi¹,
¹Hiroshima Univ., Japan

P5-3
Electro Static Discharge effects on AlGaIn/GaN HEMTs on sapphire substrates
S.-C. Lee¹, J.-C. Herl¹, K.-S. Seo¹ and M.-K. Han¹, ¹Seoul National Univ., Korea

P5-4
Study of InGaP/InGaAs Double Doped Channel Heterostructure Field-effect Transistor (DDCHFET)
H.-M. Chuang¹, C.-Y. Chen¹, P.-H. Lai¹, S.-L. Fu¹, Y.-Y. Tsai¹, C.-I. Kao¹ and W.-C. Liu¹, ¹Inst. of Microelectronics, National Cheng-Kung Univ., Taiwan

P5-5
Nitride-based blue LEDs with GaN/SiN double buffer layers
C.-H. Kuo¹, S.-J. Chang¹, Y.-K. Su¹, C.-K. Wang¹, L.-W. Wu¹, J.-K. Sheu² and J.-M. Tsai³, ¹National Cheng Kung Univ., ²National Central Univ. and ³South Epitaxy Corporation, Taiwan

P5-6
Thermal Annealing Effect in GaInNAs Thin Films Estimated by X-ray Absorption Fine Structure Spectroscopy
K. Uno¹, M. Yamada¹, T. Takizawa² and I. Tanaka¹,
¹Fac. Systems Eng., Wakayama Univ. and ²Matsushita Elec. Co., Ltd., Japan

P5-7
A Double-Barrier-Emitter Triangular Barrier Optoelectronic Switch
J.-Y. Chen¹, D.-F. Guo², K.-M. Lee¹, H.-M. Chuang¹, C.-Y. Chen¹ and W.-C. Liu¹,
¹National Cheng-Kung Univ., Taiwan and ²Chinese Air Force Academy, Taiwan

P5-8
GaAs-MISFETs with nm-Thin Gate Insulating Films Formed by Oxi-Nitridation Process
M. Takebe¹, N.C. Paul¹, S. Nakamura¹, K. Iiyama¹ and S. Takamiya¹, ¹Kanazawa Univ., Japan

P5-9
Characterization of Threading Dislocation in Si-doped GaN Films by High Spatial Resolution Cathodoluminescence Spectroscopy
R. Sugio¹, M. Yoshikawa¹ and H. Harima², ¹Toray Research Center Inc. and ²Kyoto Inst. of Technology, Japan

P5-10
Characterization of AlInAsSb/GaInAsSb Multiple Quantum Wells Grown by MOVPE
Y.-K. Su¹, C.-H. Wu¹ and J.-R. Chang¹, ¹Inst. of Microelectronics, National Cheng Kung Univ., ²Epistar Corporation, Taiwan

P5-11
Growth Temperature Dependence of Nitrogen Incorporation in GaNAs Grown by Chemical Beam Epitaxy
Y. Sun¹, M. Yamamori¹, T. Egawa¹ and H. Ishikawa¹,
¹Nagoya Inst. of Technology, Japan

P5-12
Al-doped ZnO Intermediate Layer for AlGaIn/GaN HEMT Ohmic Contact
K. Nishizono¹, M. Okada¹, M. Kamei², D. Kikuta¹, J.-P. Ao¹, K. Tominaga¹ and Y. Ohno¹,
¹The Univ. of Tokushima, Japan

P6
Optoelectronic Devices and Photonic Crystal Devices
(14 Papers)

P6-1
Investigation of Nonreciprocal Phase Shift Characteristics for Integrated Optical Waveguide Isolators Utilizing Magnetic Photonic Crystals
J.S. Yang¹, G. Lee¹, T.H. Lee¹, Y.-I. Kim¹, M.-C. Park¹, Y.T. Byun¹, D.H. Woo¹, S. Lee¹, S.H. Song¹ and S.H. Kim¹,
¹Korea Inst. of Science and Technology and ²Hanyang Univ., Korea

P6-2
Magneto-optic Spatial Light Modulator with One-Step Pattern Growth on Ion-Milled Substrates by Liquid-Phase Epitaxy
J.-H. Park^{1,2}, J.-K. Cho¹, K. Nishimura¹, H. Uchida¹ and M. Inoue^{1,2}, ¹Toyohashi Univ. of Technology, Japan, ²Gyeongang National Univ., Korea, ³ASTF and ⁴CREST-JST, Japan

P6-3
Optical Properties of Acrylate-Based Negative-Type Photoresist and Fabrication of Optical Waveguides
P. Gutafik¹, O. Sugihara² and N. Okamoto¹, ¹Shizuoka Univ. and ²Tohoku Univ., Japan

P6-4
Optical Tuning of Defect-Induced Pass-Band in Photonic Crystal Waveguide
M. Tsuji¹, Y. Iida¹ and Y. Omura¹, ¹Kansai Univ., Japan

P6-5
Numerical Analysis of Waveguides in Three-Dimensional Photonic Crystal with Finite Thickness
Y. Watanabe¹, N. Yamamoto^{1,2} and K. Komori¹, ¹AIST and ²CREST, JST, Japan

P6-6
Fabrication of Wide Area Two-Dimensional Photonic Crystal Using Holographic Lithography
J.I. Moon¹, S.H. Kim¹, S.H. Park¹ and Y.T. Lee¹, ¹Kwangju Inst. of Science Technology, Korea

P6-7
A Study of Magnetostriction and Its Application to Silicon-on-Insulator Waveguides
P.S. Chan¹ and H.K. Tsang¹, ¹The Chinese Univ. of Hong Kong., China

P6-8
Blue Luminescence of Porous Alumina Membranes Prepared by Anodic Oxidation
T. Echizenya¹, K. Takase¹, Y. Takahashi¹, Y. Takano¹ and K. Sekizawa¹, ¹Nihon Univ., Japan

P6-9
AlGaAs/InGaAs DFB Laser by One Time Selective MOCVD Growth on a Grating Substrate
Y. Takasuka^{1,2}, K. Yonei², H. Yamauchi¹ and M. Ogura¹, ¹AIST and ²Shibaura Inst. of Technology, Japan

P6-10
InGaIn/GaN Light Emitting Diodes with a Lateral Current Blocking Structure
W.-B. Chen¹, Y.-K. Su¹, C.-L. Lin¹, H.-C. Wang¹ and S.-M. Chen², ¹National Cheng Kung Univ., and ²Epitech Technology Corporation, Taiwan

P6-11
Characteristics of P-I-i-N GaAs/Al_{0.3}Ga_{0.7}As Phase Modulator and MultiMode Interference Used in the TE/TM Mode Splitter
S.-P. Kim^{1,2}, J.-M. Son^{1,2}, S.-S. Lee¹, S. Lee², D.-H. Woo² and S.-H. Kim², ¹Hanyang Univ. and ²Korea Inst. of Science and Technology, Korea

P6-12
Surface Plasmon Resonance and Emission Light Properties of Polystyrene Sphere Thin Films
K. Shinbo¹, S. Miyabayashi¹, K. Yoshizawa¹, H. Shirasawa¹, K. Kato¹ and F. Kaneko¹,
¹Niigata Univ., Japan

P6-13
Enhanced Frequency Response Associated with Negative Photoconductance in an InGaAs/InAlAs Avalanche Photodiode
G. Kim¹, I.G. Kim¹, J.H. Baek¹ and O.K. Kwon¹, ¹Electronics & Telecommunication Research Inst., Korea

P6-14
The Characteristic of InGaN/GaN Multiple-Quantum-Well Metal-Insulator-Semiconductor Photodiodes Using SiO₂ Fabricated by Photochemical Vapor Deposition
P.C. Chang¹, C.H. Chen¹, S.J. Chang¹, Y.K. Su¹, P.C. Chen¹, Y.D. Jhou¹, H. Hung¹, S.L. Wu², and K.C. Huang², ¹National Cheng Kung Univ. and ²Cheng Shiu Inst. of Technology, Taiwan

P7
**Novel Devices, Physics,
and Fabrication**
(8 Papers)

P7-1
Novel comb-type differential pressure sensor with silicon beams embedded in a silicone rubber membrane
C.T. Seo¹ and J.H. Lee¹,
¹Kyungpook National Univ., Korea

P7-2
Periodic Coulomb oscillation in highly doped Si single-electron transistor
T. Kitade¹, K. Ohkura¹ and A. Nakajima¹,¹RCNS, Hiroshima Univ., Japan

P7-3
Active Pixel Sensor Using an SOI MOSFET Photodetector with a Quantum Wire
J.-H. Park¹, S.-H. Seo¹, I.-S. Wang¹, J.-H. Kim¹, J.-K. Shin¹, P. Choi¹, Y.-C. Jo² and H. Kim²,¹Kyungpook National Univ. and ²Korea Electronics Technology Inst., Korea

P7-4
Side Gating Phenomenon in GaAs Quantum Wire Transistors
R. Jia¹, S. Kasai¹ and H. Hasegawa¹,¹RCIQE, Hokkaido Univ., Japan

P7-5
Observation of current modulation in SAM-FET fabricated by an air-bridge structure
K. Sasao¹, Y. Azuma¹, N. Kaneda¹, E. Hase¹, Y. Miyamoto¹ and Y. Majima¹,¹Tokyo Inst. of Technology, Japan

P7-6
Generation of Local Magnetic Field by Nano Electro-Magnets
H.K. Kim^{1,2}, S.H. Hong¹, B.C. Kim¹, J.S. Hwang², S.W. Hwang^{1,2} and D. Ahrn²,¹Korea Univ. and ²Univ. of Seoul, Korea

P7-7
Atomic-scale Smoothing and Structural Analysis of LiNbO₃ Surface
A. Saito^{1,2}, H. Matsumoto¹, S. Ohnisi², M. Akai-Kasaya¹, Y. Kuwahara^{1,2} and M. Aono^{1,2},¹Osaka Univ., ²RIKEN and ³National Inst. for Materials Science, Japan

P7-8
Electron Transport in Molecular Enamel Wires
Rodion Belosludov¹, Amir Farajian¹, Hiroshi Mizuseki¹, Kyoko Ichinoseki¹ and Yoshiyuki Kawazoe¹,¹Tohoku University, Japan

P8
**Quantum Nanostructure
Devices and Physics**
(10 Papers)

P8-1
Spin depolarization via tunneling effects in asymmetric double quantum dot structure
H. Sasakura¹, S. Adachi¹, S. Muto¹, H. Song², T. Miyazawa² and T. Usuki²,¹Hokkaido Univ. and ²CREST, JST and ³Fujitsu Labs Ltd., Japan

P8-2
Mechanical Properties of Nanometer-sized Cu Contacts
T. Kizuka¹, M. Mori¹, S. Fujisawa² and A. Yabe²,¹Univ. of Tsukuba, ²AIST, Japan

P8-3
A Study on Doping Density in InAs/GaAs Quantum Dot Infrared Photodetector
U.H. Lee¹, Y.H. Kang¹, J.H. Oum¹, S.-J. Lee², M. Kim², S.K. Noh², Y.D. Jang¹, D. Lee¹ and S. Hong¹,¹Korea Advanced Inst. of Science and Technology, ²Korea Research Inst. of Standards and Science and ³Chungnam National Univ., Korea

P8-4
Enhanced Optical Properties of High Density (>10¹¹/cm²) InAs/AlAs Quantum Dots by Using Hydrogen Passivation
S.-K. Park¹, J. Tatebayashi¹, Y.J. Park² and Y. Arakawa¹,¹RCAST and IIS, Univ. of Tokyo, Japan and ²Korea Inst. of Science and Technology, Korea

P8-5
Controlling the optical properties of self-assembled InAs quantum dots by various annealing treatments
J.-J. Yoon¹, S.-I. Jung¹, H. Choi¹, J.W. Lee¹, G.S. Cho¹, M.H. Jeon¹, J.-Y. Leem¹, D.Y. Lee², J.S. Kim², J.S. Son², S.I. Ban¹, J.I. Lee² and J.S. Kim²,¹InJe Univ., ²Yeungnam Univ., ³Nanomaterials Lab., ⁴Kyungwoon Univ., ⁵Materials Evaluation Center and ⁶Basic Res. Lab., ETRI, Korea

P8-6
Control of GaSb/GaAs Quantum Nanostructures by Molecular Beam Epitaxy
T. Nakai¹, S. Iwasaki¹ and K. Yamaguchi¹,¹The Univ. of Electro-Communications, Japan

P8-7
Formation of Ge Quantum dots by Selective Oxidation of SiGe alloys for Single-Electron Devices
P.-W. Li¹, W.-M. Liao¹, S.W. Lin¹, P.S. Chen¹ and M.J. Tsai¹,¹National Central Univ. Taiwan

P8-8
Investigation of Ultrafast Carrier Dynamics in Quantum Wire by Terahertz Spectroscopy
I. Morohashi^{1,2}, K. Komori^{1,2}, T. Hidaka¹, G.-R. Wang¹, M. Ogura¹ and M. Watanabe¹,¹National Inst. of Advanced Industrial Science and Technology, ²CREST, JST and ³Shonan Inst. of Technology, Japan

P8-9
Influence of deep-level concentrations on strong red photoluminescence from nano-porous silicon formed on Fe-contaminated silicon substrate
D.-Y. Lee¹, J.-W. Park¹, S.-S. Choi¹, D.-H. Kim¹, I.-H. Bae¹, J.-Y. Leem², J.-S. Kim³, S.-K. Kang⁴, J.-S. Son¹ and I.-S. Kim²,¹Yeungnam Univ., ²Inje Univ., ³National Inst. for Materials Science, ⁴Kyunghee Univ. and ⁵Kyungwoon Univ., Korea

P8-10
Identification of valence-band ordering in ZnO by using four-wave mixing
S. Adachi¹, S. Muto¹, K. Hazu², T. Sota², K. Suzuki² and S. Chichibu³,¹Hokkaido Univ., ²Waseda Univ. and ³Univ. of Tsukuba, Japan

P9
**Silicon-on-Insulator
Technologies**
(8 Papers)

P9-1
SOI SRAM / DRAM Cells for 0.5 Volt Operation
M. Terauchi¹,¹Hiroshima City Univ., Japan

P9-2
Complete Surface-Potential-Based SOI-MOSFET Model for Circuit Simulation
D. Kitamaru¹, Y. Uetsuji¹ and M. Miura-Mattausch¹,¹Hiroshima Univ., Japan

P9-3
Complementary Operation of Schottky Source/Drain SOI MOSFET with Shallow Doped Extension
S. Matsumoto¹, M. Nishisaka¹ and T. Asano¹,¹Kyushu Inst. of Technology, Japan

P9-4
A Workable Use of Floating-Body SOS MOSFET as a Transconductance Mixer
S. Lam¹, A.C.-K. Chan¹, W.-K. Lee¹, P.K.T. Mok¹, P.K. Ko¹ and M. Chan¹,¹Hong Kong Univ. of Science & Technology, Hong Kong

P9-5
Threshold Voltage Control on the Body-Tied FinFET (OMEGA MOSFET)
H.J. Jo¹, T.-S. Park², J.D. Choe¹, S.Y. Han¹, J.H. Jeong¹, M.C. Chae¹, D.G. Park¹, K. Kim¹, E. Yoon² and J.-H. Lee¹,¹Samsung Electronics Co., Ltd, ²Seoul National Univ. and ³Kyungpook National Univ., Korea

P9-6
High Performance Buried Gate Surrounding Gate Transistor (BG-SGT) for Future Three-Dimensional Devices
M. Iwai¹, Y. Yamamoto¹, R. Nishi¹, H. Sakuraba¹, T. Endoh¹ and F. Masuoka¹,¹RIEC, Tohoku Univ., Japan

P9-7
Thermal conductivity of high-integrity nanometer buried oxides by SIMOX
Y. Dong¹, X. Wang¹, J. Chen¹, M. Chen^{1,2}, X. Wang^{1,2}, P. He¹, L. Tian¹ and Z. Li¹,¹Shanghai Inst. of Microsystem and Information Technology, Chinese Academy of Sciences, ²Shanghai Simgu Technology Co., Ltd. and ³Inst. of Microelectronics, Tsinghua Univ., China

P9-8
Low frequency noise in partially-depleted SOI MOSFETs operating from linear region to saturation region at various temperatures
K.-M. Chen¹, H.-H. Hu², G.-W. Huang¹, S.-Y. Huang², A.S. Peng¹, W.-K. Yeh¹ and C.-Y. Chang²,¹Natioanal Nano Device Labs, ²Natioanal Chiao Tung Univ. and ³National Univ. of Kaohsiung, Taiwan

P10
**Non-Volatile Memory
Technologies**
(9 Papers)

P10-1
Improvement of Data Retention in Floating Gate Flash EEPROM's with P-Doped Floating Gate
B.C. Wu¹, H.W. Tsai¹, S.S. Chung¹, C.J. Lin¹, D.S. Kuo¹, and M.S. Liang²,¹National Chiao Tung Univ., ²Tsmc, Science-based Industrial Park, Hsinchu, Taiwan and ³Nexflash Inc., San Jose, USA

P10-2
New Three Dimensional High Density S-SGT Flash Memory Architecture using Self-Aligned Interconnection Fabricating Technology without Photo Lithography Process for Tera Bits and Beyond
H. Sakuraba¹, K. Kinoshita², T. Tanigami², T. Yokoyama¹, S. Horii¹, M. Saitoh¹, K. Sakiyama¹, T. Endoh¹ and F. Masuoka¹,¹RIEC, Tohoku Univ. and ²Sharp Corporation, Japan

P10-3
The Impact of Technology Parameters and Scaling on the Programming Performance and Drain Disturb in CHISEL Flash EEPROMs
D. Nair¹, N. Mohapatra¹, S. Mahapatra¹ and S. Shukuri²,¹Indian Inst. of Technology, India and ²Hitachi Ltd., Japan

P10-4
Key technologies of First 'Chain' -32M bit Ferroelectric RAM
T. Ozaki¹, N. Nagel¹, Y. Kumura¹, J. Lian¹, A. Hilliger¹, T. Tsuchiya¹, R. Bruchhaus, H. Kanaya¹, H. Koyama, U. Wellhausen, O. Hidaka, S. Shuto, S. Germhardt, Y. Shimajo, B.K. Moon, H. Itokawa, U. Egger, H. Zhuang, K. Tomioka, M. Fukushima, K. Yamakawa, D. Takashima, I. Kunishima¹, Y. Oowaki¹ and G. Beitel²,¹Semiconductor Company, Toshiba Corporation and ²Infineon Technologies Japan K.K., Japan

P10-5
High performance Pt/SrBi₂Ta: O₃/HfO₂/Si structure for 1T ferroelectric random access memory
D.-Y. Wang¹, C.-H. Chien², M.-J. Yang², P. Lehnen³, C.-C. Leu², S.-H. Chung², T.-Y. Huang¹ and C.Y. Chang¹,¹National Chiao Tung Univ., ²National Nano Device Labs and ³AIXTRON AG, Germany

P10-6
Improvement in Read Endurance of Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode
D.K. Tran¹ and S. Horita¹,¹JAIST, Japan

P10-7
A Novel Sensing Circuit for High Speed Synchronous MRAM
H. Kim¹, S. Lee¹, S. Lee¹, H. Shin¹ and D. Kim²,¹Ewha Womans Univ. and ²Kookmin Univ., Korea

P10-8
Electrical Characterization Sub-micron MTJ Cells Using SPM
S. Park¹, J. Heo¹, I. Chung¹ and T. Kim²,¹SungKyunKwan Univ. and ²Samsung Advanced Inst. of Technology, Korea

P10-9
Highly Anisotropic and Corrosion-less PtMn Etching using Negative Ions in Pulse-Time-Modulated Chlorine Plasma
S. Kumagai¹, T. Shiraiwa² and S. Samukawa¹,¹Tohoku University and ²Micro Systems Network Company, Sony Corporation, Japan

P11
**SiGe/III-V/III-N Devices
and Circuits for Wireless
and Optical
Communications**
(4 Papers)

P11-1
Balanced-type Peak Power Injection Amplifier for Simultaneous High Efficiency and Large Saturation Power
K. Iyomasa¹, M. Nakayama¹, K. Horiguchi¹, Y. Ikeda¹ and Y. Sakai¹,¹Mitsubishi Electric Corporation, Japan

P11-2
Indium Content Dependence of Electron Velocity and Impact Ionization in InAlAs/InGaAs Metamorphic HEMTs
H. Ono¹, S. Taniguchi¹ and T. Suzuki¹,¹Sony Corporation and ²AIST, Japan

P11-3
Two-Step Electrode Self-Aligned Process of InP-based RTDs for Highly Integrated RTD/HEMT Circuits
T. Ohki¹, N. Okamoto¹, T. Takahashi¹, K. Makiyama¹, K. Imanishi¹ and N. Hara¹,¹Fujitsu Labs Ltd., Japan

P11-4

The fabrication of enhancement-mode metamorphic InAlAs/InGaAs HEMT by Pt Schottky metal diffusion
C.-K. Lin¹, J.-C. Wu¹, W.-K. Wang¹, H.-C. Chiu¹ and Y.-J. Chan¹, ¹National Central Univ., Taiwan

P13**Organic Semiconductor Devices and Materials**

(6 Papers)

P13-6

Electrochemical Studies on a Self-Assembled Viologen Monolayer using Quartz Crystal Microbalance
J.-Y. Ock¹, H.-K. Shin¹, D.-J. Qian², J. Miyake² and Y.-S. Kwon¹, ¹Dong-A Univ., Korea and ²Tissue Engineering Research Center, AIST, Japan

P12 System-Level Integration and Packaging Technologies

(3 Papers)

P13-1

Characterization of hydrogen treated Pentacene OTFT
S.-C. Suen¹, W.-T. Whang² and J.-Y. Yang¹, ¹National Nano Device Labs and ²Inst. of Materials Science and Engineering, National Chiao-Tung Univ., Taiwan

P14**Micro-Nano Electromechanical Devices for Bio- and Chemical Applications**

(4 Papers)

P12-1

Effect of High Resistivity Si Substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects
S. Watanabe¹, A.B.M. Harun-ur Rashid¹ and T. Kikkawa¹, ¹RCNS, Hiroshima Univ., Japan

P13-2

Thickness Dependent Device Operation of Sublimed Molecular Field-Effect Transistors
S. Hoshino¹, M. Yoshida¹, S. Uemura¹, T. Kodzasa¹, T. Kamata¹ and K. Yase¹, ¹AIST, Japan

P14-1

Incident Angle Effect on Deep MEMS Structure in Resist Spray Coating Technique
V.K. Singh¹, M. Sasaki¹ and K. Hane¹, ¹Tohoku Univ., Japan

P12-2

Stacked π -type Equivalent Circuit Analysis of Ferromagnetic RF Integrated Inductor
M. Yamaguchi¹, S. Ikeda¹, S. Bae¹, S. Tanabe¹, K. Sugawara² and A. Konrad³, ¹Tohoku Univ., ²Mitsubishi Electric Co., Japan and ³Univ. of Toronto, Canada

P13-3

A Study on Morphology and Electrical Properties of Dendrimer Complex with Pt Ions
K.-H. Jung¹, H.-K. Shin¹, C. Kim¹ and Y.-S. Kwon¹, ¹Dong-A Univ., Korea

P14-2

A High Resolution Hemoglobin Measurement Cell Integrated with Signal Processing Circuit
T. Noda¹, T. Hidekuni¹, M. Ashiki¹, H. Ebi², K. Sawada¹ and M. Ishida¹, ¹Toyohashi Univ. of Technology and ²HORIBA Ltd., Japan

P12-3

A Study of ESD Protection under Pad Design for Copper-Low K VLSI Circuits
J.-W. Lee¹, A. Chao¹, Y. Li^{1,2} and H. Tang³, ¹National Nano Device Labs, ²National Chiao Tung Univ. and ³United Microelectronics Corporation, Taiwan

P13-4

High Resolution Periodical Structure Fabricated by Laser Machining in Photosensitive Polymers
S. Shibata¹, O. Sugihara², N. Okamoto³ and T. Kaino², ¹Shizuoka Univ., ²Tohoku Univ. and ³Shizuoka Univ., NEDO, Japan

P14-3

Vertically Buckled Bridges for Three-Dimensional SOI-MEMS
M. Sasaki¹, D. Briand², W. Noell² and N. de Rooij², ¹Tohoku Univ. and ²Univ. of Neuchatel, Japan

P13-5

Fabrication of a Photoelectrochemical Cell Using a Self-Assembled Monolayer of Tris(2,2'-bipyridine)ruthenium(II)-Viologen Linked Thiol on Multistructured Gold Nanoparticles
N. Terasaki¹, K. Otsuka², T. Akiyama² and S. Yamada², ¹AIST and ²Kyushu Univ., Japan

P14-4

An Investigation on The Mechanism of EHD Phenomena in High Intensity and Asymmetric Electric Field
S. Suzuki¹, T. Nakasone¹ and K. Ishikawa¹, ¹SEIKEI Univ., Japan

Thursday, September 18

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>A-7: Advanced Silicon Devices and Device Physics -High-k Technology II- (9:00-10:30) Chairs: K. Shibahara (Hiroshima Univ.) M. Ogawa (Kobe Univ.)</p>	<p>B-7: Silicon Process / Materials Technologies -Metal Gate, Gate Oxide- (9:00-10:20) Chairs: T. Arikado (Selete) K. Suguro (Toshiba)</p>	<p>C-7: Organic Semiconductor Devices and Materials -Organic Thin Film Transistor- (9:15-10:30) Chairs: T. Kamata (AIST) S. Shiratori (Keio Univ.)</p>	<p>D-7: New Materials and Characterization -Carbon Nanotube Devices and Materials- (9:20-10:30) Chairs: Y. Awano (Fujitsu Labs.) Y. Ochiai (NEC)</p>	<p>E-7: Novel Devices, Physics, and Fabrication -Novel Materials and Devices- (9:30-10:30) Chairs: Y. Kuwahara (Osaka Univ.) H. Yamaguchi (NTT)</p>	<p>F-7: Optoelectronic Devices and Photonic Crystal Devices -Photonic Crystal Devices I- (9:00-10:30) Chair: N. Yokouchi (Furukawa Electric) T. Baba (Yokohama National Univ.)</p>	<p>G-7: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -III-V Devices & Circuits- (9:00-10:30) Chairs: Y. Taten (Fujitsu Quantum Devices Limited) Yi-J. Chan (Natl. Central Univ.)</p>
<p>9:00 A-7-1 (Invited) High-k/Oxynitride Gate Dielectric-Searching for Serendipitous Materials- M. Hiratani¹, S. Saito¹, Y. Shimamoto¹, S. Tsujikawa¹, Y. Matsui¹, O. Tonomura¹, K. Torii¹, J. Yugami¹, and S. Kimura¹, ¹Hitachi, Ltd., Japan</p>	<p>9:00 B-7-1 Low TinV (≤ 1.8 nm) Metal-Gated MOSFETs on SiO₂ Based Gate Dielectrics for High Performance Logic Applications V. Ku¹, R. Amos¹, A. Steegen¹, C. Cabral, Jr.¹, V. Narayanan¹, P. Jamison¹, P. Nguyen¹, Y. Li¹, M. Gribelyuk¹, Y. Wang¹, J. Cai¹, A. Callegari¹, F. McFeely¹, F. Jamin¹, K. Wong¹, E. Wu¹, A. Chou¹, D. Boyd¹, H. Ng¹, M. Jeong¹, C. Wann¹, R. Jammy¹ and W. Haensch¹, V. Ku¹, R. Amos¹, C. Cabral, Jr.¹, V. Narayanan¹, P. Jamison¹, P. Nguyen¹, Y. Li¹, M. Gribelyuk¹, Y. Wang¹, J. Cai¹, A. Callegari¹, F. McFeely¹, F. Jamin¹, K. Wong¹, E. Wu¹, A. Chou¹, D. Boyd¹, H. Ng¹, M. Jeong¹, C. Wann¹, R. Jammy¹, and W. Haensch¹, ¹IBM, USA</p>	<p>9:15 C-7-1 (Invited) Towards Printed Organic Electronics; Semiconductor Materials Design for Plastic Transistors B.S. Ong¹, ¹Xerox Research Centre of Canada, Canada</p>	<p>9:20 D-7-1 Characteristics of a Carbon Nanotube FET Analyzed as a Ballistic Nanowire FET Y. Kimura¹, T. Shimizu¹ and K. Natori^{1,2}, ¹Univ. of Tsukuba and ²CREST-JST, Japan</p>	<p>9:20 E-7-1 Solid-electrolyte nanometer switch T. Sakamoto^{1,2}, H. Sunamura^{1,2}, H. Kawaura^{1,2}, T. Hasegawa^{2,3}, T. Nakayama^{2,3} and M. Aono^{2,3}, ¹Fundamental Research Labs., NEC Corp., ²SORST, JST and ³NIMS, Japan</p>	<p>9:00 F-7-1 (Invited) 3D Photonic Crystal as a Novel Dielectric Material S. Kawakami¹, T. Kawashima², T. Sato^{1,2}, T. Aoyama², W. Ishikawa², Y. Ohtera¹, H. Ohkubo¹, Kenta Miura¹, and Y. Honma² ¹Tohoku Univ., ²NICHE, ³Photonic Lattice Inc., Japan</p>	<p>9:00 G-7-1 Over 65% Efficiency 300MHz Bandwidth C-Band Internally-Matched GaAs FET H. Ohtsuka¹, K. Mori¹, H. Yukawa¹, H. Minamide¹, Y. Kittaka¹, T. Tsunoda¹, S. Ogura¹ and T. Takagi¹, ¹Mitsubishi Electric Corporation, Japan</p>
<p>9:30 A-7-2 Effect of Coulomb Scattering on Stress-Induced Mobility Degradation in nMOSFETs with HfAlO_x/SiO₂ Dielectrics W. Mizubayashi¹, N. Yasuda², H. Hisamatsu², H. Ota¹, K. Tominaga², K. Iwamoto², K. Yamamoto², T. Horikawa¹, T. Nabatame² and A. Toriumi^{1,2}, ¹MIRAI-ASRC, ²MIRAI-ASET and ³The Univ. of Tokyo, Japan</p>	<p>9:20 B-7-2 New Dual Metal Gate by Using WSix for nMOS and Pt-alloyed WSix for pMOS K. Matsuo¹, O. Arisumi¹ and S. Kyoichi¹, ¹Toshiba Corporation, Japan</p>	<p>9:45 C-7-2 Self-Alignment Organic Field-Effect Transistor using Back-Side Exposure Method T. Hyodo¹, F. Morita¹, S. Naka¹, H. Okada¹ and H. Onnagawa¹ ¹Toyama Univ., Japan</p>	<p>9:40 D-7-2 (Invited) Performance Estimation and Benchmarking for Carbon Nanotube FETs and Nanodiode Arrays H.-S.P. Wong¹, G.S. Ditlow¹, P.M. Solomon¹, X. Wang², ¹IBM Research, T.J. Watson Research Center, ²IBM Microelectronics, SRDC</p>	<p>9:45 E-7-2 Piezoresistive Nanomechanical Cantilever based on InAs/AlGaSb Heterostructure L.F. Houlet¹, H. Yamaguchi¹, S. Miyashita² and Y. Hirayama^{1,3}, ¹NTT Basic Research Labs, ²NTT-AT and ³CREST-JST, Japan</p>	<p>9:30 F-7-2 Coupled Waveguide Devices Based on Autocloned Photonic Crystals M. Shirane¹, A. Gomyo¹, K. Miura², Y. Ohtera², H. Yamada¹ and S. Kawakami², ¹NEC Corporation and ²Tohoku Univ., Japan</p>	<p>9:15 G-7-2 High-Performance InP HBTs with a Composite Collector K. Kurishima¹, M. Ida¹, K. Ishii¹ and N. Watanabe¹, ¹NTT Photonics Labs, Japan</p>
<p>9:50 A-7-3 Influence of Dielectric Constant Distribution in Stacked Gate Dielectrics on Electron Mobility in Inversion Layers M. Ono¹, T. Ishihara¹ and A. Nishiyama¹, ¹Toshiba Corporation, Japan</p>	<p>9:40 B-7-3 Highly Selective Etching of Ta/TaNx Metal Electrode on Si₃N₄ Gate Dielectric Employing SiCl₄-NF₃ Gas Mixture Plasma H. Shimada¹ and K. Maruyama¹, ¹SEIKO EPSON Corp., Japan</p>	<p>10:00 C-7-3 A Water-Soluble Photolithography Process and the Application to OTFT Fabrication C.K. Song¹ and K.H. Kim¹, ¹DONG-A University, Korea</p>	<p>10:10 D-7-3 Ultra-low Energy Nitrogen-Irradiation for Improvement of Carbon Nanotube Channel Single Electron Transistor T. Kamimura^{1,4}, K. Yamamoto² and K. Matsumoto^{3,4}, ¹Univ. of Tsukuba, ²AIST, ³Osaka Univ. and ⁴CREST/JST, Japan</p>	<p>10:00 E-7-3 InP hot electron transistors modulated by gate electrodes sandwiching emitter mesa K. Takeuchi¹, H. Maeda¹, R. Nakagawa¹, Y. Miyamoto^{1,2} and K. Furuya^{1,2}, ¹Tokyo Inst. of Technology and ²CREST-JST, Japan</p>	<p>9:45 F-7-3 Reflection Characteristics of Coupled Defect Waveguides in Photonic Crystals T. Katsuyama^{1,2}, K. Hosomi^{1,2}, T. Fukamachi^{1,2} and Y. Arakawa¹, ¹The Univ. of Tokyo, ²Hitachi Ltd., Japan</p>	<p>9:30 G-7-3 A High Reliability and High Gain InP-HEMT with Composite Channel Structure S. Kurachi¹, Y. Nonaka¹ and J. Nikaido¹, ¹Fujitsu Quantum Devices Limited, Japan</p>

Room A	Room B	Room C
10:10 A-7-4 Characterization of Soft Breakdown Effects for Post-deposition NH ₃ Plasma Treated HfO ₂ Gate Dielectrics J.-C. Wang ¹ , D.-C. Shie ¹ , T.-F. Lei ¹ and C.-L. Lee ¹ , ¹ National Chiao Tung Univ., Taiwan	10:00 B-7-4 High Quality Silicon Nitride Film Formed by Microwave-Excited Plasma Enhanced Chemical Vapor Deposition with Dual Gas Shower Head H. Tanaka ¹ , C. Zhong ² , Y. Hayakawa ³ , M. Hirayama ³ , A. Teramoto ³ , S. Sugawa ¹ and T. Ohmi ² , ¹ Tohoku Univ. and ² NICHE, Tohoku Univ., Japan	10:15 C-7-4 Time-of-flight measurement for lateral carrier transport in organic thin films M. Kitamura ¹ , T. Imada ¹ , S. Kako ¹ and Y. Arakawa ¹ , ¹ Univ. of Tokyo, Japan

Room D	Room E	Room F	Room G
	10:15 E-7-4 Single-Electron Transistors with Large-Energy Binary States in a GaN Quantum Dot K. Kawasaki ^{1,2} , Y. Kitaichi ¹ , M. Takeuchi ² and Y. Aoyagi ^{1,2} , ¹ Tokyo Inst. of Technology and ² CREST-JST, Japan	10:00 F-7-4 Enhancement of Cavity-Q in a Quasi-Three Dimensional Photonic Crystal Microcavity M. Ito ¹ , S. Iwamoto ¹ and Y. Arakawa ¹ , ¹ Univ. of Tokyo, Japan	9:45 G-7-4 75-GHz Optical Clock Divide-by-Two OEIC using InP HEMTs and Uni-Travelling-Carrier Photodiode K. Sano ¹ , K. Murata ¹ , H. Matsuzaki ¹ , H. Kitabayashi ¹ , T. Akeyoshi ¹ , H. Ito ¹ , T. Enoki ¹ and H. Sugahara ¹ , ¹ NTT Photonics Labs, Japan
		10:15 F-7-5 Proposal of a Novel Ring Waveguide Device of 2D Photonic Crystal Slab - The Transmittance Simulated by FDTD Analysis - K. Furuya ^{1,2} , N. Yamamoto ¹ , Y. Watanabe ¹ and K. Komori ^{1,2} , ¹ AIST, and ² CREST-JST, Japan	10:00 G-7-5 (Invited) High-Speed III-VHEMT and HBT Devices and Circuits for ETDM Transmission beyond 80 Gbit/s R. Quay ¹ , M. Schlechtweg ¹ , A. Leuther ¹ , M. Lang ¹ , U. Nowotny ¹ , O. Kappeler ¹ , W. Benz ¹ , M. Ludwig ¹ , M. Leich ¹ , R. Driad ¹ , W. Bronner ¹ , and G. Weimann ¹ ¹ Fraunhofer Institut für Angewandte Festkörperphysik

Break

A-8: Advanced Silicon Devices and Device Physics -Advanced CMOS Technology II- (10:45-12:05) Chairs: T. Eimori (Renesas) K. Goto (Fujitsu Labs.)	B-8: Silicon Process / Materials Technologies -Si Process-(10:45-12:05) Chairs: M. Hori (Nagoya Univ.) T. Horikawa (MIRAI-ASRC)	C-8: Organic Semiconductor Devices and Materials -Organic Optics- (10:45-12:00) Chais: K. Kudo (Chiba Univ.) C. Adachi (Chitose Inst. of Sci & Technol.)
10:45 A-8-1 Schottky Barrier Height Reduction and Drive Current Improvement in Metal Source/Drain MOSFET with Strained-Si Channel A. Yagishita ¹ , T.-J. King ² and J. Bokor ³ , ¹ Toshiba Corporation and ² Univ. of California at Berkeley, USA	10:45 B-8-1 Ni-salicyded Poly-Si/poly-SiGe Layered Gate Technology for 65nm-node CMOSFETs A. Muto ¹ , H. Ohji ¹ , T. Maeda ¹ and K. Torii ¹ , ¹ SELETE, Japan	10:45 C-8-1 Electric Field Induced Second Harmonic Generation from Vacuum Evaporated Metal-Phthalocyanine Film/Metal Electrode Interface C.-Q. Li ¹ , T. Manaka ¹ and M. Iwamoto ¹ , ¹ Tokyo Inst. of Technology, Japan

Break

D-8: New Materials and Characterization -High-k Dielectrics I- (10:45-11:25) Chairs: S. Miyazaki (Hiroshima Univ.) K. Torii (Selete)	E-8: Novel Devices, Physics, and Fabrication -Carbon Nanotubes- (10:45-12:00) Chairs: Y. Homma (NTT) F. Nihei (NEC)	F-8: Optoelectronic Devices and Photonic Crystal Devices -Photonic Crystal Devices II- (10:45-11:45) Chair: H. Yamada (NEC) T. Katsuyama (Univ. of Tokyo)	G-8: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -SiGe Technologies- (10:45-11:45) Chairs: K. Washio (Hitachi) N. Suematsu (Mitsubishi Electric)
10:45 D-8-1 Thermal Instability of Poly-Si Gate Al ₂ O ₃ MOSFETs W. Kim ¹ , T. Kawahara ¹ , H. Itoh ¹ , A. Horiuchi ¹ , A. Muto ¹ , T. Maeda ¹ , R. Mitsuhashi ¹ , K. Torii ¹ and H. Kitajima ¹ , ¹ SELETE, Japan	10:45 E-8-1 (Invited) Carbon Nanotube SPM Probe Fabricated by NanoEngineering S. Akita ¹ , and Y. Nakayama ^{1,2} , ¹ Osaka Pref. Univ., ² Osaka Univ., Japan	10:45 F-8-1 (Invited) Semiconductor Photonic Crystal Devices T. Baba ¹ , ¹ Yokohama National Univ., Japan	10:45 G-8-1 (Invited) High-Performance, Low-Cost SiGe:C BiCMOS Technology B. Tillack ¹ , D. Knoll ¹ , B. Heinemann ¹ , K.-E. Ewald ¹ , H. Rucker ¹ , R. Barth ¹ , J. Bauer ¹ , K. Blum ¹ , D. Bolze ¹ , J. Borngreber ¹ , J. Drews ¹ , G. Fischer ¹ , A. Fox ¹ , F. Fuernhammer ¹ , O. Fursenko ¹ , T. Grabolla ¹ , U. Haak ¹ , W. Hoppner ¹ , K. Kopke ¹ , D. Kruger ¹ , B. Kuck ¹ , R. Kurps ¹ , M. Marschmeyer ¹ , H. H. Richter ¹ , D. Schmidt ¹ , P. Schley ¹ , R. Scholz ¹ , W. Winkler ¹ , D. Wolansky ¹ , H.-E. Wulf ¹ , Y. Yamamoto ¹ and P. Zaumseil ¹ , ¹ IHP

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>11:05 A-8-2 Experimental Evidence of Gate-Induced Schottky Barrier Height Lowering Due to Image Force in Gated Schottky Diodes A. Kinoshita¹, K. Uchida¹ and J. Koga¹, ¹Advanced LSI Technology Lab., Toshiba Corp., Japan</p>	<p>11:05 B-8-2 Pre-amorphization and co-implantation suitability for advanced PMOS devices integration R. Surdeanu¹, B. Pawlak¹, R. Lindsay², M. van Dal¹, G. Doornbos¹, C. Dachs¹, Y. Ponomarev¹, J.J. Loo¹, K. Henson², M. Verheijen³, M. Kaiser¹, X. Pages¹, M. Jurczak² and P. Stolk¹, ¹Philips Research Leuven, ²IMEC, ³Philips Research Labs and ⁴ASM International, Eindhoven, Belgium</p>	<p>11:00 C-8-2 Conversion Between Three And Two Dimensional Optical Waves In Attenuated Total Reflection Kretschmann Configuration With Nanostructured Langmuir-Blodgett Films F. Kaneko¹, K. Wakui¹, H. Hatakeyama¹, S. Toyoshima¹, K. Shinbo¹, K. Kato¹, T. Kawakami¹, Y. Ohdaira¹ and T. Wakamatsu², ¹Niigata Univ. and ²Ibaraki National College of Tech., Japan</p>	<p>11:05 D-8-2 W/HF₂ gate stacks with T_{inv}~1.2nm and low charge trapping A. Callegari¹, P. Jamison¹, B.H. Lee², D. Neumayer¹, V. Narayanan¹, S. Zafar¹, E. Gousev¹, C.D. Emic¹, D. Lacey¹, M. Gribelyuk², C. Cabral¹, A. Steegen², V. Ku², R. Amos², Y. Li³, P. Nguyen³, F.Mc. Feely¹, G. Singco¹, J. Cai¹, S-H Ku², Y.Y. Wang², C. Wajda¹, D. O'Meara¹, H. Shinriki¹, and T. Takahashi³, ¹IBM, SRDC, ²IBM T. J. Watson Research Center, and ³Tokyo Electron America</p>	<p>11:15 E-8-2 Top-Gate Carbon-Nanotube Field-Effect Transistors with Very High Intrinsic Transconductance F. Nihey^{1,3}, H. Hongo^{1,3}, Y. Ochiai^{1,3}, M. Yudasaka^{1,2} and S. Iijima^{1,2,3,4}, ¹NEC Corporation, ²JST, ³Japan Fine Ceramics Center, ⁴AIST and ⁵Meijo Univ., Japan</p>	<p>11:15 F-8-2 Ultraviolet Second Harmonic Generation and Sum-Frequency Mixing in Nonlinear-Optical Polymer Photonic-Crystal Waveguides S. Inoue¹, K. Kajikawa¹ and Y. Aoyagi¹, ¹Tokyo Inst. of Technology, Japan</p>	<p>11:15 G-8-2 Base Current Control in Low V_{BE} Operated SiGeC Heterojunction Bipolar Transistors Using SiGe-cap Structure and High Carbon Content Base T. Saitoh¹, T. Kawashima¹, Y. Kanzawa¹, J. S. Iwanaga¹, K. Idota¹, T. Takagi¹, T. Ohnishi¹, K. Yuki¹, T. Sano¹ and S. Sawada¹, ¹Matsushita Electric Industrial Co., Ltd., Japan</p>
<p>11:25 A-8-3 Intelligent BSIM4 Model Parameter Extraction for Sub-100 nm MOSFETs era Y. Li^{1,2} and Y.-Y. Cho¹, ¹National Nano Device Labs, Taiwan and ²National Chiao Tung Univ., Taiwan</p>	<p>11:25 B-8-3 Kinetics of Boron Activation by Flash Lamp Annealing K. Yamashita¹, M. Noguchi¹, H. Nishimori¹, T. Ida¹, M. Yoshioka¹, T. Kusuda¹, T. Arikado¹ and K. Okumura¹, ¹SELETE, ²Ushio Inc, ³Dainippon Screen MFG. Co. Ltd. and ⁴Univ. of Tokyo, Japan</p>	<p>11:15 C-8-3 Low-birefringent slab waveguide fabricated with hot-embossing for sol-gel derived phenyl-methyl silsesquioxane films K. Hasui^{1,2}, M. Tomiki¹ and N. Okamoto¹, ¹Shizuoka Univ., ²Corning Japan K.K, Japan</p>		<p>11:30 E-8-3 Fabrication of Two-Dimensional Carbon Nanostructures Using Radio-Frequency Plasma-Enhanced Chemical Vapor Deposition M. Hiramatsu¹, K. Shiji¹, H. Amano¹, Y. Ando¹ and M. Hori², ¹Meijo Univ. and ²Nagoya Univ., Japan</p>	<p>11:30 F-8-3 Enhanced Light Extraction Efficiency of GaN-Based Blue LED Using Extended-Pitch Surface Photonic Crystal K. Orita, S. Tamura, T. Takizawa, T. Ueda, M. Yuri, S. Takigawa and D. Ueda, ¹Matsushita Electric Industrial Co., Ltd, Japan</p>	<p>11:30 G-8-3 A Low Power SiGe Micromixer for 2.4/5.2/5.7 GHz Multi-band WLAN Applications C.-Y. Wang¹, H.-W. Chiu¹, H.-C. Chen¹, S.-S. Lu¹ and C.-C. Meng¹, ¹National Taiwan University, Taiwan</p>
<p>11:45 A-8-4 0.13μm Low-K/Cu Logic CMOS Based Technology for High Performance Analog Devices J.-C. Guo¹, W.Y. Lien², T.L. Tsai², S.M. Chen², C.M. Wu², Y.C. Sun² and P. Yang², ¹National Chiao Tung Univ. and ²Taiwan Semiconductor Manufacturing Corp., Taiwan,</p>	<p>11:45 B-8-4 High-Speed Damage-Free Contact Hole Etching using Dual Shower Head Microwave-Excited High-Density Plasma Equipment T. Goto¹, H. Yamauchi¹, T. Kato¹, A. Teramoto¹, M. Hirayama¹, S. Sugawa² and T. Ohmi¹, ¹Tohoku Univ. and ²NICHE, Tohoku Univ., Japan</p>	<p>11:30 C-8-4 Waterproof Anti-reflection films fabricated by layer-by-layer adsorption process S. Fujita¹ and S. Shiratori¹, ¹Keio Univ., Japan</p>		<p>11:45 E-8-4 Control of Electrical Property in Multi-Wall Carbon Nanotube using Electrical Breakdown N. Aoki¹, K. Miyamoto¹, N. Oguri¹, T. Sasaki¹, K. Ishibashi² and Y. Ochiai¹, ¹Chiba Univ., ²RIKEN, Japan</p>		
		<p>11:45 C-8-5 Optical Waveguide Characterization of Some Pyroelectric Polymer Thin Films G.K. Tiwari¹, H.V. Tiwary, ¹Ravishankar Shukla Univ., India</p>				

Lunch

Lunch

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>A-9: Advanced Silicon Devices and Device Physics -Electron Mobility Characteristics- (13:30-14:50) Chairs: S. Inaba (Toshiba) N. Sugii (Hitachi)</p>	<p>B-9: Silicon-on-Insulator Technologies -SOI Low Power Applications- (13:30-14:40) Chairs: K. Ino (Toshiba) T. Ipposhi (Renesas)</p>	<p>C-9: Organic Semiconductor Devices and Materials -Molecular Devices and Materials- (13:30-14:45) Chairs: M. Iwamoto (Tokyo Inst. of Technol.) A. Sugimura (Osaka Sangyo Univ.)</p>	<p>D-9: New Materials and Characterization -High-k Dielectrics II- (13:30-14:30) Chairs: T. Nabatame (ASET) Y. Sugita (Fujitsu)</p>	<p>E-9: Novel Devices, Physics, and Fabrication -Si Nanowire and Dots- (13:30-14:30) Chairs: Y. Miyamoto (Tokyo Inst. of Technol.) S. Miyazaki (Hiroshima Univ.)</p>	<p>F-9: Optoelectronic Devices and Photonic Crystal Devices -Ultrafast Photonic Devices- (13:30-14:45) Chairs: N. Suzuki (Toshiba) S. Arahira (Oki Electric)</p>	<p>G-9: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -GaN Devices- (13:30-14:45) Chairs: M. Kuzuhara (NEC) Y. Ohno (Tokushima Univ.)</p>
<p>13:30 A-9-1 Re-Examination on the Universality of Si-MOS Inversion Layer Mobility H. Irie¹, K. Kita², K. Kyuno³, S. Takagi⁴, K. Takasaki⁵, M. Kubota⁶, S. Saito⁷, S. Nishikawa⁸ and A. Toriumi¹, ¹The Univ. of Tokyo and ²STARC, Japan</p>	<p>13:30 B-9-1 (Invited) Ultralow-power CMOS/SOI Circuit Technology for Ubiquitous Communications Y. Kado¹, Y. Matsuya¹, S. Mutoh¹, J. Terada¹, H. Morisawa¹, Y. Sato¹, T. Douseki¹ and H. Kyuragi¹, ¹NTT Microsystem Integration Labs, Japan</p>	<p>13:30 C-9-1 (Invited) Potential Profile and Opto-Electronic Properties at Nano-Interface of Conducting Polymer and Metals K. Kaneto¹ and W. Takashima¹, ¹Kyushu Inst. of Technology, Japan</p>	<p>13:30 D-9-1 Separate and Independent Control of Interfacial Band Alignments and Dielectric Constants in Transition Metal-Rare Earth Oxides G. Lucovsky¹, Y. Zhang¹, J.L. Whitten², D.G. Schlom² and J.L. Freeouf³, ¹North Carolina State Univ., ²Pennsylvania State Univ. and ³Oregon Graduate Inst., USA</p>	<p>13:30 E-9-1 Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate nMOSFETs M. Ikeda¹, Y. Shimizu¹, T. Shibaguchi¹, H. Murakami¹ and S. Miyazaki¹, ¹Hiroshima Univ., Japan</p>	<p>13:30 F-9-1 (Invited) SOA-Based Functional Devices for Future Optical Networks M. L. Nielsen¹, J. D. Buron¹, M. Nord², and M. N. Petersen¹, ¹Research Center COM, Technical Univ. of Denmark, Denmark</p>	<p>13:30 G-9-1 (Invited) GaN-based microwave power devices: A survey on the activities in Europe J. Würfl¹, ¹Ferdinand-Braun-Institut für Hochstfrequenztechnik, Germany</p>
<p>13:50 A-9-2 Channel direction impact of (110) surface Si substrate on performance improvement in sub-100 nm MOSFETs H. Nakamura¹, T. Ezaki¹, T. Iwamoto¹, M. Togo¹, N. Ikarashi¹, M. Hane¹ and T. Yamamoto¹, ¹NEC Corporation, Japan</p>	<p>14:00 B-9-2 On the Performance Advantage of undoped ultra thin-film FD-SOI MOSFETs H. Matsuhashi¹, T. Okamura¹, T. Douseki², N. Miura¹, T. Chiba¹ and S. Baba¹, ¹OKI Electric Industry co., Ltd., and ²NTT Microsystem Integration Labs, Japan</p>	<p>14:00 C-9-2 Effects of different materials use for internal floating electrode on the photovoltaic properties of tandem type organic solar cell K. Triyana¹, T. Yasuda¹, K. Fujita¹ and T. Tsutsui¹, ¹Kyushu Univ., Japan</p>	<p>13:50 D-9-2 Chemical Structures of HfO₂/Si Interfacial Transition Layer H. Nohira¹, Y. Takata¹, K. Kobayashi¹, M.B. Seman¹, S. Joumori¹, K. Nakajima¹, M. Suzuki¹, K. Kimura¹, Y. Sugita¹, O. Nakatsuka¹, A. Sakai², S. Zaima³, T. Ishikawa⁴, S. Shin⁵ and T. Hattori¹, ¹Musashi Inst. of Technology, ²RIKEN, ³JASRI, ⁴Kyoto Univ., ⁵Fujitsu Ltd. and ⁶Nagoya Univ., Japan</p>	<p>13:45 E-9-2 Hybrid Silicon Nanocrystal Silicon Nitride Memory R. Steimle¹, R. Rao¹, B. Hradsky¹, R. Muralidhar¹, M. Sudd¹, M. Ramon¹, S. Straub¹, S. Bagchi¹, X.-D. Wang¹, J. Hooker¹ and B. White¹, ¹Motorola SPS, USA</p>	<p>14:00 F-9-2 100-Gbit/s Full-Rate Operation of PD-EAM Optical Gate for Retiming Function T. Yoshimatsu, S. Kodama, K. Yoshino and H. Ito, ¹NTT Photonics Labs, NTT Corporation, Japan</p>	<p>14:00 G-9-2 Gate Direction of AlGaIn/GaN MODFET's with Low Temperature Coefficient of Threshold Voltage H. Ishida¹, T. Murata¹, T. Matsuno¹, Y. Ikeda¹, Y. Hirose¹, Y. Uemoto¹ and T. Tanaka¹, ¹Matsushita Electric Industrial Co., Ltd., Japan</p>
<p>14:10 A-9-3 Characterization of Plasma Nitridation Impact on Lateral Extension Profile in 50nm N-MOSFET by Scanning Tunneling Microscopy H. Fukutome¹, T. Saiki², M. Hori², T. Tanaka², R. Nakamura² and H. Arimoto², ¹Fujitsu Labs Ltd. and ²Fujitsu Limited, Japan</p>	<p>14:20 B-9-3 A 0.5-V Noise-Shaping A/D Converter Using Low-Threshold FD-SOI Transistors Y. Matsuya¹ and T. Douseki¹, ¹NTT Microsystem Integration Labs, Japan</p>	<p>14:15 C-9-3 Photoinduced Gate Operation and Temperature Dependence in the Coulomb staircase of Organic Single Electron Tunneling Junctions Y. Noguchi¹, T. Manaka¹ and M. Iwamoto¹, ¹Tokyo Inst. of Technology, Japan</p>	<p>14:10 D-9-3 Pulsed-source MOCVD HfO₂ ultrathin film growth optimized by <i>in situ</i> ellipsometry monitoring Y. Tsuchiya¹, M. Endoh¹ and S. Oda¹, ¹Tokyo Inst. of Technology, Japan</p>	<p>14:00 E-9-3 Monte-Carlo Simulation of Single-Electron Nanocrystal Memories J.S. Sim¹, J. Kong¹, J.D. Lee¹ and B.-G. Park¹, ¹Seoul National Univ., Korea</p>	<p>14:15 F-9-3 Semiconductor Dispersion Compensators Based on Asymmetric Coupled Waveguides Y. Lee¹, T. Shiota¹, A. Takei¹, T. Taniguchi¹ and H. Uchiyama¹, ¹Central Research Lab, Hitachi, Ltd., Japan</p>	<p>14:15 G-9-3 AlGaIn/GaN Power HEMT Using Advanced Ohmic Structure with Recessed Ohmic Technique M. Kanamura¹, T. Kikkawa¹, N. Adachi², T. Kimura¹, S. Yokokawa², M. Nagahara², N. Hara¹ and K. Joshin¹, ¹Fujitsu Labs Ltd. and ²Fujitsu Quantum Devices Ltd., Japan</p>
<p>14:30 A-9-4 High Performance Strained Si/SiGe N-channel MOSFETs: Impact of Alloy Composition and Layer Architecture S. Olsen¹, L. Driscoll¹, K. Kwa¹, S. Chattopadhyay¹ and A. O'Neill¹, ¹Univ. of Newcastle, UK</p>		<p>14:30 C-9-4 Thin film transistors with oriented copper phthalocyanine micro-crystals fabricated by physical vapor deposition under DC electric field M. Sakai¹, M. Iizuka¹, M. Nakamura¹ and K. Kudo¹, ¹Chiba Univ., Japan</p>		<p>14:15 E-9-4 Growth of Si Nanowire Using Metal-Induced Lateral Crystallization K. Makhira¹ and T. Asano¹, ¹Kyushu Inst. of Technology, Japan</p>	<p>14:30 F-9-4 Linear and Nonlinear Femtosecond Pulse Propagation through a Quantum Nano-Structure Optical Waveguide Observed with XFROG Spectroscopy N. Tsurumachi^{1,2}, N. Watanabe¹, K. Hikosaka^{1,2}, X.-L. Wang^{1,2}, K. Komori^{1,2}, T. Hattori¹ and M. Ogura^{1,2}, ¹AIST, ²CREST-JST and ³Univ. of Tsukuba, Japan</p>	

Break

Break

Room A	Room B	Room C	Room D	Room E	Room F	Room G
<p>A-10: Advanced Silicon Devices and Device Physics -Poly-Si Device and Sensor- (15:00-16:00) Chairs: N. Sugii (Hitachi) T. Eimori (Renesas)</p>	<p>B-10: Silicon-on-Insulator Technologies -SOI CMOS Technologies- (15:00-16:30) Chairs: Y. Kado (NTT) M. Terauchi (Hiroshima City Univ.)</p>	<p>C-10: Organic Semiconductor Devices and Materials -Electroluminescent Devices and Materials- (15:00-16:00) Chairs: Y. Ohmori (Osaka Univ.) K. Kaneto (Kyushu Inst. of Technol.)</p>	<p>D-10: New Materials and Characterization -High-k Dielectrics III- (15:00-16:20) Chairs: M. Hiratani (Hitachi) H. Watanabe (NEC)</p>	<p>E-10: Novel Devices, Physics, and Fabrication -Quantum Computing Devices- (15:00-16:15) Chairs: K. Ishibashi (RIKEN) Y. Pashkin (NEC)</p>	<p>F-10: Optoelectronic Devices and Photonic Crystal Devices -New Photonic Materials- (15:00-16:00) Chair: O. Wada (Kobe Univ.) T. Mizumoto (Tokyo Inst. of Technol.)</p>	<p>G-10: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications -High Voltage Devices- (15:00-16:00) Chairs: K. Morizuka (Toshiba) T. Enoki (NTT)</p>
<p>15:00 A-10-1 High Performance Poly-Si Device with Thin Gate Oxide Film Grown by Plasma Oxidation Technology F. Imaizumi¹, T. Hayashi¹, K. Ishii², A. Teramoto¹, M. Hirayama¹, S. Sugawa² and T. Ohmi¹, ¹NICHE, Tohoku Univ. and ²Tohoku Univ., Japan</p>	<p>15:00 B-10-1 (Invited) Quality Comparison of Commercial Silicon-on-Insulator Wafers by Photoluminescence M. Tajima¹, ¹Inst. of Space and Astronautical Science</p>	<p>15:00 C-10-1 Analysis of a charged bio molecular particle passing through semi conductive ion channel on biological membrane H. Hirayama¹, ¹Asahikawa medical college, Japan</p>	<p>15:00 D-10-1 Molecular Dynamic Simulation on the Crystallization of HfO₂, Hf-aluminate, and Hf-silicate Y. Kosaka¹, T. Yamasaki¹ and C. Kaneta¹, ¹Fujitsu Labs Limited², Japan</p>	<p>15:00 E-10-1 (Invited) Quantum Oscillations in Two Coupled Charge Qubits Y. Pashkin¹, T. Yamamoto^{1,2}, O. Astafiev¹, Y. Nakamura^{1,2}, D. Averin¹, and J.-S. Tsai^{1,2}, ¹RIKEN, ²NEC Corporation, ³State Univ. of New York, USA</p>	<p>15:00 F-10-1 Intersubband Transition Based on a Novel II-VI Quantum Well Structure for Ultrafast All-optical Switching R. Akimoto¹, B. Li¹, F. Sasaki¹ and T. Hasama¹, ¹AIST, Photonics Research Inst., Japan</p>	<p>15:00 G-10-1 (Invited) Development of AlGaIn/GaN power HFET for the application of an inverter circuit S. Yoshida¹, ¹Yokohama R&D Labs, The Furukawa Electric Co., Ltd., Japan</p>
<p>15:20 A-10-2 A Novel High Performance Power MOSFET with Split Well and Split Poly Structure F.-T. Chien¹, K.-W. Tu², S.-T. Su¹, C.-L. Cheng¹, J.-H. Dung¹, C.-Y. Kung² and Y.-C. Huang², ¹Feng Chia Univ., ²Chung Hsing Univ. and ³R&D Dept., Chino-Excel Technology Corp., Taiwan</p>	<p>15:30 B-10-2 Low-Noise and High-Frequency 0.10μm body-tied SOI-CMOS Technology with High-Resistivity Substrate for Low-Power 10Gbps Network LSI T. Iwamatsu¹, M. Tujiuchi¹, Y. Hirano¹, T. Matsumoto¹, H. Takashino¹, T. Ikeda¹, T. Yoshimura², D. Chen², T. Oka², H. Kondoh², T. Ipposhi¹, S. Maegawa¹, Y. Inoue¹, M. Inuishi¹ and Y. Ohji¹, ¹Renesas Technology Corp and ²Mitsubishi Electric Corporation, Japan</p>	<p>15:15 C-10-2 Fabrication and Characteristics of Increased Efficiency of Layered Polymeric Electroluminescent Diodes Y. Hino¹, M. Yamazaki¹, H. Kajii¹ and Y. Ohmori¹, ¹Osaka Univ, CRCast, Japan</p>	<p>15:20 D-10-2 Theoretical Analysis of Oxygen Diffusion in monoclinic HfO₂ M. Ikeda¹, G. Kresse², T. Nabatame¹ and A. Toriumi^{1,4}, ¹MIRAI ASET, ²Universitaet Wien, ³MIRAI AIST and ⁴Univ. of Tokyo, Japan</p>	<p>15:30 E-10-2 Measurement of Two-Qubit States detected by Quantum Point Contacts T. Tanamoto¹ and H. Xuedong², ¹Toshiba Corporation and ²Univ. at Buffalo, SUNY, USA, Japan</p>	<p>15:15 F-10-2 Control of In.Ga_{1-x}As Capping Layer Induced Optical Polarization in Edge-Emitting Photoluminescence of InAs Quantum Dots J. Pachamuthu¹, H. Tanaka¹, T. Kita¹, O. Wada¹, H. Ebe², M. Sugawara², J. Tatebayashi², Y. Arakawa², Y. Nakata² and T. Akiyama², ¹Kobe Univ., ²Research Centre for Advanced Science and Technology, Univ. of Tokyo and ³Fujitsu Labs Ltd., Japan</p>	<p>15:30 G-10-2 Si/SiGe Heterojunction Collector for Low Loss Operation of Carrier Stored Trench-Gate Bipolar Transistor T. Kudoh¹ and T. Asano¹, ¹Center for Microelectronic Systems, Kyushu Inst. of Technology, Japan</p>
<p>15:40 A-10-3 Optimization of The Ultra-Low Dark Current CMOS Image Sensor Cell Using n+ Ring Reset P.-H. Huang¹ and Y.-C. King¹, ¹STAR, National Tsing-Hua Univ., Taiwan</p>	<p>15:50 B-10-3 Fully Depleted SOI CMOS Device with Raised Source/Drain for 90nm Embedded SRAM Technology M.-H. Oh¹, C.-H. Park¹, H. S. Kang¹, C.-B. Oh¹, Y.-W. Kim¹ and K.-P. Suh¹, ¹Samsung Electronics, Korea</p>	<p>15:30 C-10-3 Passivation of organic light emitting diodes with plasma polymerized p-xylene thin films deposited by PECVD S. Sohn¹, S. Kho¹ and D. Cho¹, ¹Sungkyunkwan Univ., Physics, Korea</p>	<p>15:40 D-10-3 Etching yields of HfO₂ under Ar⁺ and CF_x⁺ (X = 1, 2, 3) ion beam irradiation K. Karahashi¹, N. Yamagishi¹, T. Horikawa¹ and A. Toriumi^{1,2}, ¹MIRAI ASET, ²MIRAI ASRC, AIST and ³Univ. of Tokyo, Japan</p>	<p>15:45 E-10-3 Coherent control in inhomogeneously broadened quantum dots ensemble and its coherent transient phenomena N. Tsurumachi^{1,2}, K. Komori^{1,2} and T. Hattori¹, ¹AIST, ²CREST-JST and ³Inst. of Applied Physics, Univ. of Tsukuba, Japan</p>	<p>15:30 F-10-3 High Performance Electroluminescence from Nanocrystalline Si with Carbon Buffer B. Gelloz¹ and N. Koshida¹, ¹Tokyo Univ. Agr. & Tech., Japan</p>	<p>15:45 G-10-3 Design and Demonstration of High Breakdown Voltage GaN-HEMT using Field Plate Structure for Power Electronics Applications W. Saito¹, Y. Takada², M. Kuraguchi², K. Tsuda², I. Omura¹ and T. Ogura¹, ¹Toshiba Corporation, Semiconductor Company and ²Toshiba Corporation, Research & Development Center, Japan</p>
<p>16:10 B-10-4 Body Contact Structure using Elevated Field Insulator for Ultra-Thin Film SOI-MOSFETs S. Yamagami¹, R. Koh¹, H. Wakabayashi¹, J.-W. Lee¹, Y. Saito², A. Ogura¹, M. Narihira¹, K. Arai¹, H. Takemura¹, Y. Ochiai¹, K. Takeuchi¹ and T. Mogami¹, ¹Silicon Systems Research Labs, NEC Corporation and ²R&D Technical Support Center, NEC Corporation, Japan</p>	<p>15:45 C-10-4 High efficiency fluorescent organic light emitting devices utilizing a phosphorescent sensitizer S. Liu¹, ¹Jilin Univ., China</p>	<p>16:00 D-10-4 Selective Dry Etching of HfO₂ in CF₄, Cl₂ and HBr Based Chemistry T. Maeda¹, H. Ito¹, R. Mitsuhashi¹, A. Horiuchi¹, T. Kawahara¹, A. Muto¹, T. Sasaki¹, K. Torii¹ and H. Kitajima¹, ¹Semiconductor Leading Edge Technologies, Inc., Japan</p>	<p>16:00 E-10-4 Observation of the spin-related even-odd effect in single-wall carbon nanotube quantum dots H. Maki¹, M. Suzuki¹, Y. Ishiwata¹ and K. Ishibashi¹, ¹RIKEN, Japan</p>	<p>15:45 F-10-4 Optical Component Coupling Using Self-Written Waveguides N. Hirose¹ and O. Ibaragi¹, ¹ASET, Japan</p>		

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Online paper submission:
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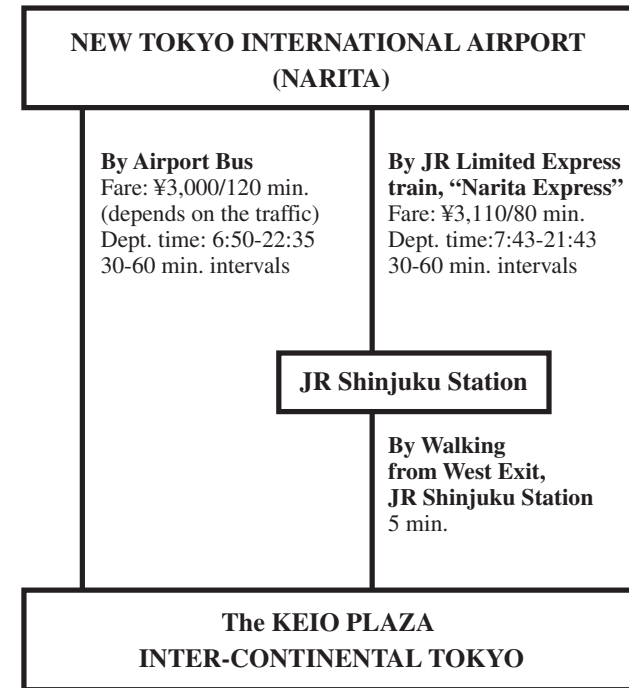
K. Shibahara (Hiroshima Univ.)

Online registration:

M. Hiratani (Hitachi)

SECRETARIAT

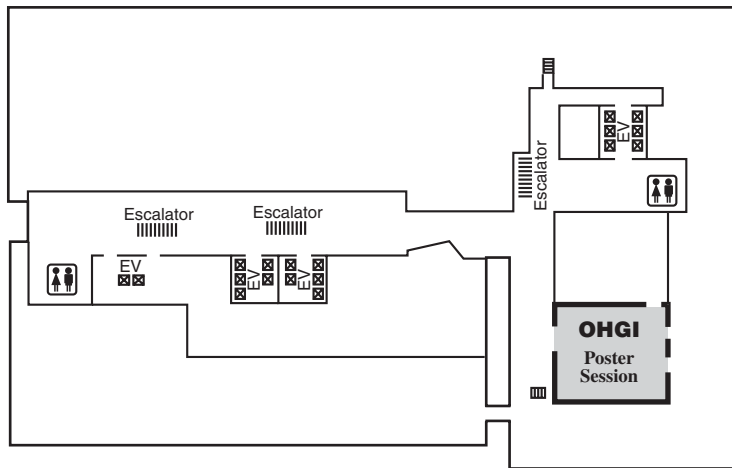
c/o Inter Group Corp.
 4-9-17, Akasaka, Minato-ku,
 Tokyo 107-8486 Japan
 TEL:+81-3-3479-5131
 FAX:+81-3-3423-1601
 E-mail: ssdm@intergroup.co.jp
 Web Site: <http://www.intergroup.co.jp/ssdm>



SSDM 2003 Floor Map, Keio Plaza Inter-Continental Tokyo

Poster Room

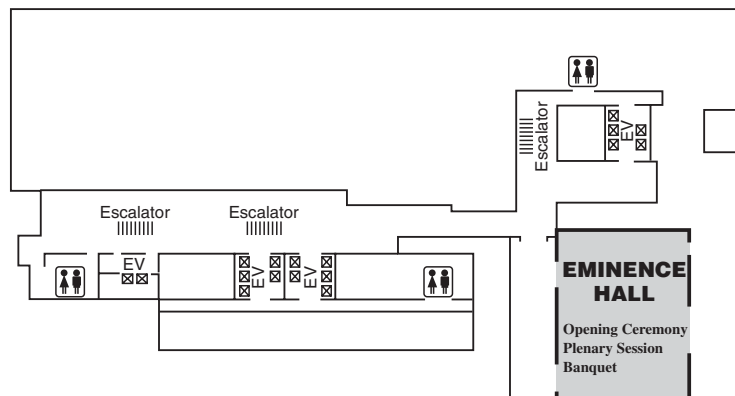
4F



Eminence Hall

5F

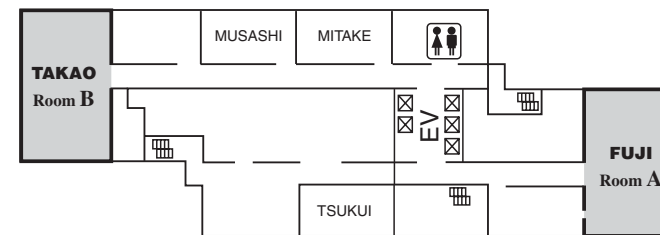
Opening Ceremony
Plenary Session
Banquet



SSDM 2003 Floor Map, Keio Plaza Inter-Continental Tokyo

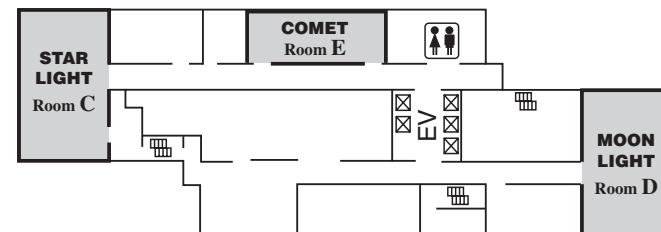
Conference Room A, B

42F



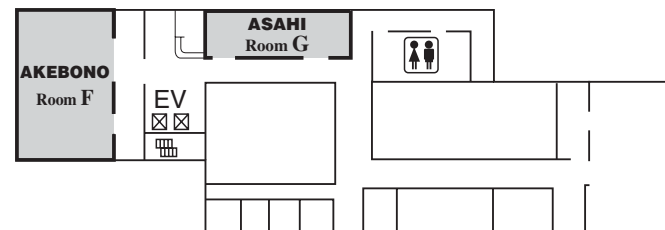
Conference Room C, D, E

43F



Conference Room F, G

47F



Access to the Keio Plaza Inter-Continental Tokyo from Shinjuku Station



徒歩 [On Foot]

●上記地図参照 ●See the map

新宿(西口)・Shinjuku Sta. (West Exit) → 5分・5min. → 京王プラザホテル・Keio Plaza Inter-Continental Tokyo

地下鉄 [Subway]

●都営大江戸線170円 ●Oedo Line 170 YEN

新宿・Shinjuku Sta. → 2分・2min. → 都庁前・Tocho-Mae Sta. A-1番出口から徒歩1分・Exit #A-1,1min.walk

タクシー [Taxi]

●約700円 ●Approx. 700 YEN

新宿(西口) Shinjuku Sta. (West Exit) → 7分・7min. → 京王プラザホテル Keio Plaza Inter-Continental Tokyo