

Friday, September 15

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 7: Photonic Devices and Device Physics	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 10: Organic Materials Science, Device Physics, and Applications		Area 4: Advanced Memory Technology	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 3: CMOS Devices/Device Physics	Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 1: Advanced Gate Stack/Si Processing Science
A-7: Novel Devices and Materials I (9:00-10:30) Chairs: H. Mizuta (Tokyo Tech) Y. Suda (Tokyo Univ. of Agriculture & Technology)	B-7: Micro-Optics and Optical Waveguides (9:00-10:30) Chairs: L. Young (Hitachi) S. Nishikawa (Mitsubishi Electric)	C-7: Micro and Nano Fluidics for Biosensing (9:00-10:30) Chairs: Y. Takamura (JAIST) H. Oana (Univ. of Tokyo)	D-7: Molecular Electronics (9:15-10:30) Chairs: T. Someya (Univ. of Tokyo) K. Kato (Niigata Univ.)		F-7: Flash Memory II (9:00-10:20) Chairs: C. Hsu (eMemory Tech.) Y. Yamauchi (Sharp)	G-7: Characterization II (9:00-10:40) Chairs: M. Kodera (Toshiba) M. Matsuura (Renesas)	H-7: Compact Modeling (9:00-10:40) Chairs: A. Asenov (Univ. of Glasgow) K. Kurimoto (Matsushita Electric)	I-7: Novel Materials (9:00-10:15) Chairs: S. Shimomura (Ehime Univ.) D. Iwai (Fujitsu Labs.)	J-7: High-k Dielectrics II (9:00-10:40) Chairs: Y. Nara (Selete) A. Toriumi (Univ. of Tokyo)
9:00 A-7-1 (Invited) Semiconductor Nanowire Devices for Future Logic and Memory B. Yu and M. Meyyappan, <i>NASA Ames Research Center, USA</i>	9:00 B-7-1 (Invited) Optoelectronic Tweezers: Optical Manipulation Using LEDs and Spatial Light Modulators M. C. Wu, <i>Univ. of California Berkeley, USA</i>	9:00 C-7-1 (Invited) Digital Microfluidics for Chemical and Biological Applications R. L. Garrell, <i>Univ. of California Los Angeles, USA</i>			9:00 F-7-1 The incorporation effect of thin Al ₂ O ₃ layers on ZrO ₂ -Al ₂ O ₃ nanolaminates in the composite oxide-high-K-oxide stack for the floating gate flash memory devices M. S. Joo, S. R. Lee, H. Yang, K. Hong, S. A. Jang, J. Koo, J. Kim, S. Shin, M. Kim, S. Pyi, N. Kwak and J. W. Kim, <i>Hynix Semiconductor Inc., Korea</i>	9:00 G-7-1 Late News	9:00 H-7-1 Suppressed short-channel effect of DG-MOSFET and its modeling H. Oka ¹ , R. Tanabe ¹ , N. Sadachika ² , A. Yumisaki ² and M. Miura-Mattausch ² , ¹ <i>Fujitsu Labs., Ltd. and</i> ² <i>Hiroshima Univ., Japan</i>	9:00 I-7-1 Epitaxial growth of La _{0.7} Ba _{0.3} MnO ₃ thin films on SrTiO ₃ and LaAlO ₃ substrates by metal-organic deposition process K. Daoudi, T. Tsuchiya, T. Nakajima, I. Yamaguchi, T. Manabe and T. Kumagai, <i>AIST, Japan</i>	9:00 J-7-1 Optimization of Hafnium Zirconate (HfZrOx) Gate Dielectric for Device Performance and Reliability R. I. Hegde, D. H. Triyoso, S. Kalpat, S. B. Samavedam, J. K. Schaeffer, E. Luckowski, C. Capasso, D. C. Gilmer, M. Raymond, D. Roan, J. Nguyen, L. La, E. Hebert, X. D. Wang, R. Gregory, R. S. Rai, J. Jiang, T. Y. Luo and B. E. White Jr <i>Jr. White, ASTS, USA</i>
9:30 A-7-2 Charge Polarity Dependence of Negative Differential Conductance in Room-Temperature Operating Silicon Single-Charge Transistor M. Kobayashi, K. Miyaji and T. Hiramoto, <i>Univ. of Tokyo, Japan</i>	9:30 B-7-2 Novel Opto-Electro Printed Circuit Board with Polynorborene Optical Waveguide M. Fujiwara ^{1,2} , Y. Shirato ¹ , H. Owari ¹ , K. Watanabe ¹ , M. Matsuyama ¹ , K. Takahama ¹ , T. Mori ¹ , K. Miyao ¹ , K. Choki ¹ , T. Fukushima ² , T. Tanaka ³ and M. Koyanagi ² , ¹ <i>Sumitomo Bakelite Co., Ltd. and</i> ² <i>Tohoku Univ., Japan</i>	9:30 C-7-2 DNA Size Separation Employing Quartz Nano-Pillars with Different Allocations R. Ogawa ¹ , N. Kaji ² , S. Hashioka ¹ , Y. Baba ^{2,3} and Y. Horiike ¹ , ¹ <i>NIMS, Nagoya Univ. and</i> ² <i>AIST, Japan</i>			9:20 F-7-2 High-k HfO ₂ /Al ₂ O ₃ nanolaminated charge trapping layers for high performance flash memory device applications S. Maikap ¹ , P. J. Tzeng ¹ , T. Y. Wang ² , C. H. Lin ¹ , H. Y. Lee ¹ , C. C. Wang ¹ , L. S. Lee ¹ , J. R. Yang ² and M. J. Tsai ¹ , ¹ <i>Industrial Technology Research Inst. and</i> ² <i>National Taiwan Univ., Taiwan</i>	9:20 G-7-2 CuAl Alloy Interconnects as a Solution to the Trade-off between Reliability and Defect Density T. Furusawa ¹ , D. Kodama ¹ , H. Miyazaki ¹ , M. Matsumoto ¹ , J. Izumitani ¹ , H. Matsumoto ² , S. Fukui ¹ , K. Hashimoto ¹ , S. Tawa ¹ , Y. Nagaki ² , M. Okada ¹ , K. Tomita ¹ , A. Ishii ¹ , N. Amou ² , K. Mori ¹ , K. Maekawa ¹ , Y. Minoura ³ , N. Suzumura ¹ , K. Honda ¹ , Y. Hirose ¹ and A. Osaki ¹ , ¹ <i>Renesas Technology Corp.,</i> ² <i>Renesas Semiconductor Engineering Corp. and</i> ³ <i>Ltec Corp., Japan</i>	9:20 H-7-2 A Continuous, Explicit Drain-Current Model for Asymmetric Undoped Double-Gate MOSFETs Z. M. Zhu ¹ , X. Zhou ¹ , K. Chandrasekaran ¹ , G. H. See ¹ and S. C. Rustagi ² , ¹ <i>Nanyang Technological Univ. and</i> ² <i>Inst. of Microelectronics, Singapore</i>	9:15 I-7-2 Molecular Dynamics and Quantum Chemical Molecular Dynamics Approach to Design of MgO Protecting Layer in Plasma Display M. Kubo ^{1,2} , H. Kikuchi ¹ , H. Tsuboi ¹ , M. Koyama ¹ , A. Endou ¹ , H. Takaba ¹ , C. A. del Carpio ¹ , H. Kajiyama ³ and A. Miyamoto ¹ , ¹ <i>Tohoku Univ.,</i> ² <i>JST-PRESTO and</i> ³ <i>Univ. of Tokyo, Japan</i>	9:20 J-7-2 Current Transportation Mechanism and Interface States Characterization of Sputtered Gd ₂ O ₃ Gate Dielectrics for ULSI Application W. C. Wu ¹ , C. S. Lai ² , K. T. Wang ¹ , J. C. Wang ³ and T. S. Chao ¹ , ¹ <i>National Chiao Tung Univ.,</i> ² <i>Chang Gung Univ. and</i> ³ <i>Nanya Technology Corp., Taiwan</i>

Room 411/412 (A)

9:45 A-7-3
High-PVCR Si/Si_{1-x}Gex Planer-Type Resonant Tunneling Diode Formed with Phosphorous doped Quadruple-layer Buffer
H. Maekawa, Y. Sano and Y. Suda, *Tokyo Univ. of Agriculture and Technology, Japan*

10:00 A-7-4

High-Density Floating Nanodots Memory Produced by Cage-Shaped Protein
K. Yamada¹, S. Yoshii¹, S. Kumagai¹, A. Miura², Y. Uraoka², T. Fuyuki² and I. Yamashita^{1,2,3},
¹Matsushita Electric, ²Nara Inst. of Science and Technology and ³CREST, Japan

10:15 A-7-5

Tunnel-coupled double nanocrystalline Si quantum dots integrated into a single-electron transistor
Y. Kawata¹, M. Khalafalla¹, K. Usami¹, Y. Tsuchiya^{1,2}, H. Mizuta^{1,2} and S. Oda^{1,2}, ¹Tokyo Tech and ²SORST-JST, Japan

Room 413 (B)

9:45 B-7-3
Micro-Racetrack Notch Filters Based on InGaAsP/InP High Mesa Optical Waveguides
W. S. Choi¹, D. H. Kim¹, S. Khisa¹, W. Zhao², J. W. Bae², I. Adesida² and J. H. Jang¹, ¹Gwangju Inst. of Science and Technology and ²Univ. of Illinois at Urbana Campaign, Korea

10:00 B-7-4

Fabrication Method of Microlens Array Using Oxidized Porous Silicon Bulk Micromachining and PDMS Replication Molding
S. K. Yeon, M. L. Ha and Y. S. Kwon, *KAIST, Korea*

10:15 B-7-5

Photocell system driven by Mechanoluminescence
N. Terasaki, C. N. Xu, Y. Imai and H. Yamada, *AIST, Japan*

Room 414/415 (C)

9:45 C-7-3
Integrated DNA Purification and Detection Device for Diagnosis of Infection Diseases
S. Hashioka¹, R. Ogawa¹, H. Ogawa² and Y. Horiike¹,
¹NIMS and ²Adbic Incorp., Japan

10:00 C-7-4

RNA Trap using Microfluidic Chip with Taper Shaped Channel
K. Ueno¹, W. Nagasaka¹, Y. Tomizawa¹, Y. Nakamori¹, E. Tamiya¹ and Y. Takamura^{1,2},
¹JAIST, and ²PRESTO, Japan

10:15 C-7-5

Manipulation of DNA Molecules in Nanopores by Electric Field for Porous Silicon Based DNA Microarray Applications
R. Yamaguchi¹, K. Ishibashi¹, K. Miyamoto¹, Y. Kimura^{1,2} and M. Niwano^{1,2},
¹Tohoku Univ. and ²CREST, Japan

Room 416/417 (D)

9:45 D-7-2
Fowler-Nordheim Tunneling in Electromigrated Break Junctions with Porphyrin Derivatives
Y. Noguchi, T. Nagase, R. Ueda, T. Kamikado, T. Kubota and S. Mashiko, *National Inst. of Information and Communications Technology, Japan*

10:00 D-7-3

Effect of UV/ozone Treatment on Nanogap Electrodes for Molecular Devices
T. Goto¹, H. Inokawa², K. Sumitomo¹, M. Nagase¹, Y. Ono¹ and K. Torimitsu¹,
¹NTT Corp. and ²Shizuoka Univ., Japan

10:15 D-7-4

Analysis of hole trapping into pentacene FET by Optical Second Harmonic Generation and C-V measurements
E. Lim, T. Manaka, R. Tamura and M. Iwamoto, *Tokyo Tech, Japan*

Room 418 (E)**Room 419 (F)**

9:40 F-7-3
P-SONOS and N-SONOS Transient Current and Field Modeling for Program and Erase
P. Y. Du and J. C. Guo, *National Chiao Tung Univ., Taiwan*

10:00 F-7-4

Lateral Redistribution and Interactive Impacts of Localized Trapped Charges during Retention Baking in SONOS Memory
H. Pang, L. Pan, L. Sun, D. Wu and J. Zhu, *Tsinghua Univ., China*

Room 501 (G)

9:40 G-7-3
Shear Stress Analyses in Chemical Mechanical Planarization Processing with Cu/porous low-k Structure
M. Kodera¹, Y. Mochizuki², A. Fukuda², H. Hiyama² and M. Tsujimura³,
¹Semiconductor Company, Toshiba Corp, ²Ebara Research Corp. and ³Ebara Corp., Japan

10:00 G-7-4

Effects of Oxidizer in Metal CMP Slurry on Open Circuit Potential Change during Metal Polishing
S. Shima, S. Kamioka, S. Yasuda, H. Nagano, Y. Wada, K. Tokushige, A. Fukunaga and M. Tsujimura, *Ebara Corp., Japan*

10:20 G-7-5

Ionic Conduction Leakage Current in Porous Silica Films
Y. Kayaba¹, K. Kohmura² and T. Kikkawa¹,
¹Hiroshima Univ. and ²Mitsui Chemicals, Inc., Japan

Room 502 (H)

9:40 H-7-3
Surface-Potential-Based MOS-Varactor Model for RF Applications
M. Miyake¹, N. Sadachika¹, D. Navarro¹, Y. Mizukane¹, T. Ezaki¹, M. Miura-Mattausch¹, H. J. Mattausch¹, T. Ohguro², T. Iizuka², M. Taguchi², S. Kumashiro² and S. Miyamoto²,
¹Hiroshima Univ. and ²Semiconductor Technology Academic Research Center, Japan

10:00 H-7-4

Using MASTAR as a Pre-SPICE Model Generator for Early Technology Assessment and Circuit Simulation
F. Boeuf¹, M. Sellier¹, B. Duriez², E. Josse¹, A. Pouydebasque², M. Müller², F. Payet¹, B. Borot¹ and T. Skotnicki¹,
¹STMicroelectronics and ²Philips Semiconductor, France

Room 511/512 (I)

9:30 I-7-3
Amorphous CuxGa_{1-x}O film deposition by ultrahigh vacuum radio frequency magnetron sputtering
H. Ishikawa, N. Takeuchi, N. Okuda, T. Takeuchi and Y. Horikoshi, *Waseda Univ., Japan*

9:45 I-7-4

Development of New Calculation Method for Rare Earth Element and Large Scale Electronic Structure Calculation of Blue Phosphor BaMgAl₁₀O₁₇:Eu²⁺
H. Onuma¹, H. Tsuboi¹, M. Koyama¹, A. Endou¹, H. Takaba¹, M. Kubo^{1,2}, C. A. del Carpio¹, P. Selvam¹ and A. Miyamoto¹,
¹Tohoku Univ. and ²PRESTO, Japan

10:00 I-7-5

MBE Growth of Gd/Fe Multilayer on GaAs(001)
H. Miyagawa, S. Koshihara, N. Takahashi, N. Tsurumachi, H. Shiraoka, K. Matsushita, S. Nakanishi and H. Itoh, *Kagawa Univ., Japan*

Small Auditorium (J)

9:40 J-7-3
The Effect of Nitrogen on Thermal Diffusion in HfO₂-based Gate Dielectrics
N. Takahashi, T. Yamasaki and C. Kaneta, *Fujitsu Labs. Ltd., Japan*

10:00 J-7-4

The Highly Reliable Evaluation of Mobility in an Ultra Thin High-k Gate Stack with an Advanced Pulse Measurement Method
R. Iijima¹, M. Takayanagi², M. Koyama¹ and A. Nishiyama¹,
¹Toshiba Corp. and ²Semiconductor Company, Toshiba Corp., Japan

10:20 J-7-5

Intrinsic Electronically-Active Defects in Transition Metal Elemental Oxides
G. Lucovsky¹, H. Seo¹, L. B. Fleming¹, M. D. Ulrich¹ and J. Luning², ¹North Carolina State Univ. and ²Stanford Synchrotron Radiation Lab., USA

Break

Break

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Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 7: Photonic Devices and Device Physics	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 10: Organic Materials Science, Device Physics, and Applications	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 4: Advanced Memory Technology	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 3: CMOS Devices/Device Physics	Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 1: Advanced Gate Stack/Si Processing Science
A-8: Novel Devices and Materials II (10:45-12:15) Chairs: Y. Takahashi (Hokkaido Univ.) M. Tabe (Shizuoka Univ.)	B-8: All-Optical Switches (10:45-12:00) Chairs: M. Sugawara (Fujitsu Labs.) M. Tokushima (NEC)	C-8: Nano and Bio Sensors I (10:45-12:15) Chairs: K. Sawada (Toyoashi Univ. of Tech.) S. A. Contera (Univ. of Oxford)	D-8: Organic Transistor I (10:45-12:00) Chairs: K. Kudo (Chiba Univ.) M. Iwamoto (Tokyo Tech)	E-8: GaAs FETs and Process Technologies (10:45-12:15) Chairs: Y. J. Chan (National Chiaotung Univ.) S. Tanaka (NEC)	F-8: MRAM/PRAM (10:45-12:25) Chairs: Y. Ohji (Renesas) N. Ishiwata (NEC)	G-8: Special Session I ; Reliability (10:45-12:25) Chairs: S. Ogawa (Selete/Matsushita) Y. Hayashi (NEC)	H-8: Advanced Channel and Substrate Technology (10:45-12:25) Chairs: Y. Momiyama (Fujitsu) K. Takeuchi (NEC)	I-8: Silicon-based Material Systems (10:45-11:45) Chairs: K. Nishi (NEC) H. Yamaguchi (NTT)	J-8: Metal/High-k CMOS (10:45-12:25) Chairs: Y. Tsunashima (Toshiba) O. Faynot (LETI)
10:45 A-8-1 Electrostatic coupling between two double-quantum dots studied by resonant tunneling current G. Shinkai ^{1,2} , T. Fujisawa ^{1,2} , T. Hayashi ¹ and Y. Hirayama ^{1,3,4} , ¹ NTT Corp., ² Tokyo Tech, ³ Tohoku Univ. and ⁴ SORST-JST, Japan	10:45 B-8-1 40G bit/s NRZ wavelength converter with narrow active waveguides and inverted operation T. Hatta ^{1,2,3} , T. Miyahara ^{1,2} , Y. Miyazaki ^{1,2} , K. Takagi ^{1,2} , K. Matsumoto ^{1,2} , T. Aoyagi ^{1,2} , K. Mishina ³ , A. Maruta ³ and K. Kitayama ³ , ¹ OITDA, ² Mitsubishi Electric Corp. and ³ Osaka Univ. Japan	10:45 C-8-1 (Invited) Microchip based Fabrication of Curved Microstructures like Spider in Nature S. H. Lee, <i>Korea Univ., Korea</i>	10:45 D-8-1 Combined Impact of Field and Carrier Concentration on Charge Carrier Mobilities in Amorphous Organic Thin Films C. Madigan and V. Bulović, <i>MIT, USA</i>	10:45 E-8-1 Enhancement Mode GaAs n-MOSFET with High-k Dielectric M. Yakimov ¹ , V. Tokranov ¹ , R. Kambhampati ¹ , S. Koveshnikov ² , W. Tsai ² , F. Zhu ³ , J. Lee ³ and S. Oktyabrsky ¹ , ¹ State Univ. of New York at Albany, ² Intel Corp. and ³ Univ. of Texas at Austin, USA	10:45 F-8-1 Process Integration of Low-Power and High-Speed 16Mb MRAM using Multi-Layer Yoke Wiring Technology T. Kajiyama ¹ , S. Miura ² , Y. Asao ¹ , T. Ueda ¹ , H. Aikawa ¹ , M. Iwayama ¹ , K. Hosotani ¹ , M. Amano ¹ , M. Yoshikawa ¹ , K. Tsuchida ¹ , S. Ikegawa ¹ , T. Kishi ¹ , M. Shimomura ¹ , K. Shimura ² , N. Ohshima ² , H. Hada ² , A. Nitayama ¹ , S. Tahara ² and H. Yoda ¹ , ¹ Toshiba Corp. and ² NEC Corp., Japan	10:45 G-8-1 (Invited) Challenges of Cu Metallization for 45nm and beyond M. H. Tsai, <i>TSMC, Taiwan</i>	10:45 H-8-1 Strained SiGe-On-Insulator N-MOSFET with Silicon Source/Drain for Drive Current Enhancement G. H. Wang ¹ , E. H. Toh ¹ , K. W. Ang ¹ , C. H. Tung ² , A. Du ² , Y. L. Foo ³ , G. Q. Lo ² , G. Samudra ¹ and Y. C. Yeo ¹ , ¹ National Univ. of Singapore, ² Inst. of Microelectronics and ³ Inst. of Materials Research & Engineering, Singapore	10:45 I-8-1 Fabrication of III-V-O-I (III-V on Insulator) structures on Si using micro-channel epitaxy with a two-step growth technique M. Shichijo, R. Nakane, S. Sugahara and S. Takagi, <i>Univ. of Tokyo, Japan</i>	10:45 J-8-1 Highly scalable and WF-tunable Ni(Pt)Si/SiON TOSI-gate CMOS devices obtained in a CMP-less integration scheme M. Muller ¹ , G. Bidal ² , A. Mondot ² , S. Denorme ² , C. Fenouillet-Beranger ¹ , F. Boeuf ² , D. Aime ² , M. Rafik ² , P. Gouraud ² , T. Kormann ¹ , G. Chabanne ² , A. Zauner ¹ , G. Braeckelmann ³ , S. Bonnetier ³ , D. Barge ¹ , C. Laviron ⁴ , A. Toffoli ⁴ , A. Tarnowka ¹ , S. Pokrant ¹ and T. Skotnicki ² , ¹ Philips Semiconductors, ² STMicroelectronics, ³ Freescale Conductors and ⁴ CEA-LETI, France
11:00 A-8-2 Photo Illumination Effect on Single-Electron-Tunneling Current Through a Thin Bicrystal SOI FET R. Nuryadi ¹ , Z. A. Burhanudin ¹ , R. Yamano ¹ , T. Ishino ¹ , Y. Ishikawa ² and M. Tabe ¹ , ¹ Shizuoka Univ. and ² Univ. of Tokyo, Japan	11:00 B-8-2 Improved Waveguide Structure for All Optical Switches based on Intersubband Transition in II-VI Quantum Wells K. Akita ^{1,2} , R. Akimoto ¹ , T. Hasama ¹ , H. Ishikawa ¹ and Y. Takanashi ² , ¹ National Inst. of Advanced Industrial Science and Technology and ² Tokyo Univ. of Science, Japan	11:00 D-8-2 Electric field distribution in organic field effect transistor evaluated by microscopic second harmonic generation T. Manaka, E. Lim, R. Tamura, D. Yamada and M. Iwamoto, <i>Tokyo Tech, Japan</i>	11:00 E-8-2 Investigation of GaAs MOSFETs with Gate Oxide Grown Using Photoelectrochemical Oxidation Method H. Y. Lee ¹ , Y. F. Lin ¹ , M. Y. Wang ¹ and C. T. Lee ² , ¹ National Formosa Univ. and ² National Cheng Kung Univ., Taiwan	11:05 F-8-2 New Magnetic Nano-Dots Memory with FePt Nano-Dots C. K. Yin ¹ , J. C. Bea ² , M. Murugesan ² , M. Oogane ¹ , T. Fukushima ¹ , T. Tanaka ¹ , K. Natori ³ , M. Miyao ⁴ and M. Koyanagi ¹ , ¹ Tohoku Univ., ² JST, ³ Univ. of Tsukuba and ⁴ Kyusyu Univ., Japan	11:05 H-8-2 Ultra-thin Ge-on-Insulator (GOI) Metal S/D p-channel MOSFETs fabricated by low temperature MBE growth T. Uehara, H. Matsubara, S. Sugahara and S. Takagi, <i>Univ. of Tokyo, Japan</i>	11:00 I-8-2 Dynamics of Defects in Strained Silicon, Strained SiGe and Strained Germanium A. Reznicek, S. W. Bedell, J. P. de Souza, K. W. Schwarz, K. E. Fogel, J. A. Ott, H. J. Hovel and D. K. Sadana, <i>IBM Research, USA</i>	11:05 J-8-2 Sub-30 nm P-channel Schottky Source/Drain FinFETs: Integration of Pt ₃ Si FUSI Metal Gate and High-k Dielectric R. T. P. Lee ¹ , K. M. Tan ¹ , A. E. J. Lim ¹ , T. Y. Liow ¹ , G. Q. Lo ³ , G. Samudra ¹ , D. Z. Chi ² and Y. C. Yeo ¹ , ¹ National Univ. of Singapore, ² Inst. of Materials Research and Engineering and ³ Inst. of Microelectronics, Singapore		

Room 411/412 (A)**11:15 A-8-3**

Fabrication of Ge Quantum-dots by Oxidation of Si_{1-x}Ge_x-on-insulator Nanowires and its Applications to Resonant Tunneling Diodes and Single-electron/Single-hole Transistors
W. T. Lai and P. W. Li, *National Central Univ., Taiwan*

11:30 A-8-4

Observation of single-electron pump operation with one gate bias in phosphorous-doped Si wires
D. Moraru¹, Y. Ono², H. Inokawa¹, K. Yokoi¹, R. Nuryadi¹, H. Ikeda¹ and M. Tabe¹,
¹Shizuoka Univ. and ²NTT Corp., Japan

11:45 A-8-5

SET-based Flexible Multi-valued NAND and NOR Gates for Half-Adder
C. K. Lee¹, S. J. Kim¹, S. J. Choi¹, J. H. Hwang¹, R. S. Chung¹, J. J. Lee¹, M. S. Kim¹, S. J. Shin¹, J. B. Choi¹, Y. S. Yu², H. W. Kye³ and B. N. Song³,
¹Chungbuk National Univ., ²Hankyong National Univ. and ³EXCEL Semiconductor Inc., Korea

Room 413 (B)**Room 414/415 (C)****11:15 C-8-2**

First Selective Detection of Proteins Using Top-Gate Carbon Nanotube Field Effect Transistor
M. Abe^{1,2}, K. Murata^{1,2,3}, A. Kojima^{3,4}, Y. Ifuku⁴, M. Shimizu⁵, T. Ataka^{1,2} and K. Matsumoto^{2,3,5,6},
¹Olympus Corp., ²NEDO, ³CREST-JST, ⁴Mitsubishi Kagaku, ⁵AIST and ⁶Osaka Univ., Japan

11:30 C-8-3

High-efficiency cell membrane perforation technique based on self-organized ZnO nanorods
M. Seki, T. Saito and H. Tabata, *Osaka Univ., Japan*

11:45 C-8-4

In-situ Monitoring of DNA Hybridization Using Surface Infrared Spectroscopy
K. Miyamoto¹, R. Yamaguchi¹, K. Ishibashi¹, Y. Kimura^{1,2} and M. Niwano^{1,2}, ¹Tohoku Univ. and ²CREST-JST, Japan

Room 416/417 (D)**11:15 D-8-3**

Organic Static Induction Transistors Based on Pentacene Thin Films with Various Source Electrodes
Y. Watanabe¹, H. Iechi^{1,2} and K. Kudo¹, ¹Chiba Univ. and ²Ricoh Co., Ltd. Japan

11:30 D-8-4

Investigation for hafnium oxide as an insulator layer of organic thin film transistor
C. W. Lin, J. H. Lin and K. C. Liu, *Chang Gung Univ., Taiwan*

11:45 D-8-5

Reduction of Bias-Induced Threshold Voltage Shift in Pentacene Field Effect Transistors by Interface Modification and Molecular Ordering
C. B. Park, T. Nishimura, T. Yokoyama, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*

Room 418 (E)**11:15 E-8-3**

Passivation Effects of 100 nm In_{0.4}AlAs/In_{0.35}GaAs Metamorphic HEMT With Remote PECVD Grown Si₃N₄ Layer
S. Kim, K. Jang, J. Lee, J. Her and K. Seo, *Seoul National Univ., Korea*

11:30 E-8-4

Microwave Performance of Pseudomorphic HEMT with Tunable Field-Plate Voltage
H. C. Chiu and F. T. Chien, *Chang Gung Univ. Taiwan*

11:45 E-8-5

80nm T-Shaped Gate Metamorphic HEMTs fabricated Using Two-Step Gate Recess Process
H. S. Yoon, J. Y. Shim, D. M. Kang, J. Y. Hong and K. H. Lee, *ETRI, Korea*

Room 419 (F)**11:25 F-8-3**

Optimization of Ring Type Electrode Process for High Density PRAM
K. C. Ryoo, Y. J. Song, D. H. Kang, C. W. Jeong, J. H. Kong, J. H. Oh, D. W. Lim, S. S. Park, J. I. Kim, J. H. Kim, J. H. Park, Y. T. Oh, J. S. Kim, J. M. Shin, J. H. Park, K. W. Lee, Y. Fai, G. H. Koh, G. T. Jeong, H. S. Jeong and K. Kim, *Samsung Electronics Co., Ltd, Korea*

11:45 F-8-4

Characteristics Improvement of Phase Change Memory with Programming Pulse Width
D. S. Chao^{1,3}, C. M. Lee¹, Y. C. Chen¹, P. H. Yen¹, D. Y. Wang¹, M. J. Chen¹, S. C. Lo², H. H. Hsu¹, W. H. Wang¹, F. Chen¹, Y. Chuo¹, C. Lien³, M. J. Kao¹ and M. J. Tsai¹, ¹EOL, ²MCL and ³National Tsing Hua Univ., Taiwan

Room 501 (G)**11:15 G-8-2 (Invited)**

Defects in Electroplated Cu and their Impact on Stress Migration Reliability
A. Uedono¹, T. Suzuki², T. Nakamura², T. Ohdaira³ and R. Suzuki³, ¹Univ. of Tsukuba, ²STARC and ³AIST, Japan

11:45 G-8-3

Nondestructive characterization of dielectric stack structures by laser-pulse-generated surface acoustic wave analysis
T. Takimura¹, N. Hata^{1,2}, Y. Shishida³, S. Chikaki³ and T. Kikkawa^{2,4}, ¹ASRC, ²AIST, ³MIRAI-ASRC, ⁴AIST, ⁵MIRAI-ASET and ⁶Hiroshima Univ., Japan

Room 502 (H)**11:25 H-8-3**

Reduction of Parasitic Resistance of Self-Aligned Copper Germanide for Germanium p-MOSFETs
Y. L. Chao and J. C. Woo, *Univ. of California Los Angeles, USA*

11:45 H-8-4

Bendable High-Performance Electronic Devices (Active Transistor, High-Density Interconnect and Passive-MIM Capacitors) on Flexible Organic-Substrate
H. Y. Li¹, L. H. Guo¹, W. Y. Loh¹, L. K. Bera¹, Q. X. Zhang¹, N. Hwang¹, E. B. Liao¹, K. W. Teoh¹, H. M. Chua¹, Z. X. Shen², G. Q. Lo¹, N. Balasubramanian¹ and D. L. Kwong¹, ¹Inst. of Microelectronics and ²Nanyang Technological Univ., Singapore

Room 511/512 (I)**11:15 I-8-3**

Inhomogeneous strain in thin silicon films analyzed by grazing incidence x-ray diffraction
H. Omi¹, T. Kawamura¹, Y. Kobayashi¹, S. Fujikawa², Y. Tsusaka², Y. Kagoshima² and J. Matsui³, ¹NTT Corp., ²Univ. of Hyogo and ³CAST, Japan

11:30 I-8-4

Characterization of Epitaxial Silicon Films Grown by Atmospheric Pressure Plasma Chemical Vapor Deposition at Low Temperatures (450-600°C)
N. Tawara, H. Ohmi, Y. Terai, H. Kakiuchi, H. Watanabe, Y. Fujiwara and K. Yasutake, *Osaka Univ., Japan*

Small Auditorium (J)**11:25 J-8-3**

Effects of Optimization of Gate Edge Profile on sub-45nm Metal Gate High-k Dielectric Metal-Oxide-Semiconductor Field Effect Transistors Characteristics
C. Y. Kang¹, R. Choi¹, S. H. Bae², S. C. Song¹, M. M. Hussain¹, C. Young¹, D. Heh¹, G. Bersuker¹ and B. H. Lee³,
¹SEMATECH, ²Univ. of Texas at Austin and ³IBM Assignee, USA

11:45 J-8-4

Compatibility of ALD Hafnium Silicate with Dual Metal Gate CMOS Integration
M. M. Hussain¹, S. -. Song¹, C. Y. Kang¹, M. Quevedo-lopez², H. Alshareef², B. Sassman¹, R. Choi¹ and B. H. Lee³,
¹SEMATECH, ²Texas Instruments and ³IBM, USA

Room 411/412 (A)

12:00 A-8-6
Multi-Functionality of Novel Structured Tunneling Devices
W. Y. Choi,
J. Y. Song, J. P. Kim,
J. D. Lee and
B. G. Park, *Seoul National Univ., Korea*

Room 413 (B)**Room 414/415 (C)**

12:00 C-8-5
Si-Based Planer Type Ion-channel Biosensors
H. Uno¹, Z. L. Zhang¹,
T. Y. Chiang¹,
K. Suzui¹, R. Tero¹,
S. Nakao¹, S. Seki²,
S. Tagawa² and
T. Urisu¹, ¹*Inst. for Molecular Science and*
²*Osaka Univ., Japan*

Room 416/417 (D)**Room 418 (E)**

12:00 E-8-6
Comparative Study of DC and Microwave Characteristics of 0.12 μ m T-Shaped Gate AlGaAs/InGaAs/GaAs PHEMTs Using a Hybrid and Conventional E-beam Lithography Process
J. W. Lim,
S. W. Yoon,
H. K. Ahn, H. G. Ji,
W. J. Chang,
J. K. Mun and H. Kim,
ETRI, Korea

Room 419 (F)

12:05 F-8-5
Thickness Dependent Nano-Crystallization in Ge₂Sb₂Te₅ films and Its Effect on Devices
X. Wei^{1,2}, L. Shi¹ and
C. T. Chong^{1,2}, ¹*Data Storage Inst. and*
²*National Univ. of Singapore, Singapore*

Room 501 (G)

12:05 G-8-4
High Performance SiN-MIM Decoupling Capacitors with Surface-smoothed Bottom Electrodes for High-speed MPUs
I. Kume¹, N. Inoue¹,
H. Ohtake¹, S. Saitoh¹,
N. Furutake¹,
J. Kawahara¹,
T. Toda²,
T. Shinmura²,
K. Matsui², T. Iwaki²,
K. Ohto²,
M. Furuyama² and
Y. Hayashi¹, ¹*NEC Corp. and* ²*NEC Electronics, Japan*

Room 502 (H)**Room 511/512 (I)****Small Auditorium (J)**

12:05 J-8-5
Full-Metal-Gate Integration of Dual-Metal-Gate HiSiON CMOS Transistors by Using Oxidation-Free Dummy-Mask Process
F. Ootsuka,
Y. Tamura,
Y. Akasaka,
S. Inumiya, H. Nakata,
M. Ohtsuka,
T. Watanabe,
M. Kitajima, Y. Nara
and K. Nakamura,
Selete, Japan

Lunch

Lunch

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 7: Photonic Devices and Device Physics	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 10: Organic Materials Science, Device Physics, and Applications	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 3: CMOS Devices/Device Physics		Area 1: Advanced Gate Stack/Si Processing Science J-9-1
A-9: Novel Devices and Materials III (13:15-14:45) Chairs: K. Ishibashi (RIKEN) T. Fujisawa (NTT)	B-9: Detectors and Sensors (13:15-15:00) Chairs: M. Tokushima (NEC) M. Sugawara (Fujitsu Labs.)	C-9: Nano and Bio Sensors II (13:15-15:00) Chairs: H. Tabata (Osaka Univ.) H. Sugihara (Matsushita Electric)	D-9: Organic Transistor II (13:30-15:00) Chairs: M. Iwamoto (Tokyo Tech) T. Someya (Univ. of Tokyo)	E-9: GaN FETs and Process Technologies (13:15-15:00) Chairs: M. Kuzuhara (Univ. of Fukui) R. Hattori (Mitsubishi Electric)	F-9: Schottky S/D and Carrier Transport (13:15-14:55) Chairs: A. Hokazono (Toshiba) J. C. S. Woo (UCLA)	G-9: Special Session II : Metallization Challenges (13:15-15:35) Chairs: J. Koike (Tohoku Univ.) M. Nihei (Selete/Fujitsu)	H-9: Carrier Transport (13:15-14:55) Chairs: H. C. Lin (National Chiao Tung Univ.) K. Takeuchi (NEC)	J-9: Reliability (13:15-15:05) Chairs: J. Yugami (Renesas) S. Miyazaki (Hiroshima Univ.)	
13:15 A-9-1 (Invited) Organic Molecular Wires P. Hadley and M. Durkut, <i>Graz Univ. of Technology, Austria</i>	13:15 B-9-1 InP/InGaAs Leaky Waveguide Photodiode with a Partially p-Doped Absorption Layer and a Distributed-Bragg-Reflector (DBR) for High-Power and High-Bandwidth-Responsivity Product Performance W. Y. Chiu, W. K. Wang, Y. S. Wu, F. H. Huang, D. M. Lin, Y. J. Chan and J. W. Shi, <i>National Central Univ., Taiwan</i>	13:15 C-9-1 Membranes as Self-Assembling Coating of Solid State Device Components: Integration of Submicron Electrical Circuitry with Biological Systems M. R. R. de Planque, N. C. Toledo, S. A. Contera and J. F. Ryan, <i>Univ. of Oxford, UK</i>	13:15 E-9-1 (Invited) Methods and Mechanisms for Ohmic Contacts on AlGaN/GaN HEMTs I. Adesida, F. M. Mohammed, L. Wang, A. Basu and V. Kumar, <i>Univ. of Illinois at Urbana-Champaign, USA</i>	13:15 F-9-1 Dopant Segregated Pt-Germanide Schottky S/D p-MOSFET with HfO ₂ /Ta ₂ N gate on Strained Si-SiGe channel W. Y. Loh ¹ , Y. Chen ^{1,2} , S. J. Lee ² , L. K. Bera ¹ , R. Yang ¹ , G. Q. Lo ¹ and D. L. Kwong ¹ , ¹ <i>Inst. of Microelectronics and</i> ² <i>National Univ. of Singapore, Singapore</i>	13:15 G-9-1 (Invited) Reliability Challenges for Advanced Copper Low-k Interconnects Z. Tokei ¹ , C. Bruynseraede ¹ , Y. L. Li ^{1,2} , I. Ciofi ¹ and G. P. Beyer ¹ , ¹ <i>IMEC and</i> ² <i>Katholieke Univ. Leuven, Belgium</i>	13:15 H-9-1 Comparative Study on Influence of Subband Structures on Electrical Characteristics of III-V Semiconductor, Ge and Si Channel n-MISFETs S. Takagi and S. Sugahara, <i>Univ. of Tokyo, Japan</i>	13:15 J-9-1 (Invited) Degradation and Breakdown of Sub-1nm EOT HfO ₂ /Metal Gate Stacks G. Groeseneken ^{1,2} , R. Degraeve ¹ , T. Kauerauf ^{1,2} , M. Cho ^{1,3} , M. Zahid ⁴ , L. A. Ragnarsson ¹ , D. P. Brunco ⁵ , B. Kaczer ¹ , P. Roussel ¹ and S. De Gendt ^{1,2} , ¹ <i>IMEC, </i> ² <i>KU Leuven, </i> ³ <i>Seoul National Univ., </i> ⁴ <i>John Moores Univ. and </i> ⁵ <i>Intel assignee at IMEC, Belgium</i>		
	13:30 B-9-2 Deep Trench Isolation for Pixel Crosstalk Suppression in Active Pixel Sensor with 1.7µm pixel pitch B. J. Park ¹ , C. R. Moon ¹ , Y. W. Lee ¹ , D. W. Kim ¹ , K. H. Paik ¹ , J. R. Yoo ¹ , Y. S. Yoo ¹ , Y. Jon ¹ , C. H. Koo ¹ , S. C. Bang ¹ , Y. K. Lee ¹ , Y. J. Cho ¹ , S. H. Hwang ¹ , D. C. Park ¹ , H. G. Jung ¹ , J. C. Shin ¹ , J. Jung ² , K. B. Lee ¹ , H. P. Noh ¹ , D. H. Lee ¹ and K. Kim ¹ , ¹ <i>Samsung Electronics Co. and </i> ² <i>Sejong Univ., Korea</i>	13:30 C-9-2 Evaluation of Electrical Stimulus Current to Retina Cells for Retinal Prosthesis by Using Platinum-Black (Pt-b) Stimulus Electrode Array T. Watanabe, K. Komiya, T. Kobayashi, R. Kobayashi, T. Fukushima, H. Tomita, E. Sugano, M. Sato, H. Kurino, T. Tanaka, M. Tamai and M. Koyanagi, <i>Tohoku Univ., Japan</i>	13:30 D-9-1 (Invited) Development of a Printed Dielectric Layer for Organic Transistors T. Kamata, S. Uemura, M. Yoshida, K. Suemori, S. Hoshino, N. Takada and T. Kozasa, <i>AIST, Japan</i>		13:35 F-9-2 Improved Performance of Schottky Barrier Source/Drain Transistors with High-K Gate Dielectrics by Adopting Recessed Channel and/or Buried Source/Drain Structures M. Ono, M. Koyama and A. Nishiyama, <i>Toshiba Corp., Japan</i>		13:35 H-9-2 Influence of High Dielectric Constant in Gate Insulator on Remote Coulomb Scattering due to Gate Impurities in Si MOS Inversion Layer Y. Nakabayashi ¹ , T. Ishihara ¹ , T. Shimizu ² and J. Koga ¹ , ¹ <i>Toshiba Corp. and</i> ² <i>Semiconductor Co., Toshiba Corp., Japan</i>		

Room 411/412 (A)

13:45 A-9-2
Possible Non-equilibrium Kondo Effect in a Nanocrystalline Silicon Point-Contact Transistor
M. A. H. Khalafalla¹, H. Mizuta¹, S. Oda¹ and Z. A. K. Durrani²,
¹Tokyo Tech and
²Univ. of Cambridge, Japan

14:00 A-9-3
Low Temperature Characteristics of Ambipolar SiO₂/Si/SiO₂ Hall-bar Devices
K. Takashina¹, B. Gaillard¹, Y. Ono¹ and Y. Hirayama^{1,2},
¹NTT Corp. and
²SORST-JST, Japan

14:15 A-9-4
Detection of Magnetic Domain Wall in a Permalloy Wire by the Local Hall Effect
Y. Sekine¹, T. Akazaki¹ and J. Nitta^{2,3},
¹NTT Corp.,
²Tohoku Univ. and
³CREST-JST, Japan

14:30 A-9-5
A Field-Effect Transistor with a Deposited Graphite Thin Film
H. Inokawa¹, M. Nagase², S. Hirono³, T. Goto², H. Yamaguchi² and K. Torimitsu²,
¹Shizuoka Univ.,
²NTT Corp. and
³NTT Afty Engineering Corp., Japan

Room 413 (B)

14:00 B-9-4
Photodetective Characteristics of Metal-Oxide-Semiconductor Tunneling Structure with Aluminum Grid Gate
H. Hashimoto, R. Yamada, K. Arima, J. Uchikoshi and M. Morita, Osaka Univ., Japan

14:15 B-9-5
A Compact Single-Photon Avalanche Diode in a Deep-Submicron CMOS Technology
H. Finkelstein, M. J. Hsu and S. Esener, Univ. of California San Diego, USA

14:30 B-9-6
Threshold Behavior of Photoresponse of Plasma Waves by New Photomixer Devices
Y. M. Mezziani¹, M. Hanabe¹, T. Otsuji¹ and E. Sano²,
¹Tohoku Univ. and
²Hokkaido Univ., Japan

Room 414/415 (C)

13:45 C-9-3
Development of a CMOS Image Sensor for Real Time In Vivo Imaging of the Protease Activity Inside the Mouse Hippocampus
D. C. Ng, T. Nakagawa, T. Tokuda, K. Kagawa, M. Nunoshita, H. Tamura, S. Shiosaka and J. Ohta, Nara Inst. of Science and Technology, Japan

14:00 C-9-4
An Optical/Potential/Voltammetric Multifunctional CMOS Image Sensor for On-chip Biomolecular/Neural Sensing Applications
T. Tokuda, I. Kadowaki, K. Kagawa, M. Nunoshita and J. Ohta, Nara Inst. of Science and Technology, Japan

14:15 C-9-5
Large scale electrode array based on distributed microchip architecture for retinal prosthesis
J. Ohta¹, T. Tokuda¹, S. Sugitani¹, M. Taniyama¹, M. Nunoshita¹, A. Uehara², Y. Terasawa² and Y. Tano³,
¹Nara Inst. of Science and Technology,
²NIDEK Co., Ltd. and
³Osaka Univ., Japan

14:30 C-9-6
Development of Si Long Microprobe (SiLM) for Platform of Intelligent Neural Implant Microsystem
R. Kobayashi, T. Watanabe, K. Komiya, T. Fukushima, K. Sakamoto, H. Kurino, T. Tanaka, N. Katayama, H. Mushiake and M. Koyanagi, Tohoku Univ., Japan

Room 416/417 (D)

14:00 D-9-2
Low Hysteresis Organic Thin-Film Transistors and Inverters with Hybrid Gate Dielectric
D. W. Park, C. A. Lee, K. D. Jung, B. G. Park, H. Shin and J. D. Lee, Seoul National Univ., Korea

14:15 D-9-3
Performance enhancement of Organic TFT by low-energy Ar ion beam treatment onto gate dielectric surface
S. Kang¹, J. Park¹, S. Jung¹, H. J. Lee² and M. Yi¹,
¹Pusan National Univ. and
²SungKyunKwan Univ., Korea

14:30 D-9-4
Stable Polymer Dielectric Film for P3HT TFT by Modified Poly-(Vinyl Phenol) with Polar Functional Group
P. Y. Lo^{1,2}, Z. Pei¹, F. Y. Yang¹, Y. R. Peng¹, Y. C. Lin¹ and Y. J. Chan²,
¹Industrial Technology Research Inst. and
²National Central Univ., Taiwan

Room 418 (E)

13:45 E-9-2
High-temperature and UV-assisted C-V characterization of GaN MIS structures
H. Kato, M. Miczek and T. Hashizume, Hokkaido Univ., Japan

14:00 E-9-3
Device Isolation by Plasma Treatment for Planar Integration of E/D-mode AlGaIn/GaN HEMTs
R. Wang, Y. Cai, W. C. W. Tang, K. M. Lau and K. J. Chen, Hong Kong Univ. of Science and Technology, Hong Kong

14:30 E-9-5
ICP Reactive Ion Etching with SiCl₄ Gas for Recessed Gate AlGaIn/GaN HFET
K. Matsuura¹, D. Kikuta¹, J. P. Ao¹, H. Ogiya², M. Hiramoto², H. Kawai³ and Y. Ohno¹,
¹Univ. of Tokushima,
²SAMCO Inc. and
³POWDEC K. Co., Japan

Room 419 (F)

13:55 F-9-3
Examination of Performance Improvement in Dopant Segregated Schottky MOSFETs; Short Channel Effects, Carrier Velocity and Parasitic Resistance
Y. Nishi, A. Kinoshita and J. Koga, Toshiba Corp., Japan

14:15 F-9-4
Study on Carrier Transport Limited by Coulomb Scattering due to Charged Centers in HfSiON MISFETs
T. Ishihara, R. Iijima, M. Takayanagi, H. Tanimoto and M. Koyama, Toshiba Corp., Japan

Room 501 (G)

13:45 G-9-2
Diffusion Barrier Property of an Interface Layer Formed with Cu-Mn, Al and Mg Alloy Films on SiO₂
J. Iijima^{1,2}, M. Haneda¹ and J. Koike¹,
¹Tohoku Univ. and
²JST, Japan

14:05 G-9-3
Self-Formation of Ti-rich Interfacial Layers in Cu(Ti) Alloy Films
S. Tsukimoto, K. Ito and M. Murakami, Kyoto Univ., Japan

14:25 G-9-4 (Invited)
New Method of Probing Barrier Integrity and Low-k Stability
C. U. Kim¹, D. M. Meng¹, N. Michael¹, Y. J. Park² and L. Matz²,
¹Univ. of Texas at Arlington and
²Texas Instruments, USA

Room 502 (H)

13:55 H-9-3
Experimental Evidence for Invalidity of Matthiessen's Rule for MOS Inversion Layer Mobility Analysis through Hall Factor Measurement
K. Kita, H. Irie and A. Toriumi, Univ. of Tokyo, Japan

14:15 H-9-4
Analytical Model for Phonon-Limited Mobility in n-MOS Inversion Layers on Arbitrarily Oriented and Strained Si Surfaces
M. Szczap^{1,2}, N. Cavassilas¹, F. Boeuf², F. Payet² and T. Skotnicki²,
¹L2MP and
²STMicroelectronics, France

14:35 H-9-5
Energy relaxation of two-dimensional electrons in Si-MOSFETs : determination of deformation potential constant of conduction band of Si
K. H. Park, K. Hirakawa and S. Takagi, Univ. of Tokyo, Japan

Room 511/512 (I)**Small Auditorium (J)**

13:45 J-9-2
Impact of Captured-Carrier Distribution on Recovery Characteristics of Positive- and Negative-Bias Temperature Instability in HfSiON/SiO₂ Gate Stack
I. Hirano, T. Yamaguchi, Y. Mitani, K. Sekine, M. Takayanagi, K. Eguchi and H. Satake, Toshiba Corp., Japan

14:05 J-9-3
Reliability of thick oxides integrated with HfSiOx gate dielectric
B. H. Lee^{1,2}, C. Y. Kang¹, T. H. Lee³, J. Barnett¹, R. Choi¹, S. C. Song¹ and R. Jammy²,
¹SEMATECH,
²IBM Assignee and
³Univ. of Texas at Austin, USA

14:25 J-9-4
Impact of Initial Traps on TDDB and NBTI Reliabilities in High-k Gate Dielectrics
K. Okada¹, H. Ota², T. Horikawa², M. Kadoshima¹, A. Ogawa¹, T. Nabatame¹ and A. Toriumi^{2,3},
¹MIRAI-ASET,
²MIRAI-ASRC-AIST and
³Univ. of Tokyo, Japan

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
14:45 B-9-7 Optical Responses of Josephson Vortex flow Transistor under irradiation of femtosecond laser pulses I. Kawayama ^{1,2} , Y. Doda ^{1,2} , H. Murakami ¹ and M. Tonouchi ^{1,2} , ¹ Osaka Univ. and ² CREST-JST, Japan	14:45 C-9-7 Liquid Sensing by Nano-gap Device with Treated Surface T. Hirokane, H. Hashimoto, D. Kanzaki, T. Takegawa, S. Morita, S. Urabe, K. Arima, J. Uchikoshi and M. Morita, <i>Osaka Univ., Japan</i>	14:45 D-9-5 Fabrication of Low-Voltage Pentacene Thin Film Transistors with Al ₂ O ₃ gate dielectric grown by oxygen plasma process K. D. Kim and C. K. Song, <i>Dong-A Univ., Korea</i>	14:45 E-9-6 SiO ₂ Passivation Effects on the Leakage Current in Dual-Gate AlGaIn/GaN High Electron Mobility Transistors M. W. Ha, J. Lim, Y. H. Choi, J. C. Her, K. S. Seo and M. K. Han, <i>Seoul National Univ., Korea</i>	

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
	14:55 G-9-5 An Excellent Cu Diffusion Barrier for Next Generation Multi-level Cu-interconnect C. J. Lee, C. F. Huang and B. Y. Tsui, <i>National Chiao Tung Univ., Taiwan</i>			14:45 J-9-5 Leakage mechanism of ultrathin SiON gate dielectric H. Watanabe, D. Matsushita, K. Muraoka and K. Kato, <i>Toshiba Corp., Japan</i>

Break

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 10: Organic Materials Science, Device Physics, and Applications	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics
C-10: MEMS and NEMS : Application (15:15-16:30) Chairs: Y. Yoshino (Murata Mfg.) T. Ono (Tohoku Univ.)	D-10: Organic Transistor III (15:15-16:15) Chairs: K. Kudo (Chiba Univ.) T. Someya (Univ. of Tokyo)	E-10: High-Voltage GaN Devices (15:15-17:00) Chairs: A. Nakagawa (New Japan Radio) T. Tanaka (Matsushita Electric)
15:15 C-10-1 (Invited) Physical Sensors in MEMS Technology K. Maenaka, <i>Univ. of Hyogo, Japan</i>	15:15 D-10-1 Threshold Voltage Control in Pentacene TFTs by Perfluoropentacene Stack T. Yokoyama, T. Nishimura, K. Kita, K. Kyuno and A. Toriumi, <i>Univ. of Tokyo, Japan</i>	15:15 E-10-1 (Invited) Recent Advances in GaN Power Devices T. Kachi, <i>Toyota Central R&D Labs., Japan</i>

Break

Area 3: CMOS Devices/Device Physics	Area 1: Advanced Gate Stack/Si Processing Science
H-10: Advanced Device Technology (15:15-16:55) Chairs: K. Shibahara (Hiroshima Univ.) A. Hokazono (Toshiba)	J-10: Metal Gate Electrode (15:15-16:35) Chairs: T. Nabatame (ASET) H. Fukutome (Fujitsu Labs.)
15:15 G-9-6 Plasma-enhanced polymerization thin films as a drift barrier for Cu interconnects T. Yoshino ¹ , J. Kawahara ² , N. Hata ¹ , Y. Shishida ² and T. Kikkawa ^{1,3} , ¹ MIRAI-ASRC, AIST, ² MIRAI-ASET and ³ Hiroshima Univ., <i>Japan</i>	15:15 H-10-1 Novel Elevated Source/Drain Technology for FinFET Overcoming Agglomeration and Facet Problems Utilizing Solid Phase Epitaxy K. Miyano, A. Kaneko, I. Mizushima, A. Yagishita, K. Suguro, Y. Saito, K. Eguchi and Y. Tsunashima, <i>Toshiba Corp., Japan</i>
	15:15 J-10-1 Work Function Modulation by Segregation of Indium through Tungsten Gate For Dual-Metal Gate CMOS Applications K. Nakajima, M. Koyama, T. Aoyama, A. Nishiyama, K. Eguchi and K. Suguro, <i>Toshiba Corp., Japan</i>

Room 411/412 (A)**Room 413 (B)****Room 414/415 (C)****Room 416/417 (D)****Room 418 (E)****Room 419 (F)****Room 501 (G)****Room 502 (H)****Room 511/512 (I)****Small Auditorium (J)**

15:30 D-10-2
Organic Field-Effect Transistor Integrated Circuits using Self-Alignment Process Technology
H. Okada, T. Nagai, T. Kimura, S. Naka and H. Onnagawa, *Univ. of Toyama, Japan*

15:45 C-10-2
Piezoelectric Optical Micro Scanner with Built-in Torsion Sensor
T. Kobayashi and R. Maeda, *National Inst. of Advanced Industrial Science and Technology, Japan*

16:00 C-10-3
High-Q Piezoelectrically Actuated RF MEMS Tunable Capacitor
M. Nishigaki¹, T. Nagano¹, T. Miyazaki¹, T. Kawakubo² and K. Itaya¹, *¹Toshiba Corp. and ²Toshiba Research Consulting Corp., Japan*

15:45 D-10-3
Alignment-Free Printable Organic Thin-Film Transistors on the Flexible Substrate
T. Arai¹, N. Sato², K. Yamaguchi², M. Kawasaki¹, M. Fujimori¹, T. Shiba¹, M. Ando¹ and K. Torii¹, *¹Hitachi, Ltd. and ²Kanagawa Univ., Japan*

16:00 D-10-4
Hall effect of polycrystalline pentacene field-effect transistors on plastic films
Y. Takamatsu, T. Sekitani, S. Nakano, T. Sakurai and T. Someya, *Univ. of Tokyo, Japan*

15:45 E-10-2
Improvement of Breakdown Voltages in GaN Schottky Barrier Diodes by Pseudo-Superjunction Structures
K. Nakazawa, H. Ueno, H. Matsuo, M. Yanagihara, Y. Uemoto, T. Ueda and T. Tanaka, *Matsushita Electric, Japan*

16:00 E-10-3
High Critical Electric Field Exceeding 8 MV/cm Measured Using AlGaIn p-i-n Vertical Conducting Diode on n-SiC Substrate
A. Nishikawa, K. Kumakura and T. Makimoto, *NTT Corp., Japan*

15:35 H-10-2
Threshold Voltage Instability of 45-nm-node Poly-Si- or FUSI-Gated SRAM Transistors Caused by Dopant Lateral Diffusion in Poly-Si
K. Hosaka, T. Aoyama, K. Suzuki, *Fujitsu Labs., Japan*

15:55 H-10-3
Novel threshold voltage fine control method for FETs within a wafer using LDSi (Locally Differentiated Scanning ion implant)
K. B. Rouh, M. Y. Lee, S. W. Jin, Y. S. Sohn, Y. S. Joung, Y. J. Ki, I. K. Han, Y. W. Song and S. W. Park, *Hynix Semiconductor Inc., Korea*

15:35 J-10-2
Diffusion control technique in TiN stacked metal gate electrodes for p-MISFETs
S. Sakashita, T. Kawahara, M. Inoue, K. Mori, S. Yamanari, M. Higashi, Y. Nishida, K. Honda, N. Murata, J. Tsuchimoto, J. Yugami, K. Fujiwara and M. Yoneda, *Renesas Technology Corp., Japan*

15:55 J-10-3
Work Function Instability at pMOS Metal/HfSiON Interfaces
Y. Tsuchiya and M. Koyama, *Toshiba Corp., Japan*

Room 411/412 (A)**Room 413 (B)****Room 414/415 (C)**

16:15 C-10-4
Solenoid RF
Transformer and Balun
J. M. Yook, J. H. Ko
and Y. S. Kwon,
KAIST, Korea

Room 416/417 (D)**Room 418 (E)**

16:15 E-10-4
High Breakdown
Voltage AlGaIn/GaN
MIS-HEMT with
TiO₂/Si₃N₄ Gate
Insulator
S. Yagi¹, M. Shimizu¹,
M. Inada¹,
H. Okumura¹,
H. Ohashi¹, Y. Yano²
and N. Akutsu²,
¹*National Inst. of
Advanced Industrial
Science and
Technology and*
²*Taiyo Nippon Sanso
Corp., Japan*

16:30 E-10-5
Pnp AlGaIn/InGaIn/
GaN Double
Heterojunction Bipolar
Transistors with Low-
Base-Resistance
($<100\Omega/\text{sq}$)
K. Kumakura and
T. Makimoto, *NTT
Corp., Japan*

16:45 E-10-6
A New Field Plate
Structure for
Suppression of
Leakage Current of
AlGaIn/GaN HEMTs
Y. H. Choi, M. W. Ha,
J. Lim and M. K. Han,
*Seoul National Univ.,
Korea*

Room 419 (F)**Room 501 (G)****Room 502 (H)**

16:15 H-10-4
Novel Gate-All-
Around MOSFETs
with Self-Aligned
Structure
J. Y. Song,
W. Y. Choi, J. P. Kim,
S. W. Kim, J. D. Lee
and B. G. Park, *Seoul
National Univ., Korea*

16:35 H-10-5
Improvement of Bulk
CMOS Electrostatic
Integrity using
Germanium and
Carbon co-implantation
B. Dumont^{1,2},
A. Pouydebasque³,
F. Milesi^{4,5}, S. Kader²,
F. Boeuf¹ and
T. Skotnicki¹,
¹*STMicroelectronics,*
²*LPM - INSA Lyon,*
³*Philips*
Semiconductors, ⁴*Ion
Beam Services and*
⁵*CEA-LETI, France*

Room 511/512 (I)**Small Auditorium (J)**

16:15 J-10-4
Thermal stability of
metal electrodes and its
impact on gate
dielectric
characteristics
H. Park^{1,4}, H. C. Wen²,
M. Chang¹, M. Jo¹,
R. Choi², B. H. Lee^{2,3},
S. C. Song²,
C. Y. Kang^{2,4}, T. Lee⁴,
G. Brown², J. C. Lee⁴
and H. Hwang¹,
¹*Gwangju Inst. of
Science and
Technology,*
²*SEMATECH,* ³*IBM
Assignee and* ⁴*The
Univ. of Texas at
Austin, Korea*