

Wednesday, October 7

**Opening Session (10:00-12:00)**

Chair: S. Samukawa, *Tohoku Univ.*  
K. Wada, *Univ. of Tokyo*

**10:00 PL-1-0**

Welcome Address and SSDM Award Presentaion  
M. Koyanagi, *Tohoku Univ.*

**10:30 PL-1-1**

Moore's Law Past 32nm: the Challenges in Physics and  
Technology Scaling  
K. J. Kuhn, *Intel Corp., USA*

**11:15 PL-1-2**

The Third Generation of Solar Photovoltaic Electricity  
T. Tomita, *Univ. of Tokyo, Japan*

**12:00-13:30 Lunch**

**Area 1: Advanced Gate Stack / Si Processing &  
Material Science**

**B-1: Characterization**

**13:30-15:40 2F Heisei <Naka>**

Chair: S. Miyazaki (Hiroshima Univ.)  
K. Shiraishi (Univ. of Tsukuba)

**13:30 B-1-1 (Invited)**

Microscopic Characterization of Devices by Scanning  
Transmission Electron Microscopy: From Single Atom  
Imaging to Macroscopic Properties  
S. J. Pennycook, K. van Benthem, A. G. Marinopoulos  
and S. T. Pantelides, *Oak Ridge National Lab. (USA)*

**14:00 B-1-2**

Three-Dimensional Visualization Technique for Crystal  
Defects in High Performance CMOS Devices with  
Embedded SiGe-Source/Drain  
S. Kudo, N. Nakanishi, Y. Hirose, K. Sato, T. Yamashita,  
H. Oda, K. Kashihara, N. Murata, T. Katayama,  
K. Asayama, J. Komori and E. Murakami, *Renesas Tech.*

Corp. (Japan)

**14:20 B-1-3**

X-ray photoelectron spectroscopy study of dipole effects at HfO<sub>2</sub>/SiO<sub>2</sub>/Si stacks

L. Q. Zhu, K. Kita, T. Nishimura, K. Nagashio, S. K. Wang and A. Toriumi, *Univ. of Tokyo (Japan)*

**14:40 B-1-4**

Impact of Si Oxidation States on Dipole Layer at HfO<sub>2</sub>/Si Interface

N. Miyata<sup>1,2</sup>, Y. Abe<sup>2</sup> and T. Yasuda<sup>1</sup>, <sup>1</sup>AIST and <sup>2</sup>Musashi Inst. of Tech. (Japan)

**15:00 B-1-5**

Evaluation of Effective Work Function of Pt on Bi-layer High-k/SiO<sub>2</sub> Stack Structure using by Backside X-ray Photoelectron Spectroscopy

T. Mori, A. Ohta, H. Murakami, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*

**15:20 B-1-6**

Molecular Dynamics Study of Oxidation Process with SiO emission and incorporation into the Si/SiO<sub>2</sub> System

N. Takahashi, T. Yamasaki and C. Kaneta, *Fujitsu Labs. Ltd. (Japan)*

**15:40-16:00 Break**

**Area 1: Advanced Gate Stack / Si Processing & Material Science**

**B-2: Characterization and Process Technology**

**16:00-18:15 2F Heisei <Naka>**

Chair : K. Shiraishi (Univ. of Tsukuba)  
S. Miyazaki (Hiroshima Univ.)

**16:00 B-2-1**

Thermally stable Ni-silicide gate electrode with TiN barrier metal for NAND flash memory application with 24 nm technology and beyond

S. J. Whang, M. S. Joo, B. M. Seo, K. E. Chang,

W. K. Kim, T. W. Jung, G. H. Kim, J. Y. Lim, K. Y. Kim, K. Hong and S. K. Park, *Hynix Semiconductor Inc. (Korea)*

**16:20 B-2-2**

Lanthanoid Metal Oxide MIM Capacitors for Precision Analog Circuits: Material Screening, Process Development, and Characterization

J. D. Chen<sup>1</sup>, J. J. Yang<sup>1</sup>, R. Wise<sup>2</sup>, P. Steinmann<sup>2</sup>, C. Zhu<sup>1</sup> and Y. C. Yeo<sup>1</sup>, <sup>1</sup>National Univ. of Singapore and <sup>2</sup>Texas Instruments Inc. (Singapore)

**16:40 B-2-3**

Oxygen-Terminated Si Surface for Atomic Layer Deposition and its Impact on Interfacial Electrical Quality of sub-nm-EOT high-k Gate Stacks

Y. Morita, S. Migita, N. Taoka, W. Mizubayashi and H. Ota, *MIRAI-AIST (Japan)*

**17:00 B-2-4**

New Criteria for Suppressing Extrinsic Defect Generation in Ultra Thin SiON Gate Insulator (EOT<1.4nm) for Advanced CMOSFETs

S. Shimamoto<sup>1</sup>, H. Kawashima<sup>2</sup>, T. Kikuchi<sup>1</sup>, Y. Yamaguchi<sup>2</sup> and A. Hiraiwa<sup>2</sup>, <sup>1</sup>Hitachi, Ltd. and <sup>2</sup>Renesas Tech. Corp. (Japan)

**Area 2: Characterization and Materials Engineering for Interconnect Integration**

**D-1: 3D Integration**

**13:30-15:40 3F Sakura**

Chair: J. Kodate (NTT)  
J. Gambino (IBM Microelectronics)

**13:30 D-1-1 (Invited)**

Through-Si-Via Technology Solutions for 3D System Integration

E. Beyne, B. Swinnen, J. V. Olmen, D. S. Tezcan, A. Jourdain and P. Limaye, *IMEC (Belgium)*

**14:00 D-1-2**

Development of EEB (Electroplated-Evaporation Bumping) Technology for Fine Pitch and Low Resistance Cu/Sn Micro-Bumps

Y. Ohara, A. Noriki, E. Iwata, T. Hiraki, K. W. Lee, M. Murugesan, J. C. Bea, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. (Japan)*

**14:20 D-1-3**

High-Aspect-Ratio Fine Cu Sidewall Interconnection over Chip Edge with Tapered Polymer for MEMS-LSI Multi-Chip Module

A. Noriki, Y. Kaiho, E. Iwata, Y. Ohara, M. Murugesan, K. W. Lee, J. C. Bea, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. (Japan)*

**14:40 D-1-4**

Back-Side Illuminated CMOS Image Sensor Fabricated using Compliant Bump

N. Watanabe<sup>1</sup>, I. Tsunoda<sup>2</sup>, T. Takao<sup>1</sup>, K. Tanaka<sup>3</sup> and T. Asano<sup>1</sup>, <sup>1</sup>*Kyushu Univ.*, <sup>2</sup>*Kyushu Inst. of Tech. and* <sup>3</sup>*Kyushu Sangyo Univ. (Japan)*

**15:00 D-1-5**

Tantalum lightshield for CMOS image sensor with global shutter

J. Gambino, R. J. Rassel, A. Watts, C. Musante, R. Krishnasamy, B. Leidy, N. Lai, T. C. Lee, P. Razina, C. Walsh, B. Czabaj, R. Preston, D. Demuyneck, J. Adkisson, J. Ellis-Monaghan and M. Jaffe, *IBM (USA)*

**15:20 D-1-6**

Nondestructive Warpage Measurements of LSI Chips in a Stacked SiP by using High-Energy X-ray Diffraction

A. Toda and N. Ikarashi, *NEC Corp. (Japan)*

**15:40-16:00 Break**

**Area 2: Characterization and Materials Engineering for Interconnect Integration**

**D-2: RF Device/Process Technology**

**16:00-18:10 3F Sakura**

Chair: Y. Hayashi (NEC Electronics Corp.)  
N. Nakano (Keio Univ.)

**16:00 D-2-1 (Invited)**

Wireless Interconnection by Electromagnetic Coupling of Open-Ring Resonators and Its Application to System Integration

Y. Ohno<sup>1</sup> and I. Awai<sup>2</sup>, <sup>1</sup>*Univ. of Tokushima and* <sup>2</sup>*Ryukoku Univ. (Japan)*

**16:30 D-2-2**

Transmission Characteristics of Silicon On-chip Integrated Antennas as Millimeter-Wave Wireless Interconnects

W. Moriyama, K. Kimoto, S. Kubota, N. Sasaki and T. Kikkawa, *Hiroshima Univ. (Japan)*

**16:50 D-2-3**

High Gain and High Directivity UWB Bow-tie Antenna with High Impedance Metamaterial Surface

S. Kubota, N. Sasaki, Y. Kayaba, W. Moriyama, T. Kozaki and T. Kikkawa, *Hiroshima Univ. (Japan)*

**17:10 D-2-4**

A Novel Multi-Layered Hetero-Structure of Ni-Zn Ferrite/TaN Buffer for Effective Magnetic Core in On-Chip Inductors

K. Kaneko, N. Inoue, N. Furutake and Y. Hayashi, *NEC Electronics Corp. (Japan)*

**17:30 D-2-5**

System-on-Package Platform with Decoupling Capacitor Integration and Thermal Performance Improvement

N. Jeon, J. Noh, J. Maeng and K. S. Seo, *Seoul National Univ. (Korea)*

**17:50 D-2-6**

Stabilities of La<sub>2</sub>O<sub>3</sub> Metal-Insulator-Metal Capacitors under Constant Voltage Stress

S. H. Wu, C. K. Deng and B. S. Chiou, *National Chiao Tung Univ. (Taiwan)*

**Area 3: CMOS Devices /Device Physics****A-1: SOI/GOI and Channel Engineering****13:30-16:00 2F Heisei <Higashi>**Chair: T. Tanaka (Fujitsu Microelectronics Ltd.)  
K. Shibahara (Hiroshima Univ.)**13:30 A-1-1 (Invited)**Ultrathin Body and BOX SOI and sSOI for Low Power Application at the 22nm technology node and below  
F. Andrieu<sup>1</sup>, C. Fenouillet-Béranger<sup>2</sup>, O. Weber<sup>1</sup>, S. Baudot<sup>1</sup>, C. Buj<sup>1</sup>, J. P. Noel<sup>1</sup>, O. Thomas<sup>1</sup>, O. Rozeau<sup>1</sup>, P. Perreau<sup>2</sup>, L. Tosti<sup>1</sup>, L. Brévard<sup>1</sup> and O. Faynot<sup>1</sup>, <sup>1</sup>CEA-LETI/MINATEC and <sup>2</sup>Also with STMicro electronics (France)**14:00 A-1-2** $V_{th}$  Dependence of  $V_{th}$  Variability in Intrinsic Channel SOI MOSFETs with Ultra-Thin BOX  
C. Lee<sup>1</sup>, A. T. Putra<sup>1</sup>, K. Shimizu<sup>1</sup> and T. Hiramoto<sup>1,2</sup>, <sup>1</sup>Univ. of Tokyo and <sup>2</sup>MIRAI-Selete (Japan)**14:20 A-1-3**Counter-doping as a solution for multi threshold voltage on FDSOI MOSFETs with a single TiN/HfO<sub>2</sub> gate stack  
C. Buj-Dufournet, F. Andrieu, O. Faynot, O. Weber, F. Allain, L. Tosti, C. Fenouillet-Béranger, D. Lafond and S. Deleonibus, CEA-LETI/MINATEC (France)**14:40 A-1-4**High Performance (110)-oriented GOI pMOSFETs Fabricated by Ge Condensation Technique  
S. Dissanayake<sup>1</sup>, S. Sugahara<sup>2</sup>, M. Takenaka<sup>1</sup> and S. Takagi<sup>1</sup>, <sup>1</sup>Univ. of Tokyo and <sup>2</sup>Tokyo Tech (Japan)**15:00 A-1-5**The Impact of Uni-axial Strain and Dynamic Body Biases on Low Frequency Noise in Nanoscale pMOSFETs  
K. L. Yeh, C. Y. Ku, W. L. Hong and J. C. Guo, National Chiao Tung Univ. (Taiwan)**15:40 A-1-7 (Invited)**The Tunnel Source n-MOSFET: A Novel Asymmetric Device for Low Power Applications  
N. Venkatagirish, A. Tura, R. Jhaveri, H. Y. Chang and J. Woo, UCLA (USA)**Area 3: CMOS Devices /Device Physics****A-2: Variability and RTS****16:00-18:20 2F Heisei <Higashi>**Chair: T. Hiramoto (Univ. of Tokyo)  
F. Boeuf (STMicroelectronics)**16:00 A-2-1**A new definition of threshold voltage by constant slope for analysis of statistical variations of MOSFETs  
T. Tanaka, H. Suzuki and O. Yamasaki, Fujitsu Microelectronics Ltd. (Japan)**16:20 A-2-2**Temperature Coefficient of Threshold Voltage in Metal/High-k Gate Transistors with Various Thickness of TiN and Capping Layers  
Y. Nishida<sup>1,2</sup>, K. Eikyu<sup>1</sup>, A. Shimizu<sup>1</sup>, T. Yamashita<sup>1</sup>, H. Oda<sup>1</sup>, Y. Inoue<sup>1</sup> and K. Shibahara<sup>2</sup>, <sup>1</sup>Renesas Tech. Corp. and <sup>2</sup>Hiroshima Univ. (Japan)**16:40 A-2-3**Impact of interface roughness on threshold-voltage variation in ultra-small three-dimensional MOSFETs  
N. Mori and H. Minari, Osaka Univ. (Japan)**17:00 A-2-4**Statistical Analysis of Time Constant Ratio of Random Telegraph Signal with Very Large-Scale Array TEG  
T. Fujisawa, K. Abe, S. Watabe, N. Miyamoto, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)**17:20 A-2-5**

Impact of Channel Doping Concentration on Random

Telegraph Signal Noise

K. Abe<sup>1</sup>, A. Teramoto<sup>1</sup>, S. Watabe<sup>1</sup>, T. Fujisawa<sup>1</sup>,  
S. Sugawa<sup>1</sup>, Y. Kamata<sup>2</sup>, K. Shibusawa<sup>2</sup> and T. Ohmi<sup>1</sup>,  
<sup>1</sup>Tohoku Univ. and <sup>2</sup>OKI Semiconductor Miyagi Co., Ltd.  
(Japan)

**17:40 A-2-6**

Experimental Study on I<sub>g</sub> RTS Noise of SiON/HfO<sub>2</sub>/TaN  
PMOSFETs  
L. Zhang<sup>1</sup>, R. Wang<sup>1</sup>, J. Zhuge<sup>1</sup>, R. Huang<sup>1</sup>, T. Yu<sup>1</sup>,  
P. Kirsch<sup>2</sup>, H. H. Tseng<sup>2</sup> and Y. Wang<sup>1</sup>, <sup>1</sup>Peking Univ. and  
<sup>2</sup>SEMATECH (China)

**18:00 A-2-7**

Leakage and Matching Optimization of SRAM-cells for  
Wireless Applications  
N. Planes<sup>1</sup>, O. Menu<sup>1</sup>, C. Laviron<sup>2</sup>, J. Bonnouvrier<sup>1</sup>,  
F. Wacquant<sup>1</sup>, R. Ranica<sup>1</sup>, C. Boccaccio<sup>1</sup>, O. Callen<sup>1</sup>,  
S. Del Medico<sup>1</sup>, D. Noblet<sup>1</sup>, M. Haond<sup>1</sup> and F. Boeuf<sup>1</sup>,  
<sup>1</sup>STMicroelectronics and <sup>2</sup>CEA-LETI (France)

**Area 4: Advanced Memory Technology**

**G-1: DRAM**

**13:30-15:20 4F Hirose <Nishi>**

Chair: K. Hamada (Elpida Memory, Inc.)  
H. Hada (NEC Corp.)

**13:30 G-1-1 (Invited)**

Overview and Future Challenges of Capacitor-less DRAM  
Technologies for High Density Memory Applications  
P. Fazan, *Innovative Silicon S.A. (Switzerland)*

**14:00 G-1-2**

A Highly Scalable 4F<sup>2</sup> DRAM Cell Utilizing a Doubly  
Gated Vertical Channel  
W. Kwon and T. J. King. Liu, *Univ. of California Berkeley*  
(USA)

**14:20 G-1-3**

Highly Scalable Capacitorless DRAM Cell on Thin-Body

with Band-gap Engineered Source and Drain

P. Tang, D. Wu, L. Zhang and R. Huang, *Peking Univ.*  
(China)

**14:40 G-1-4**

Performance Improvement of the Capacitorless DRAM  
Cell with Quasi-SOI Structure Based on Bulk Substrate  
D. Wu, R. Huang, P. Tang, Y. Zhang and Y. Wang, *Peking*  
*Univ. (China)*

**15:00 G-1-5**

Seed layer and multistack approaches to reduce leakage in  
SrTiO<sub>3</sub>-based MIM capacitors using TiN bottom electrode  
N. Menou<sup>1</sup>, M. Popovici<sup>1</sup>, K. Opsomer<sup>1,2</sup>, B. Kaczer<sup>1</sup>,  
M. A. Pawlak<sup>1</sup>, A. Franquet<sup>1</sup>, C. Detavernier<sup>2</sup>, S. Van  
Elshocht<sup>1</sup>, D. J. Wouters<sup>1</sup>, S. Biesemans<sup>1</sup> and J. A. Kittl<sup>1</sup>,  
<sup>1</sup>IMEC and <sup>2</sup>Ghent Univ. (Belgium)

**15:20-16:00 Break**

**Area 4: Advanced Memory Technology**

**G-2: Flash Memory I**

**16:00-17:50 4F Hirose <Nishi>**

Chair: Y. Shimamoto (Hitachi, Ltd.)  
M. Moniwa (Renesas Tech. Corp.)

**16:00 G-2-1 (Invited)**

Electrical Defects in Dielectrics for Flash Memories  
Studied by Trap Spectroscopy by Charge Injection and  
Sensing (TSCIS)  
R. Degraeve, M. Cho, B. Govoreanu, B. Kaczer,  
M. B. Zahid, G. Van den bosch, J. Van Houdt, M. Jurczak  
and G. Groeseneken, *IMEC (Belgium)*

**16:30 G-2-2**

Charge Localization During Program and Retention in  
NROM-like Nonvolatile Memory Devices  
E. Nowak<sup>1</sup>, E. Vianello<sup>1,2</sup>, L. Perniola<sup>1</sup>, M. Bocquet<sup>1</sup>,  
G. Molas<sup>1</sup>, R. Kies<sup>1</sup>, M. Gely<sup>1</sup>, G. Ghibaudo<sup>3</sup>, B. D. Salvo<sup>1</sup>,  
G. Reimbold<sup>1</sup> and F. Boulanger<sup>1</sup>, <sup>1</sup>CEA-LETI/MINATEC,  
<sup>2</sup>Univ. of Udine and <sup>3</sup>IMEP/INPG (France)

**16:50 G-2-3**

Study of Transient Tunneling Current and Charge-Trapping Behaviors of SONOS-type Devices using Pulse-IV Technique

P. Y. Du<sup>1,2</sup>, H. T. Lue<sup>1</sup>, S. Y. Wang<sup>1</sup>, T. Y. Huang<sup>2</sup>, K. Y. Hsieh<sup>1</sup>, R. Liu<sup>1</sup> and C. Y. Lu<sup>1</sup>, <sup>1</sup>*Macronix Int'l Co., Ltd.* and <sup>2</sup>*National Chiao Tung Univ. (Taiwan)*

**17:10 G-2-4**

Roles of Traps Generated in Al<sub>2</sub>O<sub>3</sub> Film with respect to Memory Characteristics in MANOS

K. Akiyama, T. Ozaki, H. Higashijima, Y. Tanaka, T. Shibata, Y. Akasaka and T. Kaitsuka, *Tokyo Electron Ltd. (Japan)*

**17:30 G-2-5**

A New Method to Extract the Charge Centroid in the Program Operation of MONOS memories

S. Fujii, N. Yasuda, J. Fujiki and K. Muraoka, *Toshiba Corp. (Japan)*

**Area 5: Advanced Circuits and Systems**

**C-1: Interconnect-related Circuits Technology**

**13:30-15:40 2F Heisei <Nishi>**

Chair: M. Horiguchi (Renesas Tech. Corp.)  
T. Komuro (Kanagawa Inst. of Tech.)

**13:30 C-1-1 (Invited)**

Wireless CMOS TSV  
T. Kuroda, *Keio Univ. (Japan)*

**14:00 C-1-2**

Electromagnetic Interference and Susceptibility in Inductive-Coupling Link  
K. Kasuga, N. Miura, Y. Yuan, H. Ishikuro and T. Kuroda, *Keio Univ. (Japan)*

**14:20 C-1-3**

Design of On-Chip High Speed Interconnect on CMOS 180nm Technology  
T. Oshita, S. Amakawa, N. Ishihara and K. Masu, *Tokyo*

*Tech (Japan)*

**14:40 C-1-4**

A Novel CMOS 800 Mb/s BPSK Detector for IR-UWB Communication  
M. Hafiz, N. Sasaki and T. Kikkawa, *Hiroshima Univ. (Japan)*

**15:00 C-1-5**

A 3.5-4.5 GHz CMOS UWB Receiver Frontend LNA with On-chip Integrated Antenna for Inter-chip Communication  
A. Azhari, K. Kimoto, N. Sasaki and T. Kikkawa, *Hiroshima Univ. (Japan)*

**15:20 C-1-6**

Bitline-Capacitance-Insensitive Readout Circuit using Capacitive-Feedback Charge-Integration Scheme for Low-Voltage FeRAM  
K. Kotani, Y. Koshimoto and T. Ito, *Tohoku Univ. (Japan)*

**15:40-16:00 Break**

**Area 5: Advanced Circuits and Systems**

**C-2: Power Management and Advanced Mixed-Signal Technology**

**16:00-18:00 2F Heisei <Nishi>**

Chair: T. Komuro (Kanagawa Inst. of Tech.)  
Y. Sato (NTT Microsystem Integration Labs.)

**16:00 C-2-1 (Invited)**

Recent Topics in Power Management Circuits  
H. Kobayashi, *Gunma Univ. (Japan)*

**16:30 C-2-2**

An Enhanced PMOS Charge Pump for Low Supply Voltage Applications  
C. P. Hsu, H. M. Wu and H. Lin, *National Chung Hsing Univ. (Taiwan)*

**16:50 C-2-3 (Invited)**

CMOS Circuit Design Techniques for Millimeter-Wave

Applications

R. Fujimoto, T. Mitomo, H. Hoshino and  
Y. Yoshihara, *Toshiba Corp. (Japan)*

**17:20 C-2-4**

A 10-bit, 290 fJ/conv. Steps, 0.13mm<sup>2</sup>, Zero-Static Power,  
Self-Timed Capacitance to Digital Converter  
T. M. Vo, Y. Kuramochi, M. Miyahara, T. Karashina and  
A. Matsuzawa, *Tokyo Tech (Japan)*

**17:40 C-2-5**

Qpix, a Pixel Readout LSI with a Built-in ADC for  
Particle Detector Applications  
M. K. Vu, F. Li, M. Miyahara, T. Kurashina and  
A. Matsuzawa, *Tokyo Tech (Japan)*

**Area 6: Compound Semiconductor Circuits, Electron  
Devices and Device Physics**

**J-1: GaN FETs and RF Devices**

**13:30-15:45 6F Hagi**

Chair: M. Kuzuhara (Univ. of Fukui)  
K. J. Chen (Hong Kong Univ. of Sci. and Tech.)

**13:30 J-1-1 (Invited)**

Materials and Strain Issues in AlGaIn/GaN HEMT  
Degradation  
E. Muñoz<sup>1</sup>, C. Rivera<sup>1</sup>, F. Gonzalez-Posada<sup>1</sup>, A. Redondo<sup>1,2</sup>,  
F. Romero<sup>1</sup>, R. Cuerdo<sup>1</sup>, F. Calle<sup>1</sup>, R. Gago<sup>3</sup>, A. Jimenez<sup>4</sup>  
and C. Palacio<sup>2</sup>, <sup>1</sup>Univ. Politécnica de Madrid, <sup>2</sup>Univ.  
*Autónoma de Madrid*, <sup>3</sup>CSIC and <sup>4</sup>Univ. Alcalá de Henares  
(Spain)

**14:00 J-1-2**

Compressively Strained-In<sub>x</sub>Al<sub>1-x</sub>N/Al<sub>0.22</sub>Ga<sub>0.78</sub>N/GaN  
(x = 0.245 - 0.325) Heterostructures FETs with a Regrown  
AlGaIn Contact Layer  
M. Hiroki, N. Maeda and N. Shigekawa, *NTT Corp.*  
(Japan)

**14:15 J-1-3**

AlGaIn/GaN HFET using AlN/GaN Superlattice Barrier  
Layer  
S. Yagi, Y. Kawakami, X. Q. Shen, A. Nakajima,  
T. Ide and M. Shimizu, *AIST (Japan)*

**14:30 J-1-4**

Effect of GaN Growth Pressure on the Device  
Characteristics of AlGaIn/ GaN HEMTs on Silicon  
J. Selvaraj, S. Lawrence Selvaraj and T. Egawa, *Nagoya  
Inst. of Tech. (Japan)*

**14:45 J-1-5**

Evaluation of GaN MOSFET with TEOS SiO<sub>2</sub> Gate  
Insulator  
K. Nakatani<sup>1</sup>, J. P. Ao<sup>1</sup>, K. Ohmuro<sup>1</sup>, M. Sugimoto<sup>2</sup>,  
C. Y. Hu<sup>1</sup>, Y. Sogawa<sup>1</sup> and Y. Ohno<sup>1</sup>, <sup>1</sup>Univ. of Tokushima  
and <sup>2</sup>Toyota Motor Corp. (Japan)

**15:00 J-1-6**

Quasi-Normally-Off AlN/AlGaIn/GaN MIS HEMTs  
Grown on 4 in. Silicon Substrate  
S. Tan, S. Lawrence. Selvaraj and T. Egawa, *Nagoya Inst.  
of Tech. (Japan)*

**15:15 J-1-7**

Effective Heat Spreading with Separate Ohmic in AlGaIn/  
GaN HEMTs  
K. I. Lee<sup>1</sup>, J. H. Park<sup>1</sup>, H. J. Cho<sup>1</sup>, J. C. Her<sup>1</sup>, C. S. Yoo<sup>1,3</sup>,  
H. Y. Cha<sup>2</sup> and K. S. Seo<sup>1</sup>, <sup>1</sup>Seoul National Univ., <sup>2</sup>Hongik  
Univ. and <sup>3</sup>Korea Electronic Tech. Inst. (Korea)

**15:30 J-1-8**

GaN Zero-Bias RF Mixer using a Lateral Field-Effect  
Rectifier  
K. Y. Wong, W. J. Chen and K. J. Chen, *Hong Kong Univ.  
of Sci. and Tech. (China)*

**15:45-16:00 Break**

**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**

**J-2: III-V High-mobility Channel Devices**

**16:00-18:15 6F Hagi**

Chair: S. Tanaka (Shibaura Inst. of Tech.)

Y. Miyamoto (Tokyo Tech)

**16:00 J-2-1 (Invited)**

High-Performance Inversion-Mode III-V MOSFETs

Enabled by Atomic-Layer-Deposited High-k Dielectrics

P. D. Ye, *Purdue Univ. (USA)*

**16:30 J-2-2**

Fabrication of InP/InGaAs Undoped Channel MOSFET

with Selectively Regrown N<sup>-</sup>-InGaAs Source Region

T. Kanazawa, H. Saito, K. Wakabayashi, T. Tajima,

R. Terao, Y. Miyamoto and K. Furuya, *Tokyo Tech (Japan)*

**16:45 J-2-3**

Heteroepitaxy of Si<sub>x</sub>Ge<sub>1-x</sub> (x < 5%) Source/Drain on GaAs

Substrates for the Application of III-V MOSFETs

Z. Y. Han<sup>1</sup>, G. L. Luo<sup>2</sup>, S. C. Huang<sup>2</sup>, C. H. Ko<sup>3</sup>,

C. H. Wann<sup>3</sup>, H. Y. Lin<sup>3</sup>, C. T. Chung<sup>1</sup>, C. C. Cheng<sup>1</sup>,

C. Y. Chang<sup>1</sup> and C. H. Chien<sup>1,2</sup>, <sup>1</sup>*National Chiao*

*Tung Univ.*, <sup>2</sup>*National Nano Device Lab.* and <sup>3</sup>*Taiwan*

*Semiconductor Manufac. Co., Ltd. (Taiwan)*

**17:00 J-2-4 (Invited)**

Performance Projection of III-V and Ge Channel

MOSFETs

H. Tsuchiya, A. Maenaka, T. Mori and Y. Azuma, *Kobe*

*Univ. (Japan)*

**17:30 J-2-5**

Metalorganic Vapor Phase Epitaxy of GaAs with

ALP Surface Passivation Layer for Improved MOS

Characteristics

Y. Terada, M. Deura, Y. Shimogaki,

Y. Nakano and M. Sugiyama, *Univ. of Tokyo (Japan)*

**17:45 J-2-6**

Investigation of Strained-Sb Hetrostructures with High Hole Mobility

A. Nainani<sup>1</sup>, M. Kobayashi<sup>1</sup>, D. Witte<sup>1</sup>, T. Irisawa<sup>1</sup>,

T. Krishnamohan<sup>1</sup>, K. Saraswat<sup>1</sup>, B. R. Bennett<sup>2</sup>,

M. G. Ancona<sup>2</sup> and J. B. Boos<sup>2</sup>, <sup>1</sup>*Stanford Univ.* and <sup>2</sup>*Naval*

*Res. Lab. (USA)*

**Area 7: Photonic Devices and Device Physics**

**I-1: Si Photonics and Photonic Crystals**

**13:30-15:45 6F Kaede**

Chair: H. Yamada (Tohoku Univ.)

Y. Lee (Hitachi, Ltd.)

**13:30 I-1-1 (Invited)**

Active Ge based Devices for Silicon Photonics

J. Michel, J. Liu, X. Sun, M. Beals, L. C. Kimerling, *MIT*

*(USA)*

**14:00 I-1-2**

Compact and Polarization-Independent Variable Optical

Attenuator Based on a Silicon Photonic Wire Waveguide

with Carrier Injection Structure

H. Nishi, T. Tsuchizawa, K. Yamada, T. Watanabe,

H. Shinojima and S. Itabashi, *NTT Corp. (Japan)*

**14:15 I-1-3**

Si Wire Waveguide Polarization Independent Optical

Wavelength Filters

H. Okayama, K. Kotani, Y. Maeno, D. Shimura,

H. Yaegashi and Y. Ogawa, *OKI Electric Industry Co., Ltd.*

*(Japan)*

**14:30 I-1-4**

Reducing Operation Voltage of Silicon-Ring Optical

Modulator using High-k Cladding Layer

Y. Amemiya, M. Nishida, H. Ding, M. Fukuyama and

S. Yokoyama, *Hiroshima Univ. (Japan)*

**14:45 I-1-5**

The Approach to Dislocation-free Ge Mesa on Si Fabricated by Dry Etching  
Y. Takada, J. Osaka, Y. Ishikawa and K. Wada, *Univ. of Tokyo (Japan)*

**15:00 I-1-6**

A Photonic Modulator based on a Semiconductor Soliton Device  
M. C. Shih, W. C. Su, I. T. Shu and W. S. Shei, *National Univ. of Kaohsiung (Taiwan)*

**15:15 I-1-7**

Demonstration of Quality Factor over 10,000 in Three-Dimensional Photonic Crystal Nanocavity by Cavity Size Control  
A. Tandraechanurat, S. Ishida, K. Aoki, D. Guimard, D. Bordel, M. Nomura, S. Iwamoto and Y. Arakawa, *Univ. of Tokyo (Japan)*

**15:30 I-1-8**

Analysis of Two-Dimensional Photonic Crystal Cavities with Low Refractive Index Material Cladding  
T. Yamada<sup>1,2</sup>, M. Okano<sup>2</sup>, J. Sugisaka<sup>1,2</sup>, N. Yamamoto<sup>2</sup>, M. Itoh<sup>1</sup>, T. Sugaya<sup>2</sup>, K. Komori<sup>2</sup> and M. Mori<sup>2</sup>, *<sup>1</sup>Univ. of Tsukuba and <sup>2</sup>AIST (Japan)*

**15:45-16:00 Break**

**Area 7: Photonic Devices and Device Physics**

**I-2: Si Lightemitter and THz Laser**

**16:00-18:15 6F Kaede**

Chair: H. Isshiki (Univ. of Electro-Communications)  
M. Gotoda (Mitsubishi Electric Corp.)

**16:00 I-2-1 (Invited)**

Optical Gain in Ultra-Thin Silicon Resonant Cavity Light-Emitting Diode  
S. Saito<sup>1,2</sup>, Y. Suwa<sup>1</sup>, N. Sakuma<sup>1</sup>, H. Arimoto<sup>1</sup>, D. Hisamoto<sup>1,2</sup>, H. Uchiyama<sup>1,2</sup>, J. Yamamoto<sup>1</sup>, T. Sakamizu<sup>1</sup>, T. Mine<sup>1</sup>, S. Kimura<sup>1</sup>, T. Sugawara<sup>1</sup> and M.

Aoki<sup>1,2</sup>, *<sup>1</sup>Hitachi Ltd. and <sup>2</sup>SORST-JST (Japan)*

**16:30 I-2-2**

PL Enhancement of Si Ring Resonators by Hydrogen Plasma Treatment  
Y. Wang<sup>1</sup>, J. Cai<sup>1</sup>, S. Lin<sup>1</sup>, Y. Ishikawa<sup>1</sup>, Y. Yamashita<sup>2</sup>, Y. Kamiura<sup>2</sup> and K. Wada<sup>1</sup>, *<sup>1</sup>Univ. of Tokyo and <sup>2</sup>Okayama Univ. (Japan)*

**16:45 I-2-3**

Enhanced Room-Temperature 1.6  $\mu\text{m}$  Electroluminescence from Si-Based Double Heterostructures Light-Emitting Diodes using Iron Disilicide  
M. Suzuno, T. Koizumi, H. Kawakami and T. Suemasu, *Univ. of Tsukuba (Japan)*

**17:00 I-2-4**

Fabrication and Optical Characterization of Self-standing Wide-gap Nanocrystalline Silicon Layers  
R. Mentek, B. Gelloz and N. Koshida, *Tokyo Univ. of Agri. and Tech. (Japan)*

**17:15 I-2-5**

Monolithic Integration of Si-Dot Light Emitting Diodes, Si Photodiodes, and Spin-Coated Optical Waveguides on Si LSI  
T. Tabei<sup>1</sup>, K. Maeda<sup>2</sup>, S. Yokoyama<sup>1</sup> and H. Sunami<sup>1</sup>, *<sup>1</sup>Hiroshima Univ. and <sup>2</sup>Central Glass Co., Ltd. (Japan)*

**17:30 I-2-6**

Low Reflection Optical Coupling for Hybrid Integrated Wavelength Tunable Laser with Silicon Waveguide Ring Resonators  
N. Fujioka<sup>1,2</sup>, T. Chu<sup>1,2</sup>, S. Nakamura<sup>1</sup> and M. Ishizaka<sup>1,2</sup>, *<sup>1</sup>NEC Corp. and <sup>2</sup>OITDA (Japan)*

**17:45 I-2-7**

Performance Comparison of Terahertz Quantum Cascade Lasers Predicted by Non-equilibrium Green's Function Method  
H. Yasuda<sup>1,2</sup>, T. Kubis<sup>3</sup>, P. Vogl<sup>3</sup>, N. Sekine<sup>2</sup>, I. Hosako<sup>2</sup> and

K. Hirakawa<sup>1</sup>, <sup>1</sup>Univ. of Tokyo, <sup>2</sup>NICT and <sup>3</sup>Tech. Univ. of Munich (Japan)

**18:00 I-2-8**

Terahertz Laser on Optically Pumped Graphene: Concept and its Substantiation

A. Dubinov<sup>1,2</sup>, V. Aleshkin<sup>2</sup>, M. Ryzhii<sup>1,4</sup>, T. Otsuji<sup>3,4</sup> and V. Ryzhii<sup>1,4</sup>, <sup>1</sup>Univ. of Aizu, <sup>2</sup>Inst. For Physics of Microstructures RAS, <sup>3</sup>Tohoku Univ. and <sup>4</sup>CREST-JST (Japan)

**Area 8: Advanced Material Synthesis and Crystal Growth Technology**

**H-1: SiGe Related Technologies and III-V Nano Structures**

**13:30-15:45 6F Kiri**

Chair: A. Yamada (Tokyo Tech)

H.H.Tan (The Australian National Univ.)

**13:30 H-1-1**

Epitaxial growth and defect generation in in-situ doped high percentage SiGe

A. Reznicek, T. N. Adam, Z. Zhu, K. E. Fogel, J. Li, L. Tai, P. Kulkarni, J. Kim, S. W. Bedell and D. K. Sadana, IBM (USA)

**13:45 H-1-2**

Study on SiGe Film Properties Fabricated using a Reactive Thermal CVD Method

M. Wakagi<sup>1</sup>, I. Suzumura<sup>1</sup>, H. Asanuma<sup>1</sup>, E. Nishimura<sup>1</sup>, M. Matsumura<sup>1</sup>, A. Kagatsume<sup>1</sup> and J. Hanna<sup>2</sup>, <sup>1</sup>Hitachi, Ltd. and <sup>2</sup>Tokyo Tech (Japan)

**14:00 H-1-3**

Compressively strained Ge channel heterostructures grown by RP-CVD for the next generation CMOS Devices

M. Myronov, V. A. Shah, A. Dobbie, X. C. Liu, V. H. Nguyen and D. R. Leadley, Univ. of Warwick (UK)

**14:15 H-1-4**

Formation of High Ge Concentration Virtual Substrate by Laser Annealing

C. Y. Ong<sup>1</sup>, K. L. Pey<sup>1</sup>, J. P. Liu<sup>2</sup>, Q. Wang<sup>2</sup>, C. P. Wong<sup>1</sup>, Z. X. Shen<sup>1</sup>, X. C. Wang<sup>3</sup>, H. Zheng<sup>3</sup>, C. M. Ng<sup>2</sup> and L. Chan<sup>2</sup>, <sup>1</sup>Nanyang Technological Univ., <sup>2</sup>Chartered Semiconductor Manufacturing Ltd. and <sup>3</sup>Singapore Inst. Of Manufacturing Tech. (Singapore)

**14:30 H-1-5**

Low Temperature (375°C) Metal Induced Lateral Crystallization (MILC) of Si<sub>1-x</sub>Ge<sub>x</sub> (0 ≤ x ≤ 1) using Silicide/Germanide Forming Metals (Ni, Pd and Co)

T. H. Phung<sup>1</sup>, R. Xie<sup>1,2</sup>, S. Tripathy<sup>3</sup>, M. Yu<sup>2</sup> and C. Zhu<sup>1</sup>, <sup>1</sup>National Univ. of Singapore, <sup>2</sup>Inst. of Microelectronics and <sup>3</sup>Inst. of Materials Res. and Eng. (Singapore)

**14:45 H-1-6**

Low-dislocation-density 50nm Ge Fin Fabrication on Si substrate

C. T. Chung<sup>1</sup>, S. C. Huang<sup>2</sup>, G. L. Luo<sup>2</sup>, C. H. Ko<sup>3</sup>, C. H. Wann<sup>3</sup>, H. Y. Lin<sup>3</sup>, Z. Y. Han<sup>1</sup>, C. C. Cheng<sup>1</sup> and C. H. Chien<sup>1,2</sup>, <sup>1</sup>National Chiao Tung Univ., <sup>2</sup>National Nano Device Lab. and <sup>3</sup>TSMC (Taiwan)

**15:00 H-1-7**

Positioning and numbering Ge quantum dots for effective quantum electrodynamic devices

K. H. Chen, C. Y. Chien, W. T. Lai and P. W. Li, National Central Univ. (Taiwan)

**15:15 H-1-8**

Grazing Incidence X-ray Diffraction Measurements of Columnar InAs/GaAs Quantum-Dot Structures

K. Watanabe, Y. Kimura and K. Mukai, Yokohama National Univ. (Japan)

**15:30 H-1-9**

Growth and Characterization of InGaAs Nanowires formed on GaAs(111)B by Selective-Area Metal Organic Vapor Phase Epitaxy

M. Yoshimura, K. Tomioka, K. Hiruma, S. Hara,  
J. Motohisa and T. Fukui, *Hokkaido Univ. (Japan)*

**15:45-16:00 Break**

**Area 8: Advanced Material Synthesis and Crystal Growth Technology**

**H-2: Graphen and Nanowires**

**16:00-18:15 6F Kiri**

Chair: H. Hibino (NTT Basic Res. Labs.)  
K.Horn (Fritz Haber Inst.)

**16:00 H-2-1 (Invited)**

III-V Nanowires Grown by MOCVD for Optoelectronics Applications

H. H. Tan, Q. Gao, H. J. Joyce, J. H. Kang, S. Paiman,  
J. Wong-Leung, J. Zou, M. Paladuqu, Y. Guo, H. Wang,  
X. Zhang and C. Jagadish, *Australian National Univ. (Australia)*

**16:30 H-2-2 (Invited)**

Growth and Electronic Structure of Epitaxial Graphene on Silicon Carbide

A. Bostwick<sup>1</sup>, E. Rotenberg<sup>1</sup>, J. McChesney<sup>1,2</sup>, T. Ohta<sup>1,2</sup>,  
T. Seyller<sup>3</sup> and K. Horn<sup>2</sup>, <sup>1</sup>*ALS. Lawrence Berkeley Lab.*,  
<sup>2</sup>*Fritz Haber Inst.* and <sup>3</sup>*Univ. Erlangen (USA)*

**17:00 H-2-3**

Thin Graphitic Structure Formation on Various Substrates by Gas-Source Molecular Beam Epitaxy using Cracked-Ethanol

F. Maeda and H. Hibino, *NTT Basic Res. Labs. (Japan)*

**17:15 H-2-4**

Effect of Carrier Gas (Ar and He) on the Crystallographic Quality of Multi-layer Graphene Grown on Si by Photoemission-assisted Plasma CVD

H. Sumi<sup>1</sup>, S. Ogawa<sup>1,2</sup>, A. Saikubo<sup>2,3</sup>, E. Ikenaga<sup>2,3</sup>,  
M. Nihei<sup>2,4</sup> and Y. Takakuwa<sup>1,2</sup>, <sup>1</sup>*Tohoku Univ.*, <sup>2</sup>*CREST-JST*,  
<sup>3</sup>*JASRI/SPring-8* and <sup>4</sup>*Fujitsu Ltd. (Japan)*

**17:30 H-2-5**

Electronic Structure of Carbon Nanowalls using Resonant Soft-X-Ray Emission Spectroscopy

W. Takeuchi<sup>1</sup>, M. Hiramatsu<sup>2</sup>, Y. Tokuda<sup>3</sup>, H. Kano<sup>4</sup>,  
T. Kinoshita<sup>5</sup>, Y. Kato<sup>5</sup>, T. Muro<sup>5</sup>, S. Kimura<sup>5</sup> and M. Hori<sup>1</sup>,  
<sup>1</sup>*Nagoya Univ.*, <sup>2</sup>*Aichi Inst. of Tech.*, <sup>3</sup>*Meijo Univ.*, <sup>4</sup>*NU Eco-Engi. Co., Ltd.* and <sup>5</sup>*JASRI/Spring-8 (Japan)*

**Area 9: Physics and Applications of Novel Functional Materials and Devices**

**K-1: Single Electron and Quantum Transport**

**13:30-15:45 6F Aoi**

Chair: M. Tabe (Shizuoka Univ.)  
Martin Brandt S. (Walter Schottky Institut,  
Technische Universitat Munchen)

**13:30 K-1-1 (Invited)**

From Single-atom Spectroscopy to Lifetime Enhanced Triplet Transport in MOSFETs

J. Verduijn<sup>1</sup>, G. P. Lansbergen<sup>1</sup>, G. C. Tettamanzi<sup>1</sup>,  
R. Rahman<sup>2</sup>, S. Biesemans<sup>2</sup>, N. Colleart<sup>3</sup>, G. Klimeck<sup>2</sup>,  
L. C. L. Hollenberg<sup>4</sup> and S. Rogge<sup>1</sup>, <sup>1</sup>*Delft Univ. of Tech.*, <sup>2</sup>*Purdue Univ.*, <sup>3</sup>*IMEC* and <sup>4</sup>*Univ. of Melbourne (Netherlands)*

**14:00 K-1-2**

Single-Electron Transport through Discrete Dopants

D. Moraru<sup>1</sup>, M. Anwar<sup>1</sup>, M. Ligowski<sup>1,2</sup>, S. Miki<sup>1</sup>,  
R. Nakamura<sup>1</sup>, T. Mizuno<sup>1</sup>, R. Jablonski<sup>2</sup> and M. Tabe<sup>1</sup>,  
<sup>1</sup>*Shizuoka Univ.* and <sup>2</sup>*Warsaw Univ. of Tech. (Japan)*

**14:15 K-1-3**

Tunnel Spectroscopy of Electron Subbands in Thin SOI MOSFETs

J. Noborisaka, K. Nishiguchi, H. Kageshima, Y. Ono and  
A. Fujiwara, *NTT Corp. (Japan)*

**14:30 K-1-4**

Si SET-based Flexible Multi-valued Half Adder Logic Cell  
S. J. Kim<sup>1</sup>, E. S. Park<sup>1</sup>, S. J. Shin<sup>1</sup>, J. B. Choi<sup>1</sup> and

Y. S. Yu<sup>2</sup>, <sup>1</sup>Chungbuk National Univ. and <sup>2</sup>Hankyong National Univ (Korea)

**14:45 K-1-5**

Dual-Gate Single-Electron Transistors (DG-SETs) with Silicon Nano-Wire Channel and Surrounding Side Gates  
D. S. Lee, K. C. Kang, J. E. Lee, H. S. Yang, J. H. Lee and B. G. Park, *Seoul National Univ. (Korea)*

**15:00 K-1-6**

Dislocation-Based Si-Nanodevices  
M. Reiche<sup>1</sup>, M. Kittler<sup>2</sup>, D. Buca<sup>3</sup>, A. Hähnel<sup>1</sup>, Q. T. Zhao<sup>3</sup>, S. Mantl<sup>3</sup> and U. Gösele<sup>1</sup>, <sup>1</sup>Max-Planck-Institut für Mikrostrukturphysik, <sup>2</sup>IHP Frankfurt and <sup>3</sup>Forschungszentrum Jülich (Germany)

**15:15 K-1-7**

Slow and Fast Electron Channels in a Coherent Quantum Dot Mixer  
D. G. Austing<sup>1,2</sup>, C. Payette<sup>1,2</sup>, G. Yu<sup>1</sup>, J. Gupta<sup>1</sup>, G. Aers<sup>1</sup>, S. Nair<sup>3</sup>, S. Amaha<sup>4</sup> and S. Tarucha<sup>4,5</sup>, <sup>1</sup>National Res. Council, <sup>2</sup>McGill Univ., <sup>3</sup>Univ. of Toronto, <sup>4</sup>JST and <sup>5</sup>Univ. of Tokyo (Canada)

**15:30 K-1-8**

Series Coupled Vertical Triple Quantum Dot Structures  
S. Amaha<sup>1</sup>, T. Hatano<sup>1</sup>, K. Ono<sup>2</sup>, Y. Tokura<sup>1,3</sup>, S. Tarucha<sup>1,4</sup>, J. Gupta<sup>5</sup> and D. G. Austing<sup>5</sup>, <sup>1</sup>ICORP-JST, <sup>2</sup>RIKEN, <sup>3</sup>NTT Corp., <sup>4</sup>Univ. of Tokyo and <sup>5</sup>National Res. Council of Canada (Japan)

**15:45-16:00 Break**

**Area 9: Physics and Applications of Novel Functional Materials and Devices**

**K-2: Thinfilm Transistor and Memory****16:00-17:45 6F Aoi**

Chair: Y. Uraoka (NAIST)  
P. W. Li (National Central Univ.)

**16:00 K-2-1**

New Tunneling Model with Dependency of Temperature

Measured in Si Nano-Dot Floating Gate MOS Capacitor  
M. Muraguchi<sup>1</sup>, Y. Sakurai<sup>2</sup>, Y. Takada<sup>2</sup>, Y. Shigeta<sup>4</sup>, M. Ikeda<sup>3</sup>, K. Makihara<sup>3</sup>, S. Miyazaki<sup>3</sup>, S. Nomura<sup>2</sup>, K. Shiraishi<sup>2</sup> and T. Endoh<sup>1</sup>, <sup>1</sup>Tohoku Univ., <sup>2</sup>Univ. of Tsukuba, <sup>3</sup>Hiroshima Univ. and <sup>4</sup>Univ. of Hyogo (Japan)

**16:15 K-2-2**

Light Induced Carrier Transfer in NiSi-Nanodots/Si-Quantum-Dots Hybrid FG in MOS Structures  
N. Morisawa, M. Ikeda, S. Nakanishi, A. Kawanami, K. Makihara and S. Miyazaki, *Hiroshima Univ. (Japan)*

**16:30 K-2-3**

TFT-type Flash Memory with Biomineralized Nanodots on SOI Substrate  
K. Ohara<sup>1</sup>, I. Yamashita<sup>1</sup> and Y. Uraoka<sup>1,2</sup>, <sup>1</sup>NAIST and <sup>2</sup>CREST (Japan)

**16:45 K-2-4**

Device Design Schemes and Electrical Characterization of Nonvolatile Memory Thin-Film Transistors with the Gate Structure of Al/P(VDF-TrFE)/Al<sub>2</sub>O<sub>3</sub>/ZnO  
S. M. Yoon, S. H. Yang, S. H. Ko Park, S. W. Jung, C. W. Byun, D. H. Cho, S. Y. Kang, C. S. Hwang and B. G. Yu, *ETRI (Korea)*

**17:00 K-2-5**

I-V Measurement of Pr<sub>0.7</sub>Ca<sub>0.3</sub>MnO<sub>3</sub> during TEM Observation  
T. Fujii, H. Kaji, H. Kondou, K. Hamada, M. Arita and Y. Takahashi, *Hokkaido Univ. (Japan)*

**17:15 K-2-6**

Resistance switching memory using Si/CaF<sub>2</sub>/CdF<sub>2</sub> quantum-well structures  
M. Watanabe, R. Hirasawa and Y. Nakashouji, *Tokyo Tech (Japan)*

**17:30 K-2-7**

Self-aligned Metal Double-gate P-channel Low-temperature Poly-Si TFTs Fabricated by DPSS CW Green

Laser Lateral Crystallization

T. Sato<sup>1</sup>, K. Hirose<sup>2</sup>, K. Kitahara<sup>2</sup> and A. Hara<sup>1</sup>, <sup>1</sup>*Tohoku Gakuin Univ. and* <sup>2</sup>*Shimane Univ. (Japan)*

**Area 10: Organic Materials Science, Device Physics, and Applications**

**F-1: Organic Photonic Photovoltaic Device & Memory**

**13:30-15:45 4F Hirose <Higashi>**

Chair: K. Fujita (Kyushu Univ.)

S. Aramaki (Mitsubishi Chemical Group Sci. & Tech. Res. Center, Inc.)

**13:30 F-1-1 (Invited)**

Efficient Organic p-i-n Solar Cells Having Very Thick Codeposited i-layer using Seven-nine Purified Fullerene  
M. Hiramoto, *IMS (Japan)*

**14:00 F-1-2**

Efficiency Improvement of Organic Solar Cells by Hot-Pressing

C. F. Shih, K. T. Hung, J. W. Wu, C. Y. Hsiao and W. M. Li, *National Cheng Kung Univ. (Taiwan)*

**14:15 F-1-3**

Fabrication and Photocurrent Generation of Composite Film of C<sub>60</sub> Fullerene-Ethylenediamine Adduct and a Polythiophene

T. Akiyama, S. Matsumura, H. Seo, K. Matsuoka and S. Yamada, *Kyushu Univ. (Japan)*

**14:30 F-1-4**

Accurate Derivation of All Parameters of the Single Diode Model from a Single Current-voltage Characteristic of a Solar Cell using an Extensively Valid and Stable Iterative Calculation Method

M. M. Rahman, R. Kojima, K. Ishibashi, Y. Kimura and M. Niwano, *Tohoku Univ. (Japan)*

**14:45 F-1-5**

Single Donor-Acceptor Heterojunction Organic

Photovoltaic Cell with an AgO-Based Anode

C. S. Ho<sup>1</sup>, W. C. Hsu<sup>1</sup>, C. S. Lee<sup>2</sup>, K. H. Hsiao<sup>1</sup> and W. H. Lai<sup>1</sup>, <sup>1</sup>*National Cheng Kung Univ. and* <sup>2</sup>*Feng Chia Univ. (Taiwan)*

**15:00 F-1-6**

Development of FET Type Photorewritable Memory using Photochromic Interface Layer

M. Yoshida, K. Suemori, S. Uemura, S. Hoshino, N. Takada, T. Kodzasa and T. Kamata, *AIST (Japan)*

**15:15 F-1-7**

The Effects of an Electric-field Application on Properties of P(VDF-TeFE) Thin Film

J. H. Jeong, H. Aoki, C. Kimura and T. Sugino, *Osaka Univ. (Japan)*

**15:30 F-1-8**

Influence of Substitution Group of the Side Chain of Polypeptide on the Morphology and its Hysteresis Property as a Ferroelectric Memory Device

T. Inomata<sup>1</sup>, N. Kobayashi<sup>1</sup>, S. Uemura<sup>2</sup> and T. Kamata<sup>2</sup>, <sup>1</sup>*Chiba Univ. and* <sup>2</sup>*AIST (Japan)*

**15:45-16:00 Break**

**Area 10: Organic Materials Science, Device Physics, and Applications**

**F-2: Organic Transistor**

**16:00-18:00 4F Hirose <Higashi>**

Chair: M. Nakamura (Chiba Univ.)

T. Kamata (AIST)

**16:00 F-2-1 (Invited)**

Electrical and environmental stability of organic transistors

A. Benor<sup>1</sup>, J. E. Northrup<sup>2</sup>, A. Hoppe<sup>1</sup>, V. Wagner<sup>1</sup> and D. Knipp<sup>1</sup>, <sup>1</sup>*Jacobs Univ. and* <sup>2</sup>*Electronic Materials and Devices Lab. (USA)*

**16:30 F-2-2**

Effect of Carrier Trap on the Electron Transport

## Wednesday, October 7

in Pentacene FET Observed by the Time-resolved  
Microscopic SHG Measurement

T. Manaka, F. Liu, M. Nakao, W. Martin and M. Iwamoto,  
*Tokyo Tech (Japan)*

### 16:45 F-2-3

Field-Induced Electron Spin Resonance Spectroscopy for  
Density of Trap States in Organic Transistors

H. Matsui<sup>1,2</sup>, A. S. Mishchenko<sup>3,4</sup> and T. Hasegawa<sup>1</sup>, <sup>1</sup>*AIST*,  
<sup>2</sup>*Univ. of Tokyo*, <sup>3</sup>*RIKEN* and <sup>4</sup>*RRC Kurchatov Inst. (Japan)*

### 17:00 F-2-4

Observation of Electric Field in Tetracene Field-Effect  
Transistor using Optical Second Harmonic Generation

Y. Ohshima, H. Satou, H. Kohn, T. Manaka and M.  
Iwamoto, *Tokyo Tech (Japan)*

### 17:15 F-2-5

Enhancing Mobility in Pentacene TFTs using the Film  
deposition in H<sub>2</sub> on Octadecyltrichlorosilane (OTS)  
Treated SiO<sub>2</sub>

T. Yokoyama, C. B. Park, K. Nagashio, K. Kita and  
A. Toriumi, *Univ. of Tokyo (Japan)*

### 17:30 F-2-6

Organic Thin Film Transistors with Tailored Liquid  
Sources of HfO<sub>2</sub> as High-κ Insulator

R. Nishizawa<sup>1</sup>, S. Naka<sup>1</sup>, H. Okada<sup>1</sup>, K. Suzaki<sup>2</sup> and  
K. Kato<sup>2</sup>, <sup>1</sup>*Univ. of Toyama* and <sup>2</sup>*AIST (Japan)*

### 17:45 F-2-7

Interface Charging Propagation Model for Carrier  
Migration in OFET

M. Weis, D. Taguchi, J. Lin, T. Manaka and M. Iwamoto,  
*Tokyo Tech (Japan)*

<b>Banquet/Paper Award and Young Researcher Award</b>
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19:30-21:30 2F Heisei