Improved the power efficiency of white phosphor organic light-emitting diodes with thin double-emission-layers and hole-trapping mechanism

F. S. Jiang, S. H. Wang; Y. S. Tsai, M. H. Gan; Y. Chi and H. F. Shei
National Formosa Univ.; National Tung Hua Univ. and National Chiao Tung Univ. (Taiwan)
High-efficiency white PHOLEDs can be achieved by using thin double-emission-layers and doping red phosphor on interface to suppress two emission layers. The yield and power efficiency reach 23.3 cd/A and 1.7 lm/mm² at 1000 cd/m².

Current Density Dependence of Transient Properties in Green Phosphorescent Organic Light-Emitting Diodes

H. Kaji, N. Takatoh, Y. Wang and Y. Ohnuki
Osaka Univ (Japan)
We studied the current density dependence of transient characteristics of green phosphorescent OLEDs. We discussed the transient electro-luminescence of green phosphorescent OLEDs using pulses of alternating current sine-waves with various frequencies.

High efficiency phosphorescent organic light-emitting diode by incorporating an electron transport material into emitting layer

F. S. Jiang, S. H. Wang; Y. K. Tsai; B. S. Hsieh; Y. Chi and H. P. Shieh
National Formosa Univ.; National Tung Hua Univ. and National Chiao Tung Univ. (Taiwan)
Hole transport-type host (TCTA) and electron transport material (TmPyPB) incorporated as mixed-host structure to improve the injection of carriers. While PHOLED showed the yield of 32 cd/A and power efficiency of 20 lm/W (1000 cd/m²).

Fermi-level Planing and NBTI Free of CMOS HFO, By Prec-FP, Plasma Passivation

H. H. Chiu, C. S. Lai and J. C. Wang
Chung Cheng Univ. (Taiwan)
Advanced performance and reliability were achieved with a zero-tail CMOS by CF4 plasma pre-treatment. A new physical model of interfacial reaction suppression and F-re-incorporation were presented to explain FLIP free and turn-around NBTI phenomena.

Drive Current Improvement in Si Tunnel Field Effect Transistors by means of Silicidie Engineer

IMEC and Katholieke Univ. Leuven (Belgium)
We report a novel Si Multiple Gate Tunnel Field Effect Transistor (MuTFTET) with high-k gate-dielectric and metal gate with enhanced field by silicidie enrichment. The MuTFTET device exhibit a record-on-state current of 70µA/mm at VDS of -0.99 and ILHINR of 4.2, LWR. Temperature measurements and TCAD simulations confirm the presence of multiple transport mechanisms which explain the degradation of the subthreshold swing.

Enhanced Electrical Uniformity and Breakdown of Multi-Step Deposited and Annealed HfSiOx - Insight by Scanning Tunneling Microscopy

K. Xue, D. S. Ang, K. L. Pei, G. Bernardi, P. S. Laszloy and D. Hei
Nanyang Tech. Univ. and SEMATECH (Singapore)
Grain-boundaries in crystallized high-k film have been shown to induce higher voltage loading on underlying IL, therefore accelerating stack break-down. Through STM characterization, we show directly multi-step depositions and annealing process improve electrical breakdown and high-k film.

Metal Schottky/Si Technology of Ultra Thin STOT (Silicon on Thin Box) MOSFET

A. Shima, N. Sagi, N. Miy, D. Hisamoto, K. Tsuchida and K. Torii
Hokkaido Univ. and Hokkaido Univ. (Japan)
We report a novel approach to decrease the parasitic resistance in UT-SiO1.6 MOSFET utilizing metal Schottky rise/Si-Selective deposited NWS2 with dopant segregation fabrication by laser spike annealing lowered effective SiH6 and the contact resistance.

High performance GaN-based light emitting diodes grown on 4-inch Si (111)

Y. Zhu, A. Watanabe, L. Z. Chen and T. Egawa
Nagoya Inst. of Tech. (Japan)
GaN-based LEDs grown on 4-inch Si (111) substrate by MOCVD have been demonstrated. The light output power can be improved by increasing the thickness of n-GaN with the maximum value of 1.7 mm.

Atomic Design of Guiding Principles for High performance MONOS Memories-First Principles Study of H and O Incorporation Effects for N Vacancies in Si Charge Trap Layers

K. Yamaguchi, A. Oku and K. Shichida
Univ. of Tokyo (Japan)
We found N vacancies in Si layer are suitable charge traps for MONOS-type memory based on first principles calculations. N vacancy maintains its high P/E endurance characteristics even when H and O atoms are incorporated.
Transport material into emitting layer by incorporating an electron structure to improve the injection of carriers. White and further enhance the luminous efficiency.

Metal compound (CsI) is firstly doped into Alq3. T. W. Kuo, S. H. Su, C. M. Wu and M. Yokoyama, Tung Univ. (Taiwan)

Improved the power efficiency of white phosphorescent OLEDs using pulses transient characteristics of green phosphorescent H. Kajii, N. Takahota, Y. Wang and Y. Ohmori, National Chiao, M. H. Gao, B. S. Hsieh, Nanyang Tech. Univ. and Takeda and K. Torii, Hitachi, Ltd. (Japan)

Metal Schottky S/D Technology of Ultra Thin Silicon ρ-channel Tunnel FET technology challenges of 3D CT NAND and the sight is very important to design for MLC CT-cell.

We demonstrated that nearly double the wall-effect density and the better carrier confinement from enhancement in light output power as compared Koide and H. J. Mattausch, Hiroshima Univ. (Japan)

High-k MOS Diodes on a Si (111) Substrate Grown by Surface Reconstruction Controlled Epitaxy K. Shiraishi (Univ. of Tsukuba)

Optical properties of ZnO/Al core/shell nanow. Y. H. Kuo and J. S. Yu, Kuang Hs. Univ. (Korea)

We fabricated the Au/ZnO core/shell nano-tips (NTs) by hydrothermal and thermal evaporation because the Au has excellent stability for acid dyes in ZnO doped sensitized solar cells and good capacity to enhance the light absorption.


We investigated the relationship between the structure and measurement of the ZnO nanocylinders by in situ TEM. The results show that the ZnO NCs do not have rectification property but linear relation showed by I-V curve.

Effect of Fluorine Incorporation on WSix/Al2O3/ Hexagonal SiC MOSFETs. The transformation from pulse input signals to rectification property but liner relation showed by I-V curve.

We performed photoluminescence and photon effects in advanced CMOS technologies with strain recombination theory, it was found the concentration of holes near the interface.

Dielectric Constant Inter-Silicon Oxide/Al2O3 Contact Formation for Low-k dielectrics. The experimental results show that the capacitance of the oxide layer decreases but the device performance improves after fluorine treatment.

Optical properties of ZnO/Al core/shell nano-w. R. Y. Kuo, R. L. Lo, C. Y. C. Ong, C. S. Tsai, C. L. Guan, H. Chai, D. A. Antonides and E. Fitzgerald, Nanyang Tech. Univ. and Massachusetts Institute of Technology (Singapore)

We study the effect of Fluorine on the dielectric constant and the device performance varying two neighboring back-gate epitaxial graphene. For FETs. In this paper, we have performed a comparative study on performance potentials between bilayer graphene- and graphene-nanobelt-FETs based on a first-principles approach.

Performance Potentials of Bilayer Graphene and graphene Nanoribbon FETs H. Inokawa, H. Ando and H. Takeiwa, Kobe Univ. (Japan)

A new device is expected as a new channel material for FETs. In this paper, we have performed a comparative study on performance potentials between bilayer graphene- and graphene-nanobelt-FETs based on a first-principles approach.

Effect of surface and crystalline defects on reverse K. Ito, K. Mitsui, T. Yamasaki and Y. Nogusa, Keio Univ. (Japan)

We have proposed a novel patterning method of self-assembled monolayer (SAM) in nanopore using near-field photothermal desorption. This paper reports the patterning principle and the validity of the proposed method.

Positional control of crystal grains in silicon thin film utilizing caging shaped poly. F. Tepp, A. Mura, E. Sano and S. Sanso, Tottori Univ. (Japan)

We propose crystallization method of silicon thin film utilizing caging-shape polyethylene. We perform the selective adsorption of the dopants. The location control of crystal grain was successfully achieved with the optimal size at low temperature.


We report on the experimental logic inverter, using two neighboring back-gate epitaxial graphene-on-silicon FETs. The Inversion operation was obtained at less than 0.1V biased as 0.1V, with a matched input/output voltage.

High-k Hole current achievement of hydrogen- induced two dimensional diamond MOSFETs coated with Poly-tetra-fluoro-ethylene S. Sato, K. Tepe, T. Tao, T. Oto and H. Kadowa, Ritsumeikan Univ. (Japan)

We reported that a hydrogen-terminated diamond MOSFET coated with PTFE shows high drain current of ~1.2 A/mm and transconductance of 430 mS/mm. The highest current reported in diamond FETs to date.

Control of Activation Energy for Electron Trans. in Two-Dimensional Array of Si Nanodisks M. Iijarhi, C. H. Huang, T. Moris and S. Samu- toh, Tohoku Univ. and Kyusung Inst. of Tech. (Japan)

The transformation from pulse input signals to decayed analog outputs through 2D array of Si nanodisks was clearly observed. The activation energy for this transformation in this array could be controlled by changing the nanodisk thickness.
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10:00 A-3-5

Maskless Patterning of Vapor-Deposited Photosensitive Film and Its Application to Organic Light-Emitting Diodes
M. Moriyama, W. Saito, S. Yokohara, K. Tanaka and H. Umi, Tokyo Univ. of Agri. and Tech (Japan)
A patterned emissive layer (ELM) of organic light-emitting diode was prepared by evaporating carbazole acrylate monomer and photoinitiator followed by UV exposure and rinsing in a solvent. It was found that the patterning process polymerizes the ELM and stabilizes the device characteristics and can be repeated to prepare multiple patterns.

10:15 A-3-6

Direct Probing of Carrier Behavior in Electro-luminescence ZTO/InP-NDP/AlGaN/AlOx/Al Diode by Time-Resolved Optical Second-Harmonic Generation
D. Tsuchida, L. Zhang, J. Li, T. Matsuka and M. Iwashita, Tokyo Tech (Japan)
By using electric-field-induced optical second-harmonic generation and transient electro-luminescence (EL) measurements, we directly probed carrier transient leading to EL in organic light-emitting diodes. The charging-discharging-time at multi-layer interface was responsible for EL response time.

Coffee Break (2F Forum)

Short Presentation (11:00-12:15)

- **Chairs:** E. Itoh (Shinshu Univ.) N. Nakai (Univ. of Toyama) S. Takeuchi (Fujitsu Semiconductor Ltd.)
- **Authors:**
  - **Short Presentation P-1:** Y. Hayami (Fujitsu Semiconductor Ltd.) S. Tsujikawa (Sony Corp.)
  - **Short Presentation P-3:** Y. Nishida (Renessas Electronics Corp.) F. Borel (ST Microelectronics)
  - **Short Presentation P-7:** J. Fujikata (NEC Corp.) M. Tokushima (AIST)
  - **Short Presentation P-9:** M. Moriwaki (Renessas Electronics Corp.) T. Ishihara (Fujitsu Semiconductor Ltd.)
  - **Short Presentation P-11:** Y. Uzuka (NAIST) K. Yamagishi (Sony Corp.) M. Ono (Tohoku Univ.)

12:15-13:15 Lunch
interface was responsible for EL response time.

We directly probed carrier operation luminescence IZO/α-NPD/Alq3/LiF/Al Diode by 10:15 A-3-6

It followed by UV exposure and rinsing in a solvent. It A-3: Organic Light Emitting Diodes

P-10 (11:00-12:15)

A patterned of emissive layer (EML) of organic

contacts further show 2.3 times enhanced electroluminescence. LEDs with laser annealed led to contact resistivity reduction, resulting in a optimal laser fluence, excimer laser irradiation technique. The luminous intensity of this novel technique. The UVLEDs with pattern DBR structure were fab-

10:30 D-3-7

G. H. Wang

Optical Output and Improved Luminescence by GaN based Light Emitting Diode with Enhanced Emission was also achieved at 374 nm wavelength. A five-fold enhancement in photoluminescence band-edge coupling operation with an ultraviolet

GaN based Light Emitting Diode with Enhanced Emission was also achieved at 374 nm wavelength. A five-fold enhancement in photoluminescence band-edge coupling operation with an ultraviolet

We demonstrated two-dimensional photonic crystal

Chiao Tung Univ. and H. C. Kuo

and S. C. Wang, Y. C. Yang, M. H. Lo, H. C. Kuo, and K. Washio

and 1,2

REFERENCES

We introduced an electrically pumped bi-directional

dynamic nuclear polarization with using a double

We studied theoretically hot carriers in optically pumped graphene which can be utilized at THz laser. We showed that the population inversion is possible with sufficiently strong pumping.

Thursday, September 23

G-3: Modeling, Variation and Reliability (Area 5)

H-3: Oxides and Nanowires (Area 8)

I-3: III-V Device Technologies (Area 6)

J-3: Graphene Photonics and Electronics (Area 13)

K-3: Compound Power Semiconductor Devices (Area 14)

L-3: Nano Structures and Devices (Area 11)

10:30 G-3-5

Prediction of Circuit Degradation with Transient BTI and HC Simulations

D. Hagishima, T. Ishikawa, K. Maruta, and K. Masuda, Toshiba Corp. (Japan)

We have developed the circuit simulation coupled with dynamic transistor degradations. Our simula-
tion predicts the circuit characteristics more precisely than the conventional methods by self-consistent calculations between circuit and reliability simulations.

10:00 H-3-5

Growth and Characterization of GaAs/P-Nanowires on GaAs/IIIb Substrate By Selective-Area Metal Organic Vapor Phase Epitaxy

S. Fujimura, T. Sato, S. Hara, T. Motokura, K. Hirume and T. Yuki, Hokkaido Univ. (Japan)

To form vertical one-dimensional heterostructure, we fabricated GaAs nanowires on GaAs/IIIb substrates by using selective-area MOVPE. By analyzing the growth conditions, we succeeded in forming nanowire array with good crystal quality.

10:15 I-3-5

Defect-free GaAs/AlGaAs Heterostructure Etching Process by Chlorine/Argon Mixed Gas Ne-

ural Beam

X. X. Wang, C. H. Huang, Y. Ohsu, M. Igarashi, A. Moriyama, and S. Samukawa

Toothuck Univ., `Hokkaido Univ. and `CREST-JST (Japan)

Using chlorine/argon mixed gas neutral beam, we developed a dry etching process for fabricating GaAs/AlGaAs heterostructure with characteristics of defect-free, etching selectivity of GaAs/AlGaAs close to 1, atomically smooth etched surface, and vertical etch profile.

10:15 J-3-5

Study of Hot Carriers in Optically Pumped Gra-

phone

A. Satou, Y. Otani, and Y. Yeh

Toshiba Univ. (Japan)

We studied theoretically hot carriers in optically pumped graphene which can be utilized at THz laser. We showed that the population inversion is possible with sufficiently strong pumping.

Coffee Break (2F Forum)

Short Presentation (11:00-12:15)

Short Presentation P-5 (11:00-12:15)

Chairs: S. Sugawa (Tohoku Univ.)

T. Koide (Hiroshima Univ.)

Short Presentation P-2 and P-4 (11:00-12:15)

Chairs: Y. Hayashi (Renesas Electronics Corp.)

N. Nakano (Keio Univ.)

A. Yamada (Tokyo Tech)

H. Hibino (NTT Basic Res. Labs.)

Short Presentation P-6 (11:00-12:15)

Chairs: T. Hashizume (Hokkaido Univ.)

S. Tanaka (Shibaura Inst. Tech.)

Short Presentation P-13 (11:00-12:15)

Chairs: J. Motohisa (Hokkaido Univ.)

S. Uno (Nagoya Univ.)

Short Presentation P-14 (11:00-12:15)

Chairs: K. Ohtani (JAIST)

K. Nishioaka (Univ. of Miyazaki)

Short Presentation P-11 (11:00-12:15)

Chairs: Y. Taguchi (Keio University)

I. Yamashita (JAIST)

12:15-13:15 Lunch

- 25 -
In this study, we changed the dry etching conditions. The dry etching process for patterning P(VDF-TrFE) between the film properties and the intensity of an electric field becomes crucial for nano-scale devices. We have carried out the annealing process at a temperature higher than melting point with an electric field. To improve properties of P(VDF-TrFE) thin film, we used molecular carbon ion implantation and laser annealing. This principle has been used to develop novel devices. 12% improvement in both read and write operations was observed from this structure. We propose and demonstrate an application of ultra-thin on-the-fly wavelength conversion technology. We selectively deflect an input light pulse from a photonic crystal waveguide by fine tuning that technique and a photonic crystal nanocavity.

Threshold voltage (Vth) fluctuation has become a key concern in semiconductor devices. Fine tuning the junction implantations and based on films of pentacene and a SiO2 gate insulator that are separated by push-pull organic insulator that are separated by push-pull organic branched polymer and metal nanoparticle composites. This paper proposes the design method and synthesis of POMs.

Carrier Transport in Electrical Bistable Device

Electronic properties of the graphene were studied using the quantum chemical structure Defined by Geometry and Electrostatic Potential. The Kansai Electric Power Co., Ltd., H. Tsuchida and C. Aoki, Univ. of California, Riverside (USA) have investigated the number of electrons in Si DQD structure. 3D numerical simulation is used to determine the conductance band offset of the crystallized SiDQD.
In this study, we changed the dry etching conditions.

We have carried out the annealing process at a temperature. This reduction is mainly due to the increase in drain current and the decrease of ion collision to the substrate.

In this talk, we will review the results of our experimental and theoretical investigation of thermal conduction in graphene and few-layer graphene. Graphene applications in interconnects, thermal management and 3D electronics will be discussed.

In this paper, we proposed a distributed amplifier in 90-nm CMOS technology, using the gate-drain transformer coupling and pattern ground folded layout method to achieve high gain-bandwidth of 137.2 GHz and minimized chip size of 0.97x0.42 mm2.

Recently, a brain machine interface (BMI) / brain computer interface (BCI) has been researched in order to restore communication function for the severely disabled people due to amyotrophic lateral sclerosis, spinal injury, brain stroke etc. Especially, Electroencephalograms (EEG) is attracting attention as a key signal to realize these systems.

We developed a low-power current reference circuit with little temperature dependence for micro-power LSIs in a 0.35-μm standard CMOS process.

We achieve nanotube growth densities of 2E12 to 2E13 cm−2 by particular catalytic pre-treatments, for use in Vias and interconnects, the highest achieved to date.

We review electron spin qubits in silicon based on threshold-operated CMOS Digital LSIs and computer interface (BCI) has been researched in order to restore communication function for the severely disabled people due to amyotrophic lateral sclerosis, spinal injury, brain stroke etc. Especially, Electroencephalograms (EEG) is attracting attention as a key signal to realize these systems.

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Surface Manipulation of Precursor Carbazole Dendron Polymer Thin Films by Conducting-AFM Nanolithography

In this study, conducting-AFM nanolithography was used to manipulate the surface morphology of carbazole precursor dendron polymer thin films. Bias voltages were locally applied to the sample by using conducting-AFM. We have successfully obtained the locally controlled conjugated polymer due to the polymerization (Cross-linking) and the doping of the polycarbazole.

Coffee Break (2F Forum)
A hybrid sensor of QCM and SPR methods was developed. In this paper, we have reported the high performance of an a-IGZO thin-film transistor with a high-k dielectric layer on a glass substrate.

In this study, we have developed a fully quantum Monte Carlo simulator based on the Wigner transformation. Fully Quantum Study of Silicon Devices with emerging technology.

The polarization analyzing sensor is expected to be a solution for analyses of optically active compounds. We designed a polarization analyzing image sensor using 65nm CMOS process. By this sensor, polarization characteristics are successfully measured.

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The interaction between graphene and SiO₂ surface is necessary to preclude electron trapping at deep traps in a-IGZO device measurement data on short-term change. It is shown that ION as well as SS can be enhanced by controlling the doping concentration and geometry.

We investigated the degradation of a-IGZO TFTs under dynamic stress. Excellent properties were obtained. The effects of plasma condition on film properties were also investigated.

In this study, we fabricated ZnO thin-films using plasma-assisted ALD to improve the performance. Excellent properties were obtained. The effects of plasma condition on film properties were also investigated.

The degradation of a-IGZO TFTs was caused by the AC stress. We found that the AC voltage change under the AC stress and this degradation was caused by the Negatively-Charged Donor traps.

Impact of Surface Treatment of SOI/Si Substrate on Mechanically Exfoliated Graphene. The interaction between graphene and SiO₂ surface is critical to improve the mobility as well as the size of graphene. We study the effect of O₂ plasma treatment for SiO₂ surface on the interaction.

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Glass encapsulation was observed. Damage, identical durability that compared to the MoO$_3$ as passivation layer for reducing plasma damage, was studied. We have studied OLEDs with double-layered polymer dielectrics. The transistors have a switchable channel current and long retention time.

### Nonvolatile memory thin film transistors using double-layered dielectric layers and in the -OH groups inside the PDA to obtain that phase were investigated. GIDL current is drastically reduced and the memory effect originates from the charges stored in the interfaces between the polymer dielectrics. The transistors have a switchable channel current and long retention time.

Thursday, September 23

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<tr>
<td>A. Toriumi, Univ. of Tokyo (Japan)</td>
<td>Y. Nakajima, K. Kita, Y. Nishihara, K. Nagashio and A. Toriumi, Univ. of Tokyo (Japan)</td>
<td>H. Nakagawa, H. Okada and S. Naka, Univ. and Res. Inst. of Toyo University (Japan)</td>
<td>S. Ito, K. Tanii, T. Takahama and A. Toriumi, Univ. of Tokyo (Japan)</td>
<td>T. Numata, Toshiba Corp. (Japan)</td>
<td>A. Toriumi, Univ. of Tokyo, M. Nihei (AIST)</td>
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**Session B (Basement Floor)**

**“Silicon Solar Cells -Their key technologies and future prospects-”**

Organizer: T. Fukui, (Hokkaido Univ.)

Moderator: A. Yamada (Tokyo Tech), A. Masuda (AIST)

**Rump Session (Sanjo Conference Hall)**

**Rump Sessions (18:30-20:00)**

**Session A (1st Floor)**

“Will Carbon Create A New ICT Paradigm Beyond The Si Establishments?”
Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of Tokyo), M. Nihei (AIST)

**Session B (Basement Floor)**

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<tr>
<td><strong>17:50 G-5-4</strong> Amperometric Electrochemical Sensor Array for One-Chip Simultaneous Imaging: Circuit and Microelectrode Design Considerations J. Hasegawa, N. Uno and K. Nakazato, Nagoya Univ. (Japan) We introduce amperometric sensor circuit array for rapid and simultaneous electrochemical imaging, and also propose a novel microelectrode structure to reduce the time to reach the steady-state current, which is verified by computer simulation.</td>
<td><strong>17:35 I-5-4</strong> Novel Passivation Layer for Improvement of Reliability In Amorphous Indium Gallium Zinc Oxide Thin Film Transistor (TFTs) S. H. Choi, Y. W. Lee, J. Y. Kwon and M. K. Han, Seoul National Univ. (Korea) We have proposed and fabricated the a-IGZO TFTs with novel passivation layer consisting of sub-layers with different substrate temperatures. And we have verified that the proposed device could improve bias-illumination stability and enhance the electrical characteristics of a-IGZO TFTs.</td>
<td><strong>17:35 J-5-4</strong> Graphene based transversal-gated field effect transistor due to band gap modulation S. B. Kamar, T. Fujita and G. Liang, National Univ. of Singapore (Singapore) We explore a transversal-gated FET in which an asymmetric electrochemical potential is applied. This potential causes a reduction in the band gap of the AGNR, thus resulting in larger current flow across the device. The device performance is improved by introducing vacancies at the top edge.</td>
<td><strong>17:50 K-5-4</strong> Numerical Analysis of a Solar Cell with a Tensile-Strained Ge as a Novel Narrow Band Gap Absorber Y. Hashiba, M. Shinoda, A. Yamada and M. Komegi, Tokyo Tech (Japan) The solar cell performances of the InGaAs tensile-strained Ge: InGaAs double-hetero structure are numerically demonstrated as a thin, low-cost, and lattice-adjutable narrow band gap absorber in future multijunction solar cells.</td>
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**Rump Session (Sanjo Conference Hall)**

**Rump Sessions (18:30-20:00)**

**Session A (1st Floor)**

“Will Carbon Create A New ICT Paradigm Beyond The Si Establishments?”
Organizer: Y. Mochizuki (NEC)
Moderator: A. Toriumi (Univ. of Tokyo), M. Nihei (AIST)

**Session B (Basement Floor)**

“Silicon Solar Cells - Their key technologies and future prospects”
Organizer: T. Fukui, (Hokkaido Univ.)
Moderator: A. Yamada (Tokyo Tech), A. Masuda (AIST)