9:30 A-6-1 (Invited) 
Inkjet Printing of Organic Thin-Film Transistors 
T. Kayasawa, S. Morita, K. Nakamura, K. Inoue, K. Nakamura and T. Aoki, Seiko Epson Corp. (Japan)

The application of inkjet printing to the fabrication of organic TFT backplanes are reviewed. A hybrid approach in which inkjet printing is combined with photolithography is explained in detail. The phenomena happening in the inkjet printing of semiconductor are also discussed.

9:30 A-6-2 (Invited) 
Organic CMOS Logic Papers with In-Field User Customizability 

We report the manufacturing of user-customized logic paper—in which organic complementary logic is embedded. The logic paper provides on-demand in-field customizability to the users by making use of commercially available inkjet printing.

9:45 A-6-3 
Effects of an Interface Dipole Monolayer on Pentacene Organic Field-Effect Transistors 
W. Teo, B. Lee, W. Martin, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)

Effect of an aligned dipole monolayer with opposite color orientation on pentacene OFET performance was investigated. We found the monolayer greatly shifted threshold voltage, mobility and on/off ratio and they are controllable depending on the molecular orientation.

10:00 A-6-4 
Organic Transistors and circuits with parylene gate dielectric manufactured using submicrometer inkjet 
T. Yokota, Y. Noguchi, Y. Kata, T. Sekitani and Y. Someya, Tokyo Tech, Sony (Japan)

We fabricated organic TFTs and thin-film ring oscillator circuits by submicrometer inkjet printing. The TFTs have a channel length smaller than 500 μm, and the 3 μm linewith Ag source/drain electrodes.

10:10 B-6-4 
Accurate Measurement of Silkicada Specific Contact Resistivity by Cross Bridge Kelvin Resistor for 28 nm CMOS technology and Beyond 
K. Kurihara, Y. Doi, K. Nakamura, T. Ohno and K. Someya, Tokyo Tech, Nvidia (Japan)

It is confirmed that specific-contact-resistivity measurement resolution by using modified cross bridge Kelvin resistor is extended to 10⁻¹⁰ Ω cm², and experimentally found that 28nm-CMOS technology realizes 1x10⁻¹⁰ and 7.8x10⁻¹³ Ω cm² for n+ and p+ source/drain, respectively.

10:20 B-6-4 
Extreme-Thick SOI for Mainstream CMOS Challenges and Opportunities 

Source and drain formation techniques which are required in next generation Si devices such as memory SSLs and system SSLs are reviewed and the new challenge for the future are discussed in this paper.

9:30 C-6-1 (Invited) 
Overview and Challenges in Source/Drain Formation Technology in High Performance Power Transistors 
K. Sugaya, Toshiba Corp. (Japan)

Source and drain formation techniques which are required in next generation Si devices such as memory SSLs and system SSLs are reviewed and the new challenge for the future are discussed in this paper.

9:30 C-6-2 
Variability in Variable-Body-Factor Silicon-on-Insulator CMOS Technology 
Y. Yang, G. Du, R. Han and X. Liu, Peking Uni. (China)

A side-gate is used in the variable-body-factor silicon-on-insulator (SOI) CMOS technology to adjust the body-factor, which will, how-ever, introduce new variability to the SOI CMOS device. In this work, we systematically investigated the influences of LER (line-edge roughness), WVR (work function mismatch) and STV (silicon layer thickness variation) on 20-nm-gate variable-body-factor SOI MOSFETs.

10:00 C-6-2 
Towards Optical Networks-on-Chip Using CMOS Complementary Metal-Oxide-Semiconductor Technology 

The optical networks-on-chip (ONOC) concept consists of optical components on a network-on-chip, including III-V microbulk lasers, photodetectors, and wave-feeding structures, each of which are demonstrated in a demonstrator using a complementary metal-oxide-semiconductor (CMOS) compatible III-V-laser-on-chip integration technology at 200nm wafer scale.

9:30 D-6-2 
Universal Relationship between Settling Time of Floating-Body SOI MOSFETs and the Substrate Induced Stress on their Body-Tied Conductive Channel 
A. Takai, K. Ohtsuka, N. Hijibehzad, D. Hori, M. Miyake, S. Amano, M. Muraoka and M. Muraoka, Hitachi, Ltd. (Japan)

A device-size-independent universal relationship between the substrate induced stress and the body-tied conductive channel of floating-body SOI MOSFETs and the substrate current in their body-tied channel can play an important role in compact modeling of history effects.

10:00 D-6-4 
Monitoring One-bit Counter Circuit with Light Emitting Diode Indicators Fabricated in SiH7N7S Nanoheterostucture 
S. Tanaka, K. Natori, T. Nishio, M. Kajoh, Y. Hayashi, Y. Yamada, H. Okada, A. Wakahara, H. Yoda and T. Ueda, Tokyo Tech (Japan)

We fabricated a modulated stacked QD structure with various Sb beam equivalent pressure. Long-range energy transfer can be confirmed using micro-LED arrays with pulse width modulation (PWM) driver by flip-chip bonding method for nanoscale hetero-optical optoelectronic integrated circuit.

10:10 E-6-1 (Invited) 
Synthesis of pure phase BiFeO3 films grown on Iridium electrode by MOCVD for ferroelectric integrated circuit 
Y. Kanno, H. Kuroda, T. Bando, Y. Hirotsu, M. Hasegawa and D. Kimura, Tohoku Univ. (Japan)

We have successfully demonstrated the feasible synthesis of the pure phase BiFeO3 films without voids grown on the sputtered-niobium electrode by MOCVD using double-layered deposition method for the first time.

10:20 E-6-4 (Late News) 
Highly spin-polarized tunneling in Heusler-alloy-based magnetic tunnel junction with a CoMnBi upper electrode and a MgO barrier 
H. Liu, T. Taira, Y. Honda, K. Matsumoto and T. Uemura, and M. Yamamoto, Hokkaido Univ. (Japan)

High tunnel magnetoresistance ratio of 10% for 4.2 K and 335% at room temperature were demonstrated for Heusler-alloy-based magnetic tunnel junctions with a CoMnBi upper electrode and a MgO barrier. The key factors influencing the spin-dependent tunneling characteristics are discussed.
9:00 G-6-1 (Invited) CMOS High-Speed Image Sensors —Pixel Devices, Circuits, and Architectures—
S. Kanazawa, Shinshu Univ. (Japan)
CMOS high-speed image sensors are reviewed from the viewpoints of pixel devices and circuit techniques. Possible column-parallel ADC architectures for power-efficient high-speed high-quality imaging and global shutter pixels for low noise are discussed.

9:30 G-6-2 A Column Parallel Cyclic ADC with an Embedded Programmable Gain Amplifier for CMOS Image Sensors
T. Iida, M. A.USTAF, Z. Zou, H. Ohyama, S. Itoh and S. Kanazawa, Shinshu Univ. (Japan)
This paper proposes a column parallel cyclic ADC with an embedded programmable gain amplifier. The measurement results of a prototype chip show the effectiveness of the embedded PGA for the reduction of ADC non-linearity and random noise.

9:50 G-6-3 A CMOS Image Sensor with an Automatic Pixel-Sensitivity Adjustment Function
G. Baram, "Hiroyuki" and T. Arna, "Kyushu Inst. of Tech. and Tokuyama Inst., Sci. and Tech. Foundation (Japan)
We developed an image sensor LSI that automatically adjusts the exposure time for each pixel according to the brightness of its surrounding pixels. The developed sensor LSI uses a 65 nm CMOS 1-poly 3-metal process and has a die size of 3.75mm x 3.75mm. The power consumption is 267μW.

10:10 G-6-4 A Subnanowatt Vibrating-sensing Circuit for Dust-Sensitive Laser-Node Sensors
T. Shimamura, H. Morimura, M. Uygun and S. Matsu, NTT Microsystem Integration Laboratories (Japan)
The sensing circuit should be ultra-small power on the dust-size sensor node. We propose a vibrating-sensing circuit based on mechanical charge transfer. The test chip detects the vibration of sub-hertz-sized dust with sub-nanowatt power.

10:30 H-6-1 Invited
Alloys and Noble Metal Linear Materials to Extend Damascene Cu Schemes
T. Nogami, IBM (USA)
CVD-Cu films characterized (barrier properties and O2 incorporation). PVD-Ta/CVD-Cu/PVD-Cu applied to Cu/ULK REOL to produce reduced post-CMP defectivity and improved EM. However, EM advantage lost when divots due to corrosion formed at trench entrance.

10:30 H-6-2 Migration of Copper through Tungsten-Filled Via on Single Damascene Copper Interconnects
B. Kim, J. Kim, B. M. Seo, J. S. Oh, J. Y. Choi, K. Kang, H. J. Choi, and S. Park, Hynix Semiconductor Inc. (Korea)
A phenomenon of copper migration through tungsten-filled vias, which is single damascene copper underlayers, was examined. Successful mitigation of this problem was demonstrated through the enhancement of barrier metal or the change of soaking gas from silane to diborane in CVD W deposition process.

10:30 H-6-3 Thermally Stable Isolation of AlGaN/GaN Transistors by Using Fe Ion Implantation
H. Umeda, T. Takizawa, Y. Anda, U. Teda and T. Tanaka, Panasonic Corp. (Japan)
Thermally stable isolation for AlGaN/GaN transisators by Fe ion-implantation is demonstrated. The Fe ions form deep levels after high temperature annealing. This technique enables high breakdown voltages and promising for monolithic integration of GaN devices.

10:40 J-6-1 Invited
Thermal Stability of Isolation of AlGaN/GaN Transistors by Using Fe Ion Implantation
H. Umeda, T. Takizawa, Y. Anda, U. Teda and T. Tanaka, Panasonic Corp. (Japan)
Thermally stable Isolation for AlGaN/GaN transistors by Fe ion-implantation is demonstrated. The Fe ions form deep levels after high temperature annealing. This technique enables high breakdown voltages and promising for monolithic integration of GaN devices.

9:00 F-6-1 (Invited)
Circuit Implementation of InAs Nanowire FETs
W. Pfei, K. Blechler, O. Bener and F. J. Tegude, University of Duisburg-Essen (Germany)
We report on the fabrication of InAs nanowire metal-oxide-semiconductor field-effect transistor and their implementation in basic circuits. The position controlled deposition of the InAs nanowires within the pre-patterned circuits on the host substrate is done by field-assisted fluid self-assembly method.

9:45 K-6-3 Enhanced Photoluminescence Properties of Self-Assembled InAs Surface Quantum Dots by Antimony Incorporation
We present a study of surfactant effect from self-assembled InAs surface quantum dots grown on GaAs substrate by incorporating antimony (Sb) into the QD layers with various Sb beam equivalent pressure.

10:00 C-6-1 (Invited)
Overview and Challenges in Source/Drain For-

9:00 J-6-2 Transport Physics of Quasi-Ballistic Nanowire MOSFETs
K. Natori, Tokyo Tech (Japan)
Transport physics of nanoscale MOSFETs is discussed based on characteristics of nanowire MOSFETs. The compact model discloses various new effects.

9:00 J-6-4 Impacts of Diameter-Dependent Annealing in Silicon Nanowire MOSFETs
B. Wang, T. Tu, W. Ding and R. Huang, Peking Unive. (China)
The diameter-dependent annealing effect in silicon nanowire MOSFETs is investigated. The implanted dopants diffuse faster in thin nanowires than those in thick nanowires during annealing process, which results inunderestimating the nanowide 3D extension length.

9:45 K-6-2 Energy transfer in multi-stacked InAs quantum dots
We fabricated a modulated stacked QD structure from different types of InAs quantum dots. Energy transfer from small QDs to large QDs was clearly observed. Long-range energy transfer can be considered from the measurement of PL intensity.

10:00 K-6-4 Structures changes caused by quantum of InAs/ GaAs(001) quantum dots
M. Takahara, IAEI (Japan)
Structures of InAs/GaAs(001) free-standing quantum dots before and after quantized were studied by in situ synchronon X-ray diffraction. It has been revealed that quantum results in significant structure changes. They take place quickly when the substrate goes through a temperature range in which dislocation islands are preferably formed.
Friday, September 24

10:15 A-6-5 Effects of Gold Nanoparticles on Pentacene Organic Field-effect Transistors
K. Lee, W. Oh, Y. Jung, J. Moon, T. Yokoyama, Tokyo Tech and Shioval Academy of Sciences (Japan)
By incorporating gold nanoparticles into PVA with different concentrations as nanocomposite gate insulator in pentacene OETF, the carrier behaviour of the device was studied by considering the carrier injection and transport processes in terms of contact resistance and effective mobility.

11:30 A-4-6 Fabrication of Au electrodes with photopolymerization of trisacryl difluor thin films
Y. Sato, R. Ye, K. Ohita and M. Baba, Inate Univ (Japan)
we fabricated electrodes of thin films on micropatterned poly(DT) thin films photopolymerized through microcontact printing process is easier and environment friendlier than the past process. Furthermore, we investigated OTFTs with the Au/poly(DT) electrodes.

11:30 A-4-6 Fabrication of Au electrodes with photopolymerization of trisacryl difluor thin films
Y. Sato, R. Ye, K. Ohita and M. Baba, Inate Univ (Japan)
we fabricated electrodes of thin films on micropatterned poly(DT) thin films photopolymerized through microcontact printing process is easier and environment friendlier than the past process. Furthermore, we investigated OTFTs with the Au/poly(DT) electrodes.

11:30 A-4-6 Fabrication of Au electrodes with photopolymerization of trisacryl difluor thin films
Y. Sato, R. Ye, K. Ohita and M. Baba, Inate Univ (Japan)
we fabricated electrodes of thin films on micropatterned poly(DT) thin films photopolymerized through microcontact printing process is easier and environment friendlier than the past process. Furthermore, we investigated OTFTs with the Au/poly(DT) electrodes.

11:30 A-4-6 Fabrication of Au electrodes with photopolymerization of trisacryl difluor thin films
Y. Sato, R. Ye, K. Ohita and M. Baba, Inate Univ (Japan)
we fabricated electrodes of thin films on micropatterned poly(DT) thin films photopolymerized through microcontact printing process is easier and environment friendlier than the past process. Furthermore, we investigated OTFTs with the Au/poly(DT) electrodes.
Coffee Break (2F Forum)

G-7: Data Converter Circuits (Area 5)
(11:15-12:30)
Chairs: T. Kohda (Hiroshima Univ.)

H-7: 3D Interconnect (Area 2)
(11:15-12:25)
Chairs: J. Gambino (IBM) J. Kodato (NTT)

I-7: Processing and Interface Technologies (Area 6)
(11:15-12:50)
Chairs: K. Seo (Seoul National Univ.)
K. Kamakura (NTT Corp.)

J-7: Nanowire Growth and Applications (Area 13)
(11:15-12:30)
Chairs: N. Aoki (Chiba Univ.)
K. Tateno (NTT Corp.)

K-7: Growth and Characterization of Nitrides (Area 8)
(11:15-12:30)
Chairs: T. Isu (Fujitsu Labs. Ltd.)
M. Takahashi (JAERI)

10:30 G-6-5
A SPICE-based Multi-physics Seamless Simulation Platform for CMOS-HEMS
We report a SPICE version of such multi-physics solver that is capable of microelectromechanical transient analysis, AC harmonic analysis, and electro-mechanical mixed-signal simulation that can be performed seamlessly with the LSI simulation.

11:30 G-7-2
A 0.35 V 14mW 75MHz 10b CMOS Current Steering DAC
N. Shimosaki, R. Ito, M. Miyahara and A. Matsumara, Tokyo Tech (Japan)
An ultra-low voltage and power of 0.35 V and 1.4 mW, yet high speed of 750 MHz 10 bit current DAC has been developed using digital feedback technique and forward body biasing.

11:35 G-7-7
Evaluation of Copper Diffusion in Thinned Wafer with Extrinsic Gettering for 3D-LSI by Capacitance-Time(C-T) measurement*
J. C. Box, K. W. Lee, M. Murgongram, T. Fukazawa, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
The effects of extrinsic gettering(ICG) layers formed on p-wafers and p-wafers by backside grinding and the following chemical mechanical polishing(CMP), dry polishing(DP) and ultraplanarization(UP) on the contamination induced has been investigated.

10:15 I-6-5
Reduced contact resistance and Improved surface morphology for Organic Contacts on GaN/GaN based Semiconductors employing iKRF Laser Irradiation
We employ excimer laser annealing for ohmic contact formation to n-type GaN. Laser annealing achieved reduced sheet resistance in contact formed, essential for high performance GaN light emitting diodes (LEDs) and heterostructure field-effect transistors activations. Forward current in LEDs increased due to the reduced contact resistance.

11:30 I-7-2
Direct Liquid Cooling Technology for Power Semiconductors
J. C. Box, K. W. Lee, M. Murgongram, T. Fukazawa, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We first demonstrate the reduction of temperature in transient liquid direct cooling (DLC) of GaN power devices for high power and high voltage switching applications. In the DLC structure, junction temperature reductions of up to 50% and 100% higher power levels were demonstrated, and the thermal resistance was reduced by as much as 32%.

Nonequilibrium Carrier Transport Observed in Pnp AlGaN/GaN HBTs
K. Kamakura and T. Makimoto, NTT Corp. (Japan)
We found nonequilibrium carrier transports in the nitride-based HBTs. They were ascribed to the high energy carrier injection into the base, and also to the carrier distribution induced by the electric field inside the base.

Nonequilibrium Carrier Transport Observed in PnpAlGaN/GaN HBTs
K. Kamakura and T. Makimoto, NTT Corp. (Japan)
We found nonequilibrium carrier transports in the nitride-based HBTs. They were ascribed to the high energy carrier injection into the base, and also to the carrier distribution induced by the electric field inside the base.

A Theoretical Study of Electron Wave Function Penetration Effects on Electron-Mediated Acoustic-Phonon Interactions in Silicen Nanowire MOSFETs
J. Hatto, S. Uno, N. Moro, K. Sakatsume, Nagaoka Univ., Osaka Univ. and CREST-JST (Japan)
We have theoretically studied the interaction between electrons and modulated acoustic phonons in gate biased silicon nanowires with taking into account electron wave function penetration into the oxide layer.

Single-electron transport through a Germanium Nanowire Quantum Dot
S. K. Shin*, S. Hwang*, N. Fukushima, T. Takahata, S. Takagi, Y. Shigemori, Y. Nakano and M. Sugiyama, Univ. of Tokyo (Japan)
We investigated the annealing effect on InAs growth, annealed in group-V gas ambient at much higher temperature than that during growth and the protection effect of group-V atoms during annealing in terms of surface contamination.

10:30 J-7-3
Volumetric Growth of InAs Nanowire Quantum Dots on a Wafer Utilizing Concentric Distribution
Using concentric distribution of QD density on a wafer, we obtain a series of QDs with charged excitonic states from positive to negative via neutral states at a time. As a result, we succeed in growth of InAs QDs with selectively charged states on a same wafer by only Si doping.

11:45 K-7-2
Reduction of S-parameter by the Introduction of Nitrogen in GaN: A Perspective for Realization and Its Comparative Study with Photoluminescence Spectroscopy
N. Igarashi, F. Ishikawa, M. Kondow, T. Ohshima, A. Yabuchi, M. Nomura, Y. Ohji, S. Yamaura, M. Yamamoto and T. Arakawa, Univ. of Tokyo and NECT Corp. (Japan)
The hydrothermally grown Al-doped ZnO nanowires were controlled by high-voltage poly-Si thin film transistor to improve the anode current stability of field emitter.

10:15 K-6-5
High-temperature phosphorous passivation of Si surface for improved heterolateral growth of InAs as an initial step of III-As MOVPE on Si
M. Otsuka, N. Okahara, H. Masuda, K. Noda, N. Watanabe, T. Fukushima, S. Takagi, Y. Shigemori, Y. Nakano and M. Sugiyama, Univ. of Tokyo (Japan)
We investigated the annealing effect on InAs growth, annealed in group-V gas ambient at much higher temperature than that during growth and the protection effect of group-V atoms during annealing in terms of surface contamination.

10:30 K-6-6
Growth of InAs Quantum Dots with Various Charged States on a Wafer Utilizing Concentric Distribution
Using concentric distribution of QD density on a wafer, we obtain a series of QDs with charged exci-}

Friday, September 24

4F 222
2F 223
We have performed both experimental and theoretical studies of transport mechanism in first layer grain sizes and grain boundaries of the pentacene films and found that the grain boundary model is valid both in grain size dependent and temperature dependent mobility experiments.

12:15 C-7-4
FinFET: Junctions Optimization by Conventional Ion Implantation for Sub-32nm Technology Nodes Circuit Applications
A. Veloso, A. De Keersgieter, S. Brus, N. Horagiuchi, P. P. Abk and T. Hoffmann,IMEC (Belgium)
This work demonstrates the junctions formation methodology for aggressively scaled FinFET devices, using conventional ion implantation, and compatible with dense pitch devices, without penalty in RSD nor device performance, and yielding higher SRAM SNM values.

11:45 D-7-3
Enhanced Sensitivity of SOI Photodiode by Au Nanoparticles
Y. Matsuo, A. Ono, H. Sato and H. Inokawa, Shizuoka Univ. (Japan)
We demonstrated the enhancement of the quantum efficiency of SOI photodiode by Au nanoparticles. The enhancement mechanism is explained by the increment of the effective path in SOI due to the scattering and the multiple reflections.

11:55 C-7-3
Advantage of Plasma Doping for Source/Drain Extension in Bulk FinFET
T. Izumida, K. Okino, T. Kamemura, M. Kondo, S. Inaba, S. Ishi, N. Aoki and Y. Iyoshima, Toshiba Corp. (Japan)
We demonstrate the efficiency of plasma doping on the fabrication of bulk FinFET, showing detailed boron distributions in a narrow fin region analyzed by atom-probe tomography and SIMS, and device characteristics calculated by 3D simulations.

Bias-temperature-instability and thermal anneal penalty in RSD nor device performance, and yield high SRAM SNM values.

12:00 A-7-4
Transport Mechanism at the First-layered Pentacene Grains and Grain Boundaries
Y. Hu, L. Wang, Q. Qi and C. Jiang, National Center for Nanoscience and Tech. and Chinese Academy of Sci. (China)
We have performed both experimental and theoretical researches of transport mechanism in first layer grain sizes and grain boundaries of the pentacene films and found that the grain boundary model is valid both in grain size dependent and temperature dependent mobility experiments.

13:30 C-8-1
Using Power Transform to Study DC and AC CHC Effects on mOSFETs in 65nm Technology
S. Y. Chou, C. H. Tu, M. X. Wu, H. S. Huang, Z. W. Bao, S. Chen and J. Ko, National Taiwan Univ. of Tech. and United Microelectronics Corp. (Taiwan)
For the first time, this article is to use power transform to describe mOSFET degradation due to DC and AC CHC stress. The power transform model is a function of voltage (Vds, Vgs), current (Ids), and temperature (T). All the results show that the power transform model can well fit the experimental data of DC and AC CHC stress.
Friday, September 24

G-7: Data Converter Circuits (Area A5)

11:55 G-7-3
Low-Cost Fully Time-Domain Winner-Take-All Circuit with High-Time-Difference Resolution Limited only by With-In-Die Variation
The time-domain Winner-Take-All (WTA) circuit detects the first arriving signal and determines the winner. In this paper, a time-domain WTA circuit with high-time-difference resolution limited only by with-in-die variation is developed.

12:15 G-7-4 (Late News)
3.6-Times Higher Acceptable Bit Error Rate, 97% Lower-Power, VRAM & NAND-Integrated Solid-State Drives (SSDs) with Adaptive Codeword ECC
M. Fukuda, K. Hisagai, S. Tanakamara and K. Takesachi, Univ. of Tokyo (Japan)
An adaptive codeword ECC is proposed for VRAM/NAND integrated SSDs. The acceptable raw bit error rate before ECC of VRAM/NAND and NAND increases by 3.6-times. The 10Gbps high-speed write is achieved with 97% power reduction.

H-7: 3D Interconnect (Area 2)

12:05 H-7-3
Through Silicon Photonic Via with Si core for Law loss and High Density Vertical Optical Interconnection in 3D-LSI
A. Noreiki, K. W. Lee, J. Bae, T. Fukusaka, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
We proposed through-Si photonic via with Si core (TSPV) for low-loss and high-density vertical optical interconnection in 3D-LSI. We confirmed light confinement of the TSPV and showed feasibility of very fast TSPV by 2D-FDTD simulation.

H-7: 3D Interconnect (Area 2)

12:45 H-7-3
Impact of Interface States and Bulk Carrier Lifetime on Photocapacitance of Metal/Insulator/GaN Structures
P. Bidinosti, M. Mireić, B. Admecić, C. Mireić and T. Hashizume, Školskii Univ. of Tech and Hirokaido Univ. (Poland)
The capacitance of a metal insulator/GaN ultraviolet detector has been calculated versus the light extinction intensity and gate voltage. The influence of the interface states and bulk carrier lifetime on the photodetector characteristics has been discussed and the calculation results have been compared with experimental data.

13:00 H-7-4
Lateral GaN nanowires with triangular and trapezoidal cross-sections grown on (311)B and (001) substrates
G. Zhang, K. Tabeno, H. Gyotsubo and T. Segawa, NTT Corp. (Japan)
The cross-sectional shape of lateral nanowires can be varied by using substrates with different orientations. Lateral nanowires with triangular and trapezoidal cross-sections were grown on (311)B and (001) substrates.

13:15 H-7-5
New Stacked MIM Capacitors with a Side-contact Formation Technology
T. Inatomi, S. Segiyan, K. Nishimura and M. Isla, NTT Corp. (Japan)
We proposed new stacked MIM capacitors with electrical side-contacts, which enable to be fabricated with very few masks and a short turn-around time. We successfully fabricated five-layer stacked MIM capacitor and increase capacitance density from 3.6pF/um^2 to 1.51pF/um^2.

Friday, September 24

I-7: Processing and Interface Technologies (Area 6)

11:45 I-7-3
C-V Characteristics and Analysis of Undoped Planar MOS capacitor data
The capacitance of a metal/insulator/GaN ultraviolet detector has been calculated versus the light extinction intensity and gate voltage. The influence of the interface states and bulk carrier lifetime on the photodetector characteristics has been discussed and the calculation results have been compared with experimental data.

I-7: Nanowire Growth and Applications (Area 13)

11:45 J-7-3
Electrical Characterization of InGaAs nanowire MISFETs Fabricated by Dielectric-first Process
Y. Kobaishi, T. Sato, K. Tomozuka2,3, S. Haru, T. Fuku and K. Motoki,1,2,3,4 Hokkaido Univ. and 1ST PRESTO (Japan)
We attempted gate-dielectric-first process to fabricate MISFETs using single InGaAs nanowires formed by selective-area MOVPE. We obtained improved maximum drain current as compared to our previous nanowire FETs.

12:00 J-7-4
C-7-3
CHC Effects on nMOSFETs in 65 nm Technology
S. Y. Chen,1,2 S. Chou,1,2 S. Kim1,2 and J. K. Furdyna1,2,1 United Microelectronics Corp., 2 Samsung Univ. of Notre Dame (Korea)
Much recent progress in silicon nanophotonic technology has enabled the prospect of high-performance low-power integration at sub-22nm technology. In this paper, we proposed the high-chance-cut (CHC) technology for multi-valued memory device and the future outlook of the method will be discussed.

K-7: Growth and Characterization of Nitrides (Area 8)

12:00 K-7-3
Nucleus and Spiral Growth of GaN Studied by Selective-Area Metastable Vapor Phase Epitaxy
T. Akasaki, Y. Kobayashi and M. Kasa, NTT Corp. (Japan)
We have fabricated step-free GaN surfaces with a diameter up to 50 microns by selective-area metastable vapor phase epitaxy. We also discuss the mechanism of both nucleus and spiral growth of GaN in detail.

12:15 K-7-4
High-speed MRAM Random Number Generator
J. Shin, K. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)
The enhancement mechanism is explained by the parameters in the set delay and cell delay. We demonstrated the enhancement of the quantum effects in MRAM by using the high-speed MRAM Random Number Generator.

12:30-13:30 Lunch

G-8: Bio Nano-fusion Technologies (Area 11)

11:30-15:00
Chair: J. Ohnai (NAIST)

M. Nakanishi (Toyota Technological Inst.)

13:30 G-8-1 (Invited)
Novel Quantum Effect Devices realized by Fusion of Bio-template and Defect-Free Neutral Beam Etching
S. Sakumoto,1,2,3 Tohoku Univ. and 1ST (Japan)
A 2D Si ND array with a high-density and well-ordered arrangement could be fabricated by using bio-template and damage-free Si neutral beam etching. In this structure, the controllable band gap energy (from 2.2eV to 1.45eV) and high photonic absorption coefficient (>105 cm^-1) could be obtained at RT by controlling the Si-ND structure.

H-8: 3D Integration (Area 2)

13:30 H-8-1 (Invited)
Low temperature bonding for 3D integration
T. Sugai, Univ. of Tokyo (Japan)
The surface-activated bonding (SAB) is a highly potential method providing a low temperature interconnect process viable for 3D integration. The applications of SAB are demonstrated in Cu direct bonding, and hetero-semiconductor wafer bonding, and the future outlook of the method will be discussed.

13:30 H-8-1 (Invited)
Crystalline Silicon Solar Cells, Thinner the Better
T. Hashizume1,2,3,4 AIST and Univ. of Tsukuba (Japan)
Historical trajectory of research and development of the very ultra thin c-Si solar cell/module was reviewed. According to theoretical and experimental reports, more than 20% efficiency with about 10 micro-meter thick cell is one of future targets.

13:30 H-8-1 (Invited)
High-speed MRAM Random Number Generator
J. Shin, K. Koide and H. J. Mattausch, Hiroshima Univ. (Japan)
The enhancement mechanism is explained by the parameters in the set delay and cell delay. We demonstrated the enhancement of the quantum effects in MRAM by using the high-speed MRAM Random Number Generator.

K-8: Si and Ge-based Materials and Devices (Area 8)

13:30 K-8-1
Very high mobility 2D holes in strained Ge quantum well epilayers grown by Reduced Pressure Chemical Vapor Deposition
M. Myronov1,2,3 K. Serimura1,2 D. R. Leadlay1 and Y. Shiokazu1, Univ. of Warwick and 1Tohoku City Univ. (UK)
For the first time, we report a very high 2D-HG mobility obtained in compressive strained Ge quantum well epilayers grown on Si(001) virtual substrate by an industrial type RT-CVD technique.

13:30 K-8-1
Very high mobility 2D holes in strained Ge quantum well epilayers grown by Reduced Pressure Chemical Vapor Deposition
M. Myronov1,2,3 K. Serimura1,2 D. R. Leadlay1 and Y. Shiokazu1, Univ. of Warwick and 1Tohoku City Univ. (UK)
For the first time, we report a very high 2D-HG mobility obtained in compressive strained Ge quantum well epilayers grown on Si(001) virtual substrate by an industrial type RT-CVD technique.
We report on rectification properties of pentacene single crystals deposited onto NiO-metal gates. The electrical measurements were performed in a vacuum chamber with the gate voltage varying from 0 to -1.5 V. The rectification properties were studied at various frequencies ranging from 0.1 to 1 MHz. The rectification factor (R) was deduced from the ratio of the rectified current to the total current flowing through the device. The results showed that the rectification factor increases with decreasing reverse bias and increasing frequency. The measured rectification factor for a frequency of 1 MHz was found to be 120. This value is consistent with previous reports on rectification in organic thin-film transistors. The high rectification factor indicates the potential of pentacene single crystals as rectifying elements in low-frequency applications.

Rectification properties of pentacene single crystals deposited onto NiO-metal gates were investigated. The electrical measurements were performed in a vacuum chamber with the gate voltage ranging from 0 to -1.5 V. The rectification properties were studied at various frequencies from 0.1 to 1 MHz. The rectification factor (R) was calculated from the ratio of the rectified current to the total current flowing through the device. The results showed that the rectification factor increases with decreasing reverse bias and increasing frequency. The measured rectification factor for a frequency of 1 MHz was 120, consistent with previous reports. The high rectification factor indicates the potential of pentacene single crystals as rectifying elements in low-frequency applications.

We investigated the rectification properties of pentacene single crystals deposited onto NiO-metal gates. The electrical measurements were conducted in a vacuum chamber with the gate voltage ranging from 0 to -1.5 V. The rectification properties were studied at various frequencies from 0.1 to 1 MHz. The rectification factor (R) was deduced from the ratio of the rectified current to the total current flowing through the device. The results showed that the rectification factor increases with decreasing reverse bias and increasing frequency. The measured rectification factor for a frequency of 1 MHz was 120, which is consistent with previous reports. The high rectification factor indicates the potential of pentacene single crystals as rectifying elements in low-frequency applications.
We fabricated organic TFTs using DNTT as p-type. The paper reports totally different carrier behaviors - rectify an AC voltage at a frequency above 1 MHz. Megahertz Operation of Rectifier Circuits using deposited arrays of OTFTs on large areas.

We investigated the growth condition of NiSi₂ on Si substrates by using a versatile atomic force microscope. We observed large positive magnetoresistance in the heterostructure, which might be caused by the magnetization of NiSi₂. In the heterostructure, the magnetization is aligned parallel to the magnetic field during the growth of NiSi₂ on Si. We also observed large positive magnetoresistance in the heterostructure, which might be caused by the magnetization of NiSi₂. In the heterostructure, the magnetization is aligned parallel to the magnetic field during the growth of NiSi₂ on Si.

The top electrode (TE) material plays an important role in determining the device characteristics. We demonstrated highly productive microbump bonding method for the chip-to-wafer 3D integration. We aligned chips onto Si wafer using self-upperment method and established conductor lines of 50-μm-size microbumps.

High Density and Power Efficient SIP with 3C Technology. S. Hasegawa, Y. Motobu, H. Usami, T. Kaneko, K. Hara and T. Takahashi, Univ. of Tokyo (Japan). We demonstrated the fabrication of poly-Si TFTs on poly-carbonate substrate at temperatures below 135°C, i.e. well below the glass transition temperature of poly-carbonate. TFTs whose electronic mobility is over 0.6 cm²/Vs can be fabricated.
16:00 A-9-3
Direct observation of carrier behavior leading to electroeluminescence in tetracene field-effect transistor
T. Okahata, H. Satoh, T. Manaka, H. Kohin, N. Morako and M. Iwamoto, Tokyo Tech (Japan)
We probed the carrier behavior leading to electroeluminescence in tetracene field-effect transistor using optical and electrical characterization method. We observed high density of carriers and their transport behavior. We also observed electroeluminescence at low temperature.

16:10 B-9-3
TO- and LO-modes analyses in asymmetric stretching vibrations in ultra thin thermally grown GeO,
G. J. F. Amaratunga, P. R. P. Jayasuriya, A. J. J. Perera and H. H. H. Dias, University of Moratuwa, Sri Lanka
A high-resolution MOEMS device was fabricated on SOI substrate using 248 nm photolithography process. The device consists of a thin silicon membrane with a cavity and a pair of metal electrodes. The device was tested under various operating conditions such as temperature, humidity, and vibrations. The device exhibited high sensitivity and good linearity over a wide range of operating conditions.

16:55 A-9-4
Diffuser micropump structured with extremely thin diaphragm of 2 micro-thick polyimide film
Y. Lin, H. Komatsubuchi, D. Tan and Y. Nishioka, Nihon Univ. (Japan)
The simple structure air-actuated valveless micropump with the 2.1 micron-thick polyimide membrane was designed, fabricated and measured. The micropump was fabricated on the 60 micron-thick Si wafer using surface micromachining techniques.

17:00 A-9-5
Quantitative Analysis of Stress Relaxation in SiO2 film on Si wafer using Raman Spectroscopy
S. Inoue, M. O. Nishihara, T. Oheda and N. Ikuhara, Tohoku Univ. (Japan)
The study was conducted on SiO2 film on Si wafer using Raman spectroscopy. The objective was to investigate the stress relaxation behavior of SiO2 film on Si wafer. The analysis was performed using Raman spectroscopy to study the stress relaxation behavior of SiO2 film on Si wafer.

17:45 A-9-6
Design of Broadband Optical Switch Based on Mach-Zehnder Interferometer with Si wire waveguides
K. Kinta, T. Shoji, S. Suda, H. Kawanaka, T. Hasebe and M. Hikosaka, AIST (Japan)
Design and fabrication of a broadband optical switch based on Mach-Zehnder interchanger with Si wire waveguides. The device was fabricated using SOI technology and exhibited a bandwidth of 600 nm with a loss of less than 1 dB. The device was demonstrated to be suitable for optical interconnection applications.

18:00 A-9-7
High ON/Off resistant NiO ReRAM using Post-Plasma-Oxidation (PPO) process
A. Oka, M. Itoh, K. Ishihara and S. Yorimitsu, National Institute of Materials Science, Japan
A high ON/Off resistant NiO ReRAM device was fabricated using a post-plasma-oxidation process. The device exhibited a high ON/Off ratio of 10^5 with a low write/erase power consumption of 1 mW.

15:45 A-9-2
Interface and Strain Characterization (Area 3)

C-9: Emerging Device Technology (Area 3)

15:30 C-9-1 (Invited)
CVD Graphene for High Speed Electronics
B. C. Hwang, C. A. Qiao, M. Yong, H. Xie Xie and J. C. St. Rust, UCLA (US)
High-resolution measurements of the surface potential was demonstrated on oxidized Si surfaces by scanning multi-atomic tunneling spectroscopy at optimized tunneling gap. The potential maps agree with build-in potential for p-junctions, while nanometer-scale fluctuations were caused by structure and charge variations.

15:30 C-9-2
High Hole-Mobility 65nm Biaxially-Strained GeFETs: Fabrication, Analysis and Optimization
HAADF-STEM revealed that Pt segregates at lattice-matched areas of the interface and occupied even, Pt, someya, 1, someya, 2, someya, 3, someya, 4, one, two, three, four, K. Kita, Pantisano, 1,3, C. W. Lee, J. S. Roh and S. K. Park, Hynix Semiconductor Inc.
High hole-mobility 65nm biaxially-strained GeFETs, with reduced EOT while maintaining minimal SCE, have been fabricated and electrically characterized in-depth for the low and high field transport. We demonstrate a 30% enhancement in the field-effect mobility compared to pMOSFETs.

15:45 C-9-3
Evaluation of optical absorption and light propagation loss in Er3+ SiO2 nanowaveguides
K. Homma, T. Nakajima, T. Komiya and H. Ishikawa, Univ. of Electro-Communications (Japan)
We demonstrated that the Er3+ SiO2 nanowaveguides, which are used in optical absorption and light propagation loss in the Er3+ SiO2 nanowaveguides. The results show that the optical absorption is low in the Er3+ SiO2 nanowaveguides, and the light propagation loss is also low, which is beneficial for high-speed optical communication systems.

16:00 C-9-4
Design and Simulation of Silicon Ring Optical Interferometer (RIO) for L2 Cache SRAM
Y. H. Chung, S. S. Chang, S. J. Shi and S. K. M. Kang, Korea University, Seongnam
We investigated high-speed (sub-nano second) spin-transfer torque based on NiO magnetic device for high-capacity memory. The device is fabricated using a double-pulse current and shows high sensitivity to the magnetic field.

16:30 C-9-5
Mechanical stability of free-standing bilayer lipid membranes
K. Sawada, T. Kakuda, T. Ishii, S. Ito, N. Igarashi, M. Narihiro and T. Hase, Renesas Electronics Corp. (Japan)
Free-standing lipid bilayers are important for cell-membrane research and nanoscale technology. We investigated the mechanical stability of free-standing lipid bilayers using AFM force-distance measurements.

15:30 D-9-1
Real-time synchrotron radiation X-ray diffraction and abnormal temperature dependence of photoemission from silicium electrodes on few-layer graphene film deposited on Ni and Ni dots using CVD method. Under low temperature growth condition, the uniformity of graphene was remarkably improved. Top-gated graphene transistors are made by transferring the graphene film onto a SiO2 substrate. Ambipolar conduction is clearly observed from 20°C via curve.

15:30 D-9-2
Overview and Future Challenges of Hafnium Oxide ReRAM
hafnium oxide Hafnium Oxide ReRAM with high speed, low power operation, and excellent reliabilities including nonvolatility and endurance is demonstrated. A 3 kb array with robust cycling endurance can be achieved by effective verifications. Some challenges must be overcome to realize this memory as a promising nonvolatile memory.

16:00 E-9-2
New Tunneling Barrier Width Model of the Schmitt Trigger Switching Mechanism in Hafnium Oxide-Based Random Access Memory
We investigated high-speed (sub-nano second) spin-transfer torque based on NiO magnetic device for high-capacity memory. The device is fabricated using a double-pulse current and shows high sensitivity to the magnetic field.

16:15 F-9-3
Sodium Ion Detection by Fluorinated-Atomic Layer Deposition Films
Y. Lee, C. K. Chen and T. C. Tsai, National Taipei University
We fabricated Na+-sensitive films by fluorinated-atomic layer deposition (ALD) and demonstrated their sodium ion detection ability. The films were characterized for their selectivity and sensitivity to sodium ions.

15:00 A-9-1
Interface of Portamento Process of Self-Assembled Monolayer Gate Dielectric for 2-V Operation High-Mobility Organic TFT
We investigated the optimized parameters of oxygen plasma process of self-assembled monolayer gate dielectric for organic TFTs. Short exposure time of plasma process (200 W, 30 sec) produces good transistors with high mobility of 0.97 cm²/Vs and small hysteresis.
15:30 G-8-1
Free-Standing Lipid Bilayers Based on Nonpolar Alumina Films
Mechanical stability of free-standing bilayer lipid membranes (BLMs) was improved by suspending the BLMs in nonpolar alumina films. The membrane stability was investigated in terms of lifetime and breakdown voltage.

16:00 G-8-2
Fabrication of CMOS-compatible Pol-Si Nanowire FET Sensor
H. Chen1, C. Y. Liu1, M. C. Chen2, H. C. Chou1, C. C. Huang1, and H. H. Chou1, National Chiao Tung Univ. and National Nano Device Lab. (Taiwan)
A low-cost, superior performance Pol-Si nanowire FET sensor fabrication method features entire CMOS processing. A self-aligned nanowire fabrication in bulk-Si technology is also disclosed for the first time for highly integrated sensor system design.

16:15 G-8-4 (Late News)
Light-Addressable Potentiometric Sensors for Sodium Ion Detection by Fluorinated-Atomic Layer Deposition Hafnium Oxide Membrane
C. H. Chiou1, J. H. Yang2, T. F. Lu3, C. E. Lu1, C. M. Yang1 and C. S. Lai, Chang Gung Univ. and Inouera membranes Inc. (Taiwan)
In this study, an inorganic method was investigated for Na⁺ detection based on LAPS. The sensing membrane, HF02 layer, was deposited by ALD and treated by RTA and CF4 plasma. The pH sensitivity was decreased and pNa sensitivity was increased by CF4 plasma. Finally, the highest pNa sensitivity was 34.8 mV/pNa measured from pNa 1 to pNa 4.

15:30 H-9-1
Characterization of LTO coating on microfluids of CMOS image sensor
CMOS image sensors with an LTO coating on the microfluids have been characterized for dark current, quantum efficiency, and reliability.

15:30 I-9-1 (Invited)
Impact of Metal Contamination in Silicon Solar Cells
G. Coletti, ECS Solar Energy (the Netherlands)
Impact of transition metals on the conversion efficiency of silicon solar cells is presented. Fe, Cr and Ti reduce the internal quantum efficiency (IQE) at long wavelength reducing the carrier diffusion length. Ni reduces the IQE at short wavelength increasing recombination in the solar cell emitter region. Cu reduces the IQE at both short and long wavelengths. A physical model is presented explaining the data.

15:30 I-9-2
Optimization design of a-Si:H/μc-Si:H tandem thin film solar cells with a low-refractive-index AZO transparent conducting oxide
J. W. Leem and J. S. Yu, Kyung Hee Univ. (Korea)
Aluminum-doped zinc oxide (AZO) thin films with low-refractive-index (low-n) as a transparent conducting oxide (TCO) layer for Si solar cells are deposited on Si and glass substrates by magnetron sputtering using an oblique angle deposition method. To improve the efficiency, the a-Si:H/μc-Si:H tandem solar cells with a TCO layer of low-n AZO are designed using a Silvaco ATLAS simulation.

15:30 I-9-3 (Late News)
MEMS Resonance Test for Mechanical Characterization of Nano-Scale Thin Films
The purpose of this study is to develop a quantitative measurement method for the Young’s modulus of nanometer-thick films. We developed the test technique using a MEMS resonator array and measured the Young’s modulus of Al and plasma-polymerization films made from CH4 and CHF3 gases.

15:30 I-9-4 (Late News)
Three-terminal a-Si solar Cells
C. H. Tai, C. H. Lin, C. M. Hwang and C. C. Lin, National Dong Hwa Univ. (Taiwan)
A new back-to-back pin-tip structure increases the average electric field in a solar cell. The 0.28-μm-thick three-terminal a-Si solar cell achieved an efficiency of 11.4%.
Printed Electrode for All-Printed Diode and Transistors.

We have developed a mechanical sintering technique, printed electrode with various work functions from 3.5eV to 5eV could be prepared on a plastic substrate. These printed alloys were effective to improve the performance of printed diode and transistors.

Printed Electrode for All-Printed Polymer Diode Fabrication

We have developed a mechanical sintering technique for printed metal patterns. Using this technique, printed electrode with various work functions from 3.5eV to 5eV could be prepared on a plastic substrate. These printed alloys were effective to improve the performance of printed diode and transistors.

A Tunable Emission Prepared by Novel Photo-induced Color-Change Materials

An organic phosphor C-54ST was used as a green light dopant in this study. After protonation the above emitting layers could be easily switched. In conjunction with a blue-light pumping source, the above emitting layers could be easily switched.

Fabrication of Sol-Gel Alumina Dielectric for Low-Voltage Operating Pentacene Transistor

A sol-gel alumina dielectric for pentacene transistor has been introduced. With this alumina dielectric, the low voltage pentacene thin film transistor is fabricated and it is free from the threshold voltage shift problem.

Development of Accelerometer Using Mach-Zehnder Interferometer Type Optical Waveguide

A novel inertial force sensor which uses a Mach-Zehnder Interferometer (MZI) type optical waveguide made of crystal silicon is developed. In this sensor, one branched waveguide of the MZI have floating beam structure which is formed by removal of its underlying SiO2 layer.

Novel Low Power RRAM with a U-type Cell Structure for Improving Resistive Switching Characteristics

We propose a novel RRAM structure which makes it possible to reduce the reset current by controlling the number of the electrical path. Numerical simulation is also performed to investigate the optimal process condition.

Crosstalk improvement in Si-wire optical cross-bar switch

Achieved low-crosstalk is -50 dB for the bar state and is -30 dB for the cross state. We discuss on the limiting factors.
K. K. Han
Low-Voltage Operating Pentacene Transistor
Fabrication of Sol-Gel Alumina Dielectric for

and transistors.

transitive to improve the performance of printed diode

functions from 3.5eV to 5eV could be prepared on

technique, printed electrode with various work

technique for printed metal patterns. Using this

Takada, T. Kodzasa and T. Kamata, AIST (JAP AN)

M. Yoshida, K. Suemori, S. Uemura, S. Hoshino, N.

Printed Electrode for All-Printed Polymer Diode

Fabrication

A-9: Organic Transistors and Device

Fabrication

A-9: Organic Transistors and Device

16:30 A-9-5

An organic phospher C-545T was used as a green

light dopant in this study. After protonation the

An organic phospher C-545T was used as a green

Univ. (Taiwan)

W. T. Liu and W. Y. Huang, National Sun Yat-sen

induced Color-Change Materials

16:45 A-9-6

Uniaxial and Biaxial Strain Distribution Map-

1F 211 1F 212 1F 213 2F 221 4F 241 4F 242 4F 243 4F 244 4F 245 4F 246 2F 222 2F 223

1F 211 1F 212 1F 213 2F 221 4F 241 4F 242 4F 243 4F 244 4F 245 4F 246 2F 222 2F 223

1

Seoul National Univ. and

SS=60mV/dec, DIBL=7mV.

Floating beam structure which is formed by removal

of its underlying SiO2 layer.

Floating beam structure which is formed by removal

of its underlying SiO2 layer.

2

JSPS (Japan)

, T. Sadoh

1

and M. Miyao

1

1

1

1

1

MIRAI-Selete,

and S. Yokoyama

1,2

3

AIST (Japan)

, M. Nakada

1,2

, T. Takahashi

1

, S. Aoyagi

2

NEC

1,2

K. C. Ryoo

1

1

1

1

1

H. Jeong

2

Samsung

1

1

C. W. Lee, I. Ferain, A. Kranti, N. Dehdashti Akha

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,

Cork (Ireland)

M. White, A. M. Kelleher, B. McCarthy, S. Gheo

van, P . Razavi, R. Yan, R. Yu, B. O'Neill, A. Blake,