2004 International Conference on Solid State Devices and Materials (SSDM 2004)

SECRETARIAT
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ADVANCE PROGRAM

2004 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference—September 15-17, 2004
Short Course—September 14, 2004
Place—Tower Hall Funabori (Tokyo, Japan)

Late News Paper Deadline—July 25, 2004

Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS
Technical-Cosponsored by
IEEE Electron Devices Society
in cooperation with
The Electrochemical Society of Japan
IEEE EDS Japan Chapter
IEEE Japan Council
The Institute of Electrical Engineers of Japan
The Institute of Electronics, Information and Communication Engineers
The Institute of Image Information and Television Engineers
Japan Institute of Electronics Packaging
Marubun Research Promotion Foundation

Website : http://www.ssdm.jp

SSDM 2004 Time Table

Wednesday, September 15

LARGE HALL

10:00-12:30 PL: Opening Session

Room A (ZUIUN)	Room B (HEIAN)	Room C (TOUGEN)	Room D (FUKUJU)	Room E (Small Hall)	Room F (Training Room)	Room H (303)	Room I (307)
14:00-16:00 **Area 2: Advanced Silicon Devices and Device Physics** A-1: Advanced Devices I	**14:00-15:50** **Area 3: Silicon Process/Materials Technologies** B-1: High-K Gate Dielectric I		**14:00-15:50** **Area 10: Non-Volatile Memory Technologies** D-1: Non-Volatile Memory Technologies I	**14:00-15:50** **Area 5: New Materials and Characterization for Silicon LSIs** E-1: Nano Materials & Characterization	**14:00-16:00** **Area 6: Compound Semiconductor Materials and Devices** F-1: Optical Devices	**14:00-16:00** **Area 8: Novel Devices, Physics and Fabrication** H-1: Nanoelectronics and Nanodevices	**14:00-15:50** **Area 1: Advanced Silicon Circuits and Systems** I-1: High Speed Digital
16:15-18:15 **Area 2: Advanced Silicon Devices and Device Physics** A-2: High-K Dielectrics/Metal Gate Stack	**16:15-18:15** **Area 3: Silicon Process/Materials Technologies** B-2: Interconnect			**16:15-18:05** **Area 5: New Materials and Characterization for Silicon LSIs** E-2: High-K Reliability	**16:15-18:15** **Area 6: Compound Semiconductor Materials and Devices** F-2: III-V Electronic Devices	**16:15-18:15** **Area 8: Novel Devices, Physics and Fabrication** H-2: Si Nanodevices	**16:15-17:45** **Area 1: Advanced Silicon Circuits and Systems** I-2: Low Power Analog
		18:30-20:30 Banquet					

Thursday, September 16

Room A (ZUIUN)	Room B (HEIAN)	Room C (TOUGEN)	Room D (FUKUJU)	Room F (Training Room)	Room G (401)	Room H (303)	Room I (307)
9:15-10:45 **Area 13: Organic Semiconductor Devices and Materials** A-3: Organic LED I	**9:15-10:45** **Area 3: Silicon Process/Materials Technologies** B-3: Silicide & Junction	**9:15-10:35** **Area 5: New Materials and Characterization for Silicon LSIs** C-3: Gate Dielectrics Characterization I	**9:15-10:45** **Area 10: Non-Volatile Memory Technologies** D-3: Non-Volatile Memory Technologies II	**9:15-10:45** **Area 12: System-Level Integration and Packaging Technologies** F-3: 3D&Interconnect	**9:15-11:00** **Area 11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** G-3: High Speed and Photonic Devices and IC's	**9:15-10:45** **Area 8: Novel Devices, Physics and Fabrication** H-3: Novel Devices and Characterization	
11:00-12:30 **Area 13: Organic Semiconductor Devices and Materials** A-4: Organic LED II	**11:00-12:20** **Area 2: Advanced Silicon Devices and Device Physics** B-4: Advanced Memory Technology	**11:00-12:30** **Area 5: New Materials and Characterization for Silicon LSIs** C-4: Strained Si/SiGe/Ge Devices & Materials	**11:00-12:30** **Area 10: Non-Volatile Memory Technologies** D-4: Non-Volatile Memory Technologies III	**11:00-12:15** **Area 12: System-Level Integration and Packaging Technologies** F-4: Wafer Level Integration	**11:15-12:00** **Area 11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications** G-4: GaN Devices and their Applications	**11:00-12:30** **Area 8: Novel Devices, Physics and Fabrication** H-4: Nanowires and Nanotubes	**11:00-12:15** **Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications** I-4: N/MEMS for Bio-and Chemical Applications I
13:15-15:00 Poster Session (Exhibition Hall)							
15:15 -16:30 **Area 2: Advanced Silicon Devices and Device Physics** A-5: Novel Device and Sensors	**15:15-16:35** **Area 3: Silicon Process/Materials Technologies** B-5: Metal Gate Electrode	**15:15-16:35** **Area 4: Silicon-on-Insulator Technologies** C-5: SOI-Device Applications	**15:15-16:30** **Area 6: Compound Semiconductor Materials and Devices** D-5: GaN Electronic Devices I	**15:15-16:45** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** F-5: Photonic Crystal Fibers and Devices		**15:15-16:35** **Area 1: Advanced Silicon Circuits and Systems** H-5: Image Sensing and Processing	**15:15-16:30** **Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications** I-5: N/MEMS for Bio-and Chemical Applications II
	17:00-18:20 **Area 3: Silicon Process/Materials Technologies** B-6: Advanced Process	**17:00-18:00** **Area 4: Silicon-on-Insulator Technologies** C-6: SOI-Device Characterization	**17:00-18:00** **Area 6: Compound Semiconductor Materials and Devices** D-6: GaN Electronic Devices II	**17:00-18:15** **Area 12: System-Level Integration and Packaging Technologies** F-6: System in Package		**17:00-18:00** **Area 1: Advanced Silicon Circuits and Systems** H-6: Memory Cicuits	**17:00-18:00** **Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications** I-6: N/MEMS for Bio-and Chemical Applications III

18:30-20:30 Rump Session
Room A "Why don't you enjoy High-K Science?"
Room B "Challenges of Spintronics: from basic physics to nanoscale devices"

Friday, September 17

Room A (ZUIUN)	Room B (HEIAN)	Room C (TOUGEN)	Room D (FUKUJU)	Room F (Training Room)	Room G (401)	Room H (303)	Room I (307)
9:15-10:35 **Area 2: Advanced Silicon Devices and Device Physics** A-7: Advanced Gate Stack and DRAM	**9:15-10:15** **Area 3: Silicon Process/Materials Technologies** B-7: High-K Gate Dielectric II	**9:15-10:35** **Area 4: Silicon-on-Insulator Technologies** C-7: SOI-Strained Technology	**9:15-10:30** **Area 6: Compound Semiconductor Materials and Devices** D-7: GaN-Optical Devices	**9:15-10:30** **Area 13: Organic Semiconductor Devices and Materials** F-7: Molecular Electronics	**9:15-10:30** **Area 9: Quantum Nanostructure Devices and Physics** G-7: Fabrication and Characterization	**9:15-10:30** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-7: Quantum Effect Photonic Devices	
10:45-12:05 **Area 2: Advanced Silicon Devices and Device Physics** A-8: Advanced Devices II	**10:45-12:25** **Area 3: Silicon Process/Materials Technologies** B-8: High-K Gate Dielectric III	**10:45-12:05** **Area 4: Silicon-on-Insulator Technologies** C-8: SOI-Materials	**10:45-12:15** **Area 6: Compound Semiconductor Materials and Devices** D-8: GaN-Crystal Growth	**10:45-12:15** **Area 13: Organic Semiconductor Devices and Materials** F-8: Organic Electronics	**10:45-12:15** **Area 9: Quantum Nanostructure Devices and Physics** G-8: Quantum Devices and Circuits	**10:45-12:15** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-8: All-Optical Signal Processing	
13:45-15:05 **Area 2: Advanced Silicon Devices and Device Physics** A-9: Nanoscale Device Physics	**13:45-15:05** **Area 3: Silicon Process/Materials Technologies** B-9: DRAM	**13:45-15:05** **Area 5: New Materials and Characterization for Silicon LSIs** C-9: Gate Dielectrics Characterization II	**13:45-15:15** **Area 6: Compound Semiconductor Materials and Devices** D-9: Fe-Si	**13:45-15:15** **Area 13: Organic Semiconductor Devices and Materials** F-9: Organic FET I	**13:45-15:15** **Area 9: Quantum Nanostructure Devices and Physics** G-9: Control of Quantum State	**13:45-15:15** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-9: Semiconductor Lasers	
15:30-16:50 **Area 2: Advanced Silicon Devices and Device Physics** A-10: Analog Devices and Compact Modeling	**15:30-16:50** **Area 4: Silicon-on-Insulator Technologies** B-10: SOI-3D Structure	**15:30-16:30** **Area 5: New Materials and Characterization for Silicon LSIs** C-10: High-K Dielectrics	**15:30-16:45** **Area 6: Compound Semiconductor Materials and Devices** D-10: Wide-Gap Materials	**15:30-16:15** **Area 13: Organic Semiconductor Devices and Materials** F-10: Organic FET II	**15:30-16:45** **Area 9: Quantum Nanostructure Devices and Physics** G-10: Quantum Dots	**15:30-16:45** **Area 7: Optoelectronic Devices and Photonic Crystal Devices** H-10: Optical Filters and Detectors	

SSDM 2004 Advance Program
General Information

DATE
Conference: **September 15-17, 2004 (Official language is English)**
Short Course: **September 14, 2004 (in Japanese)**

LOCATION
Tower Hall Funabori
4-1-1 Funabori, Edogawa-ku, Tokyo 134-0091, Japan
Phone: +81-3-5676-2211 Fax: +81-3-5676-2501
Tower Hall Funabori is a landmark facility in Edogawa ward. Edogawa ward is an historic and cultural center in Tokyo, located adjacent to the business and coastal areas of Tokyo.
For further information (*Japanese only), see
http://www.city.edogawa.tokyo.jp/shisetsu/bunka/bunka1.html

About Edogawa Ward
http://www.city.edogawa.tokyo.jp/english/profile.html

REGISTRATION
The registration desk will be open from September 14th to 17th. The registration hours are as follows:

September	14	9:00-17:00	Front of Secretariat "Hourai, 2F"
	15	9:00-12:00	Front of "Large Hall 5F"
	15	13:00-17:00	Front of Secretariat "Hourai, 2F"
	16	9:00-17:00	Front of Secretariat "Hourai, 2F"
	17	9:00-15:30	Front of Secretariat "Hourai, 2F"

Advance registration is accepted only through the conference website before September 1, 2004. (http://www.ssdm.jp) After that date, registration can be made at the conference site. Early registration is recommended.

	Registration Fee		Short Courses in Japanese	Banquet
	On or before August 14	After August 14		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanying person(s)				¥4,000/person

1) The registration fee includes one copy of the abstract book, a CD-ROM. However, it does not include the Banquet, and extra payment of ¥7,000 or ¥4,000 is required to attend the Banquet for regular participants and student participants, respectively.
2) Those who register as students are required to fax a copy of their current student ID to the secretariat at the time of registration, and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of online registration of individual information.
3) Registration is complete only with full payment.

Payment of the registration fee is to be made by one of the following methods. Please note that we do not accept personal checks.

1. Bank Transfer
A direct bank transfer can be made to the account below. A copy of the receipt for the bank remittance should be sent to the secretariat by fax. The registration ID must be written on the fax sheet. Please note that the bank service charge must be borne by the applicant.
- Name of Bank: Bank of Tokyo-Mitsubishi, Akasaka Branch
- Account Name: SSDM2004
- Account No.: 1528425 (ordinary deposit)

2. Credit Card
VISA, MasterCard and JCB are acceptable.

Confirmation of Pre-Registration
The Secretariat will e-mail a confirmation to you after verifying payment in early September. Please print the confirmation slip out, bringing it with you to the conference and present it at the registration desk.

REGISTRATION CANCELLATION
Conference:
Cancellation fee of ¥3,000 will be deducted from the refund. Cancellation should be made in writing to the SSDM 2004 Secretariat. No cancellation will be accepted after August 19, 2004. Extended Abstracts will be sent to absent registrants after the Conference.

Short Course:
Cancellation fee of ¥2,000 will be deducted from the refund. Cancellations should be made in writing to the SSDM 2004 Secretariat. No cancellation will be accepted after August 19. A text will be sent to the absent registrants after the Conference.

BANQUET
Banquet will be held at "Fukuju and Tougen" of Tower Hall Funabori (2F) on September 15 from 18:30-20:30. Tickets (Regular ¥7,000 / Student ¥4,000) can be purchased at the registration desk.
To Purchase Banquet ticket through our website is recommended. The URL is http://www.ssdm.jp.

LATE NEWS PAPERS

Late News Paper Deadline is July 25, 2004.

Late news papers describing important new developments may be submitted. A 2-page abstract must be sent in the camera-ready format as required for the regular papers. The accepted papers will be included in the extended abstracts.
The abstract must be submitted through the conference website: http://www.ssdm.jp
Notice of acceptance will be e-mailed by the middle of August.
The accepted papers for Late News will be on "Advanced Program Part II" which will be distributed at the venue during the conference.

SPECIAL Issue of JJAP
Authors of papers accepted for SSDM 2004 are encouraged to submit the original and significant part of the papers to the Special Issue of the Japanese Journal of Applied Physics. The special issue will be published in April 2005.

RUMP SESSIONS - September 16th (Thursday) 18:30-20:30

Session A (Room A, ZUIUN, 2F)

"Why Don't You Enjoy High-k Science?"
High-k materials have been tackled for scaled CMOS applications. Although the recent progress is remarkable, most of the problems in the high-k gate stack technology seem to be based on the fundamental material science. If it is the case, technology tunings or improvements will be in vain or take us a long time to the final success. On the other hand, high-k materials provide a number of interesting subjects to study. The static or dynamic motions of atoms and electrons in the highly ionic oxides under an electric field, the atom-scale characteristics at the ionic/non-ionic film interface, or the material properties of nanometer thick-ionic films, are just examples.
In addition, the glass science, the ionic conduction chemistry or the physics of the Schottky barrier formation will also be included in the high-k research. Those subjects are certainly related with CMOS applications directly or indirectly, but we would propose two engagements in the rump session. 1) Forget about the technology node of ITRS, and then 2) focus on extracting the essence of high-k materials science. You might hopefully catch something for breaking through the high-k technology hardships on the way to your home after the rump session.

Moderator: A. Nishiyama (Toshiba, Japan)
A. Toriumi (Univ. of Tokyo, Japan)

Organizer: A. Toriumi (Univ. of Tokyo, Japan)

Panelists: T.P. Ma (Yale Univ., USA)
R. Degraeve (IMEC, Belgium)
K. Shiraishi (Univ. of Tsukuba, Japan)
S. Saito (Hitachi, Japan)

A couple of panelists will be further invited.

Session B (Room B, HEIAN, 2F)

"Challenges of Spintronics: from basic physics to nanoscale devices"
Recent progress in spintronics is brilliant. Many interesting topics, such as new spintronics devices based on metal and semiconductor nanostructures, spin control in semiconductors and its application to optical and electrical devices, and coherent control of spin for future quantum information processing, have been developed in spintronics.
In this rump session we will discuss these fascinating aspects of spintronics including the control of nuclear spin in solid-state systems. Our intention is to highlight the present status, remaining problems and future dreams of spintronics from viewpoints of basic physics and device applications.

Moderator: Y. Hirayama (NTT, Japan)
H. Munekata (Tokyo Tech, Japan)

Organizer: Y. Hirayama (NTT, Japan)

Panelists: K. Ando (AIST, Japan)
Y. Avishai (Ben-Gurion Univ., Israel)
H. Kosaka (Tohoku Univ., Japan)
J. Nitta (NTT, Japan)
K. H. Ploog (Paul-Drude-Institute, Germany)
S. Tahara (NEC, Japan)
M. Tanaka (Univ. of Tokyo, Japan)
S. Tarucha (Univ. of Tokyo, Japan)

(Tentative)

SHORT COURSE

Short Course entitled "The Latest JISSO Technology for SiP Solutions" will be held on Tuesday, September 14. All lectures are given in Japanese.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

Submission of an abstract for review and subsequent acceptance is considered by the committee as an agreement that the work will not be published by the author prior to the presentation at the conference. This policy will be enforced by the automatic withdrawal of the paper by the conference committee.

AWARDS

"SSDM Awards" will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for outstanding contribution to the field of solid state devices and materials, among papers presented prior to 1998.

SSDM Paper Award

Given for the best paper presented at SSDM 2003.

SSDM Young Researcher Award

For after excellent papers by young researchers presented at SSDM 2003.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of student ID should be submitted at application.

Travel Grant

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.
An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF) which is one of the cooperative organizations.

VISA REQUIREMENT

All foreign participants must have a valid passport. Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese Embassy or Consulate as soon as possible.

In general, each applicant is required to submit the following documents when applying for a visa:
(1) A letter of invitation (optional document written in English)
(2) A letter of guarantee (written in Japanese)
(3) Documents certifying the purpose of the visit (written in Japanese)
(4) The applicant's itinerary while in Japan (written in Japanese)

Please follow the steps outlined below when applying for a visa:

1. Contact the nearest Japanese Embassy and ask what documents are required to obtain a visa.
2. Contact the SSDM Secretariat and ask for a Reply Form for Visa Application, which is needed to obtain the required documents listed above.
3. When you receive the Reply Form for Visa Application, fill it out and return it to the Secretariat. All requested documents will be sent to you as soon as we receive the Reply Form.

OFFICIAL TRAVEL AGENT

JTB Corp.
Yokohama Group Tours Office
6F, 3-29-1 Tsuruya-cho, Kanagawa-ku, Yokohama 221-0835, Japan
Phone:+81-45-316-4602 Fax: +81-45-316-5703 E-mail: danyoko9@mnm.jtb.co.jp

Hotel accommodations

JTB has blocked rooms at following hotels in Tokyo for the conference period. Reservations can be made through the conference website. If the hotel of your first choice is fully booked, your second choice or a hotel in the same grade will be reserved.

No.	Hotel Name (Check-in & Check-out time)	Room Rates (per person, per night)		Address / Phone / Nearest Station / Access to the Site
		Single	Twin	
1	Hotel Grand Palace (12:00/12:00)	*¥15,115	¥8,085	1-1-1, Iidabashi, Chiyoda-ku, Tokyo +81-3-3264-1111 1 min.walk to Subway Toei Shinjuku Line Kudanshita Sta. 30 min. by Subway & walk to the site.
2	Tokyo Marriott Hotel Kinshicho Tobu (14:00/11:00)	*¥11,125	¥8,925	1-2-2, Kinshi, Sumida-ku,Tokyo +81-3-5611-5511 3 min. walk to Subway Hanzomon Line Kinshicho Sta. 20 min. by subway & walk to the site.
3	Hotel Park Lane Nishikasai (14:00/10:00)	*¥7,875	¥7,350	6-17-9, Nishikasai, Edogawa-ku, Tokyo +81-3-3675-8900 2 min. walk to Tozai Line Nishikasai Sta. 20 min. by Local Bus & walk to the site.
4	Mizue Daiichi Hotel (15:00/10:00)	*¥7,035	¥6,300	2-6-16, Mizue, Edogawa-ku, Tokyo +81-3-5243-8000 1 min. walk to Toei Shinjuku Line Mizue Sta. 10 min. by train & walk to the site.
5	Toyoko inn Tozaisen Nishikasai (16:00/10:00)	*¥6,500		5-11-12, Nishikasai, Edogawa-ku, Tokyo +81-3-5676-1045 1 min. walk to Tozai Line Nishikasai Sta. 20 min. by Local Bus & walk to the site.
6	Hotel Seaside Edogawa (**Japanese Style Room**) (14:00/10:00)	*¥13,586	¥8,536 (Twin) ¥6,885 (Triple) ¥6,335 (Fourth)	6-2-2 Rinkai-cho, Edogawa-ku, Tokyo +81-3-3804-1180 3 min. walk to JR Keiyo Line Kasairinkaikoen Sta. (3 min. by train to Tokyo Disney Land) 40 min. by Local Bus & walk to the site.

Notes: Room rates include tax and service charge. Only #5, #6 hotels include breakfast.
*Indicates single occupancy of a twin or double room

Application and payment

Participants wishing to reserve hotel accommodations should access the Accommodation page of the conference website. Reservations should be made by no later than August 20, 2004. (Confirmation sheet will be sent by JTB.)
Application should be accompanied by a remittance covering the total accommodation fee plus handling fee ¥525 due JTB.

No reservation will be confirmed in the absence of this payment. All payment must be in Japanese yen. If the remitter's name is different from the participant's name, or if the amount covers more than one person, please inform us of the details for the payment.

Payment should be made through:
- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. AMEX
- A bank transfer to JTB Corp. (Message: Ref:125772-002)
  Account at the Bank of Tokyo Mitsubishi, Yokohama Branch #480, 3-27-1 Honcho, Naka-ku, Yokohama-shi, Kanagawa 231-0005, Japan (Account number: 0043079)

Cancellation

In the event of cancellation, written notification should be sent to JTB. The following cancellation fees will be deducted before refunding.

Hotels: Up to 21 days before the arrival date...............¥525
2 to 20 days before...20% of daily room charge (minimum ¥525)
1 day before ....80% of daily room charge
On the day of arrival or no notice given...........100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Tokyo is warm and sometimes humid in September. The temperature range is 18-30˚C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

SSDM 2004 INSTRUCTION for SPEAKERS

<Oral Presentation>

Presentation Time

	Session Time	Presentation Time	Discussion
Plenary	45 min.	40 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of the presentation time, Third: End of the discussion time.

Audio-Visual Equipment

The meeting rooms will contain the following audiovisual equipment:
- LCD data projector (PC is not provided)
- Overhead projector
- Microphone
- Projection laser pointer

Speakers wishing to present their paper using LCD projector are requested to verify their PC's compatibility with the sample LCD projector that will be located in the "Preview Room" on the second floor, prior to their presentations.
They are also recommended to bring transparencies for overhead projector in case there is a problem with the LCD data projector. If presentations are interrupted due to problems caused by inadequate prior preparations, the time allotted to speakers will not be extended.

<Poster Presentation>

Poster sessions are scheduled on Thursday, September 16, from 13:15 to 15:00. Poster boards will be available with identifying labels at the Exhibition Hall, 1F. Authors are requested to prepare their posters between 9:00 and 12:00 on September 16, and remove their posters by 17:00 on September 16. The posters remaining after 17:00 will be disposed of by the secretariat. Usable space on each poster board will be approximately 1,100mm wide and 1,700mm high. Pushpins will be available. Each presentation will be assigned a board, labeled with the paper number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near their posters during the poster session for discussions.

Wednesday, September 15

Large HALL, 5F

PL: Opening Session (10:00 - 12:30)
Chairpersons: K. Masu, Tokyo Tech and J. Sone, NEC

10:00 PL-0
Welcome Address and Award Presentation
H. Ishiwara, Tokyo Tech

10:15 PL-1 (Plenary)
Our Challenges to Achieve an Advanced Science and Technology-Oriented Nation
M. Ohyama, Councile for Science and Technology Policy, Cabinet Office, Japan

11:00 PL-2 (Plenary)
Silicon-based Devices and Technology for the Nanoscale Era
J.D. Plummer, Stanford Univ., USA

11:45 PL-3 (Plenary)
Spintronics - From Materials to Circuits -
H. Ohno, Tohoku Univ., Japan

12:30-14:00 Lunch

Room A (ZUIUN)

Area 2: Advanced Silicon Devices and Device Physics

A-1: Advanced Devices I
(14:00-15:50)
Chairs: K. Shibahara (Hiroshima Univ.)
S. Inaba (Toshiba)

14:00 A-1-1 (Invited)
Gate Stress Induced Performance Enhancements
Z. Krivokapic, Q.Xiang, W. Maszara and M. Lin, *AMD, USA*

14:30 A-1-2
Physical Origin of Drive Current Enhancement in Ultra-thin Ge-On-Insulator (GOI) MOSFETs under Full Ballistic Transport
S. Takagi, *Univ. of Tokyo, Japan*

Room B (HEIAN)

Area 3: Silicon Process/Materials Technologies

B-1: High-K Gate Dielectric I
(14:00-15:50)
Chairs: M. Kubota (Matsushita Electric)
F. Ohtsuka (SELETE)

14:00 B-1-1 (Invited)
Electrical Characterization of High-k Gated MOSFETs and Interfaces
T.P. Ma, *Yale Univ.*, USA

14:30 B-1-2
Electron Mobility Degradation Mechanisms in HfSiON MISFETs under the Real Operating Condition
R. Iijima, M. Takayanagi, T. Ishihara, T. Yamaguchi and A. Nishiyama, *Toshiba Corp., Japan*

Room C (TOUGEN)

Room D (FUKUJU)

Area 10: Non-Volatile Memory Technologies

D-1: Non-Volatile Memory Technologies I
(14:00-15:50)
Chairs: T. Nakamura (Rohm)
Y. Shimada (Matsushita Electric)

14:00 D-1-1 (Invited)
Preparation of Novel PZTN Thin Film Co-doped Si
T. Kijima, Y.Hamada, T. Aoyama, E. Natori1 and T. Shimoda, *Seiko Epson Corp., Japan*

14:30 D-1-2
30-day-long Data Retention in Ferroelectric-gate FETs with HfO_2 Buffer Layers
K. Takahashi[1], B. E. Park[2], K. Aizawa[1] and H. Ishiwara[1], [1]*Tokyo Tech and* [2]*Univ. of Seoul, Japan*

Room E (Small Hall)

Area 5: New Materials and Characterization for Silicon LSIs

E-1: Nano Materials & Characterization
(14:00-15:50)
Chairs: K. Kikuta (NEC)
T. Kanayama (AIST)

14:00 E-1-1 (Invited)
Nanoelectronic Scaling Tradeoffs: What does Materials Physics have to say?
V. Zhirnov and R. Cavin, *Semiconductor Research Corporation, USA*

14:30 E-1-2
Dopant Profiling in Vertical Ultrathin Channel for Double-gate MOSFET by Scanning Nonlinear Dielectric Microscopy (SNDM)
M. Masahara, S. Hosokawa, T. Matsukawa, K. Endo, Y. Naitou, H. Tanoue, and E. Suzuki, *AIST, Japan*

Room F (Training Room)

Area 6: Compound Semiconductor Materials and Devices

F-1: Optical Devices
(14:00-16:00)
Chairs: K. Ohtani (Tohoku Univ.)
K. Kojima (Mitsubishi Electric)

14:00 F-1-1 (Invited)
Growth, Fabrication, and Operating Characteristics of Ultra-Low Threshold 1.31μm Quantum Dot Lasers
R. Hogg[1], K. M. Groom[1], H. Y. Liu[1], I. R. Sellers[2], S. K. Ray[1], T. Badcock[2], M. Gutierrez[1], M. Hopkinson[1], J. S. Ng[1], J. P. R. David[1], D. J. Mowbray[2] and M.S.Skolnick[2], [1]*Dept.of Electronic &Electrical Engineering, Univ. of Sheffield and* [2]*Dept.of Physics&Astronomy, Univ. of Sheffield, UK*

14:30 F-1-2
Temperature dependent photoluminescence of highly strained InGaAsN/GaAs Quantum Well (λ=1.28-1.45 μm) with GaAsP strain-compensated layer
Y. H. Chang[1], H. C.Kuo[1], Y. A. Chang[1], M. Y. Tsai[1], S. C. Wang[1], N. Tansu[2], J. Y. Yeh[3] and L. J. Mawst[3], [1]*National Chiao-Tung Univ.,* [2]*Lehigh Univ. and* [3]*Univ. of Wisconsin-Madison, Taiwan*

Room H (303)

Area 8: Novel Devices, Physics and Fabrication

H-1: Nanoelectronics and Nanodevices
(14:00-16:00)
Chairs: K. Ishibashi (RIKEN)
J. Motohisa (Hokkaido Univ.)

14:00 H-1-1 (Invited)
Nanoelectronics and Nanodevices:Issues in Future Information Processing
D. K. Ferry, *Arizona State Univ., USA*

14:30 H-1-2 (Invited)
Solid-Electrolyte Nanometer Switch Implemented in Si LSI
T. Sakamoto[1,2], S. Kaeriyama[3], H. Sunamura[1,2], M. Mizuno[3], H. Kawaura[1,2], T. Hasegawa[2,4], K. Terabe[2,4], T. Nakayama[2,4] and M. Aono[2,4], [1]*Fundamental & Environmental Research Labs., NEC Corp.,* [2]*JST,* [3]*System Devices Research Labs., NEC Corp., and* [4]*NIMS, Japan*

Room I (307)

Area 1: Advanced Silicon Circuits and Systems

I-1: High Speed Digital
(14:00-15:50)
Chairs: T. Kuroda (Keio Univ.)
M. Takamiya (NEC)

14:00 I-1-1 (Invited)
CMOS Scaling on I/O Design
C. K. K. Yang, M. Garg, and J. C. S. Woo, *UCLA, USA*

14:30 I-1-2
Fast-lock and Low-power DLL with Super-short Cyclic Delay Line
H. Nakaya, N. Katoh and Y. Sasaki, *Hitachi, Ltd., Japan*

Room A (ZUIUN)

14:50 A-1-3
Suppression of Boron Penetration from S/D Extension to improve Gate Leakage Characteristics and Gate-Oxide Reliability for 65nm node CMOS and beyond
T. Hayashi, T. Yamashita, K. Shiga, K. Hayashi, H. Oda, T. Eimori, M. Inuishi and Y. Ohji, *Renesas Technology Corp., Japan*

15:10 A-1-4
Dopant Profile Design Methodology for 65nm Generation via Inverse Modeling
T. Tanaka, M. Yamaji, H. Kanata, Y. Tagawa, S. Satoh and T. Sugii, *Fujitsu Ltd., Japan*

15:30 A-1-5
Strained-Si for CMOS 65nm node : $Si_{0.8}Ge_{0.2}$ SRB or "Low Cost" approach?
F. Boeuf[1], F. Payet[1], N. Casanova[1], Y. Campidelli[1], N. Villani[1], O. Kermarrec[1], H. Jean-Michel[2], E. Nicolas[1], L. Francois[1], M. Pierre[1], P. Cedric[1], C. Veronique[2], L. Cyrille[2], A. Franck[1] and J. Stephane[3], *[1]STMicroelectronics, [2]CEA-LETI and [3]Philips Semiconductor, France*

Room B (HEIAN)

14:50 B-1-3
Nitrogen profile engineering in the interfacial SiON for HfAlOx gate dielectric
R. Mitsuhashi, K. Torii, H. Ohji, T. Kawahara, A. Horiuchi, H. Takada, M. Takahashi and H. Kitajima, *SELETE, Japan*

15:10 B-1-4
Direct comparison of ZrO_2 and HfO_2 on Ge substrate in terms of the realization of ultra-thin high-k gate stacks
Y. Kamata, Y. Kamimuta, T. Ino and A. Nishiyama, *Toshiba Corp., Japan*

15:30 B-1-5
1.2nm HfSiON/SiON stacked gate insulators for 65nm-node MISFETs
M. Saitoh, N. Ikarashi, H. Watanabe, S. Fujieda, H. Watanabe, T. Iwamoto, A. Morioka, T. Ogura, M. Terai and K. Watanabe, *NEC Corp., Japan*

Room C (TOUGEN)

Room D (FUKUJU)

14:50 D-1-3
Fabrication and Characterization of 1k-bit 1T2C-Type Ferroelectric Memory Cell Array
H. S. Kim[1], S. Yamamoto[1], T. Ishikawa[2] and H. Ishiwara[1], *[1]Tokyo Tech and [2]R&D Association for Future Electron Devices, Japan*

15:10 D-1-4
Robust 3-Metallization BEOL Process for 0.18 μm Embedded FRAM
S. K. Kang, H. S. Rhie, H. H.Kim, B. J.Koo, H. J. Joo, J. H. Park, Y. M. Kang, D. Y. Choi, S. Y. Lee and K. Kim, *Samsung Electronics Co. Ltd., Korea*

15:30 D-1-5
Impact of the Grain Size and Orientation of $SrBi_2(Ta,Nb)_2O_9$ Films on the Polarization for Nano-Scale FeRAMs
K. Kaibara, K. Tanaka, K. Uchiyama and Y. Shimada, *Matsushita Electric Industrial Co. Ltd., Japan*

Break

Room E (Small Hall)

14:50 E-1-3
Study of L_{gate} dependence of 2-D carrier profile in N-FET by Scanning Tunneling Microscopy
H. Fukutome, T. Aoyama and H. Arimoto, *Fujitsu Labs. Ltd., Japan*

15:10 E-1-4
Simple Models on Enhancement of Mechanical Properties of Porous Silica Low-k Films by Tetramethylcyclotetrasiloxane (TMCTS) Vapor Annealing Treatment
Y. Seino[1], R. Ichikawa[1], Y. Takasu[1], K. Kohmura[2], H. Tanaka[2], S. Oike[2], M. Murakami[2] and T. Kikkawa[1,3], *[1]AIST, [2]ASET and [3]Hiroshima Univ., Japan*

15:30 E-1-5
Microstructure Characterization of Skeletal Silica in Porous Low-*k* Films by Infrared Spectroscopic Ellipsometry
S. Takada[1], N. Hata[1, 2], Y. Seino[1, 2], N. Fujii[2, 3] and T. Kikkawa[1, 2, 4], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*

Room F (Training Room)

14:45 F-1-3
Study of the electron properties by persistent photoconductive measurement in $Ga_xIn_{1-x}N_yAs_{1-y}$
S. H. Hsu, Y. K. Su, S. J. Chang and P. H. Wu, *National Cheng Kung Univ., Taiwan*

15:00 F-1-4 (Invited)
InGaAs-Based Quantum Wells for Ultrafast All-Optical Switches Using Intersubband Transitions
T. Mozume, J.Kasai, N.Georgiev, T.Simoyama, S.Sekiguchi, A.V.Gopal, H.Yoshida and H.Ishikawa, *FESTA Labs., Japan*

15:30 F-1-5
High-performance Multi-color InAs/AlGaAs Quantum Dot Infrared Photodetector
S. D. Chen, Y. Y. Chen and S. C. Lee, *National Taiwan Univ., Taiwan*

15:45 F-1-6
InP/InGaAs/InP Double Hetero-junction Solar Cells with Increased Open-Circuit Voltage
C. Y. Kim, J. H. Cha, J. Kim and Y. S. Kwon, *KAIST, Korea*

Room H (303)

15:00 H-1-3
Measurement of Two-Qubit States using a Two-Island Single Electron Transistor
T. Tanamoto[1], S. Fujita[1] and X. Hu[2], *[1]Toshiba Corp. and [2]Univ. at Buffalo, Japan*

15:15 H-1-4
Large Negative Resistance Property Observed in 3-D Network of DNA and Gold Nanoparticle Formed by DNA Mediated Self-organization
Y. Fujii, T. Shimizu, M. Hosoda, G. Wu, S. Huang, H. Sakaue, T. Takahagi and S. Shingubara, *Hiroshima Univ., Japan*

15:30 H-1-5
Significant Reduction of Phonon Scattering Potential in 1D Si Quantum Dot Array Interconnected with Thin Oxide Layers
S. Uno[1], N. Mori[2], K. Nakazato[3], N. Koshida[4] and H. Mizuta[5], *[1]Hitachi Cambridge Lab., [2]Osaka Univ., [3]Nagoya Univ., [4]Tokyo Univ. of Agriculture and Technology and [5]Tokyo Tech, UK*

15:45 H-1-6
Development of New Kinetic Monte Carlo Simulator for Theoretical Design of MgO Protecting Layer in Plasma Display
M. Kubo[1,2], T. Masuda[1], H. Tsuboi[1], M. Koyama[1], H. Kajiyama[3] and A. Miyamoto[1], *[1]Tohoku Univ., [2]PRESTO-JST and [3]Univ. of Tokyo, Japan*

Room I (307)

14:50 I-1-3
Digital Low-Power Real-Time Video Segmentation by Region Growing
T. Morimoto, O. Kiriyama, H. Adachi, T. Koide and H. J. Mattausch, *Hiroshima Univ., Japan*

15:10 I-1-4
18 GHz Operation of an 8-bit Microprocessor Based on a Single-Flux-Quantum LSI Technology
A. Fujimaki[1], M. Tanaka[1], T. Kondo[1], T. Kawamoto[1], Y. Yamanashi[2], N. Nakajima[2], A. Akimoto[2], N. Yoshikawa[2], H. Terai[3] and S. Yorozu[4], *[1]Nagoya Univ., [2]Yokohama National Univ., [3]National Institute of Information and Communications Technology and [4]Superconductivity Research Lab., Japan*

15:30 I-1-5
High-Speed Digital Systems by Hybridization of CMOS and Single-Flux-Quantum Logic Circuits
N. Yoshikawa[1], T. Tomida[1], K. Tokuda[1], Q. Liu[2], S. Whiteley[2] and T. V. Duzer[2], *[1]Yokohama National Univ. and [2]Univ. of California Berkeley, Japan*

Break

Room A (ZUIUN)

Area 2: Advanced Silicon Devices and Device Physics
A-2: High-K Dielectrics/Metal Gate Stack
(16:15-18:15)
Chairs: Y. Momiyama (Fujitsu)
C.C. Wu (TSMC)

16:15 A-2-1
Fully Silicided NiSi Gates on HfSiON Gate Dielectrics for Low Power Application
K. Manabe, K. Takahashi, T. Ikarashi, A. Morioka, H. Watanabe, T. Yoshihara and T. Tatsumi, *NEC Corp., Japan*

16:35 A-2-2
Weak Temperature Dependence of Non-Coulomb Scattering Component of $HfAlO_x$-Limited Inversion Layer Mobility in n^+poly-Si/$HfAlO_x$/SiO_2 n-MOSFETs
N. Yasuda[1], H. Hisamatsu[1], H. Ota[2] and A. Toriumi[2, 3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo, Japan*

16:55 A-2-3
High Mobility Dual Metal Gate MOS Transistors with High-k Gate Dielectrics
K. Takahashi, K. Manabe, A. Morioka, T. Ikarashi, T. Yoshihara, H. Watanabe and T. Tatsumi, *NEC Corp., Japan*

17:15 A-2-4
Temperature effects of constant bias stress on NFETs with Hf-based gate dielectric
R. Choi[1], B. H. Lee[2], C. D. Young[1], J. H. Sim[1] and G. Bersuker[1], *[1]International SEMATECH and [2]IBM, USA*

Room B (HEIAN)

Area 3: Silicon Process/Materials Technologies
B-2: Interconnect
(16:15-18:15)
Chairs: N. Kobayashi (SELETE)
T. Nakamura (Fujitsu)

16:15 B-2-1 (Invited)
Carbon nanotube technologies for future ULSI via interconnects
Y. Awano[1,2], M. Nihei[1,2], S.Sato[1,2], A. Kawabata[1,2], D.Kondo[1,2], M. Ohfuti[1,2] and N. Yokoyama[2], *[1]Fujitsu Ltd. and [2]Nanotechnology Research Center, Fujitsu Labs., Ltd., Japan*

16:45 B-2-2 (Invited)
Interface Adhesion and Phase Formation in Cu Interconnect
J. Koike, A. Sekiguchi and M. Wada, *Tohoku Univ., Japan*

17:15 B-2-3
Etch-byproduct Pore Sealing for ALD-TaN Deposition on Porous Low-k Film
A. Furuya, E. Soda, H. Okamura, N. Ohtsuka, M. Shimada, N. Ohashi and S. Ogawa, *SELETE, Japan*

17:35 B-2-4
Recovery of Process-induced Damages of Porous Silica Low-κ Films by TMCTS Vapor Annealing
Y. Oku[1], N. Fujii[1], Y. Seino[2], Y. Takasu[3], H. Takahashi[1], Y. Sonoda[1], T. Goto[1], H. Miyoshi[1], S. Takada[3] and T. Kikkawa[2,4], *[1]MIRAI-ASET, [2]MIRAI-ASRC-AIST, [3]ASRC-AIST and [4]Hiroshima Univ., Japan*

Room C (TOUGEN)

Room D (FUKUJU)

Room E (Small Hall)

Area 5: New Materials and Characterization for Silicon LSIs
E-2: High-K Reliability
(16:15-18:05)
Chairs: J. Yugami (Renesas)
M. Takayanagi (Toshiba)

16:15 E-2-1 (Invited)
Reliability Issues in High-k Stacks
R. Degraeve[1], F.Crupi[2], M. Houssa[1], D.H.Kwak[3], A.Kerber[4], E.Cartier[5], T.Kauerauf[1,6], Ph.Roussel[1], J.L.Autran[7], G.Pourtois[1], L.Pantisano[1], S.De Gendt[1], M.M.Heyns[1] and G.Groeseneken[1,6], *[1]IMEC, [2]Univ. of Calabria, [3]Samsung Electronics Co. Ltd., [4]Infineon Technologies, [5]IBM, [6]Catholic Univ. Leuven and [7]Univ. of Provence, Belgium*

16:45 E-2-2
Influences of Traps within HfSiON Bulk on Positive- and Negative-Bias Temperature Instability of HfSiON Gate Stacks
S. Fujieda, S. Kotsuji, A. Morioka, M. Terai and M. Saitoh, *NEC Corp., Japan*

17:05 E-2-3
Breakdown Mechanisms and Lifetime Prediction for 90nm-node Low-power HfSiON/SiO_2 CMOSFETs.
M. Terai, Y. Yabe, H. Watanabe, S. Fujieda, A. Morioka, S. Kotsuji, T. Iwamoto, M. Saitoh, T. Ogura and Y. Saito, *NEC Corp., Japan*

17:25 E-2-4
Degradation Mechanism of $HfAlO_X$/SiO_2 Stacked Gate Dielectric Films through Transient and Steady State Leakage Current Analysis
K. Okada[1], W. Mizubayashi[2], N. Yasuda[1], H. Ota[2], K. Tominaga[1], K. Iwamoto[1], T. Horikawa[2], K. Yamamoto[1], H. Hisamatsu[1] and H. Satake[1], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo, Japan*

Room F (Training Room)

Area 6: Compound Semiconductor Materials and Devices
F-2: III-V Electronic Devices
(16:15-18:15)
Chairs: T. Takahashi (Fujitsu Labs.)
N. Kobayashi (Univ. of Electro-Communications)

16:15 F-2-1
High performance 0.1μm GaAs PHEMT with Si pulse doped cap layer for 77GHz car radar applications
S. Kim, H. Noh, K. Jang and K. Seo, *Seoul National Univ., Korea*

16:30 F-2-2
Transconductance Linearity Improvement of E-pHEMT with High Vg.on
K. Jang, S. Kim, J. Lee and K. Seo, *Seoul National Univ., Korea*

16:45 F-2-3
InGaP/InGaAs DCFETs with Drain and Source Recess Process
F. T. Chien[1], J. M. Yin[1], S. T. Su[2], M. H. Lai[2], K. W. Tu[2] and C. L. Cheng[2], *[1]Feng Chia Univ., and [2]Chino-Excel Technology Corp., Taiwan*

17:00 F-2-4
A New Camel-Gate Field Effect Transistor with a Composite Channel Structure
P. H. Lai, C. H. Yen, C. I. Kao, H. M. Chuang, S. F. Tsai, C. Y. Chen and W. C. Liu, *National Cheng-Kung Univ., Taiwan*

Room H (303)

Area 8: Novel Devices, Physics and Fabrication
H-2: Si Nanodevices
(16:15-18:15)
Chairs: M. Tabe (Shizuoka Univ.)
D. K. Ferry (Arizona State Univ.)

16:15 H-2-1 (Invited)
Silicon Quantum Tunneling Devices-FIBTET and MOSET
B. G. Park, K. R. Kim, K. W. Song, H. H. Kim, J. I. Huh and J. D. Lee, *Seoul National Univ., Korea*

16:45 H-2-2
SET/CMOS Hybrid Integration Process for Multiple-Valued Logics
K. W. Song[1], Y. K. Lee[1], K. R. Kim[1], J. I. Huh[1], J. D. Lee[1], B. G. Park[1], J. Han[2] and Y. W. Kim[2], *[1]Seoul National Univ. and [2]Samsung Electronics Co. Ltd., Korea*

17:00 H-2-3
Room-Temperature Demonstration of Low-Voltage Static Memory Based on Negative Differential Conductance in Silicon Single-Hole Transistors
M. Saitoh[1], H. Harata[1,2] and T. Hiramoto[1], *[1]Univ. of Tokyo and [2]Chuo Univ., Japan*

17:15 H-2-4
Photo-Induced Electron Charging to Silicon-Quantum-Dot Floating Gate in Metal-Oxide-Semiconductor Memories
T. Nagai, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki, *Hiroshima Univ., Japan*

Room I (307)

Area 1: Advanced Silicon Circuits and Systems
I-2: Low Power Analog
(16:15-17:45)
Chairs: M. Takamiya (NEC)
T. Kuroda (Keio Univ.)

16:15 I-2-1 (Invited)
Sub-100nm MOSFET Modeling for Integrated-Circuit Design
A. Vladimirescu, *UC Berkeley, USA*

16:45 I-2-2
A Low-Noise Amplifier using Variable Degeneration Inductance
R. Fujimoto, H. Yoshida, A. Kuroda and S. Otaka, *Toshiba Corp., Japan*

17:05 I-2-3
A Low Noise Amplifier Using Chopper Stabilization for a Neural Sensor LSI
T. Yoshida, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu, *Hiroshima Univ., Japan*

17:25 I-2-4
Watchdog Circuit for Product Degradation Monitor using Subthreshold MOS Current
T. Hirose, R. Yoshimura, T. Ido, T. Matsuoka and K. Taniguchi, *Osaka Univ., Japan*

Room A (ZUIUN) | **Room B (HEIAN)** | **Room C (TOUGEN)** | **Room D (FUKUJU)**

Room A (ZUIUN)

17:35 A-2-5
Charge Trapping Characteristics of Hafnium Based High-κ Dielectrics with Various Metal Electrodes
C. Young[1], G. Bersuker[1], H. C. Wen[1], G. Brown[1] and P. Majhi[2], *[1]International Sematech and [2]Phillips, USA*

17:55 A-2-6
Dependences of Device Performances on Interfacial Layer Materials of High-k MISFETs due to Wave Function Penetration into Gate Dielectrics
M. Ono and A. Nishiyama, *Toshiba Corp., Japan*

Room B (HEIAN)

17:55 B-2-5
A Metallurgical Prescription Suppressing Stress-induced Voiding (SIV) in Cu lines
M. Abe, N. Furutake, S. Saito, N. Inoue and Y. Hayashi, *NEC Corp., Japan*

Room C (TOUGEN)

Room D (FUKUJU)

18:30-20:30 Banquet (TOUGEN FUKUJU 2F)

Room E (Small Hall) | **Room F (Training Room)** | **Room H (303)** | **Room I (307)**

Room E (Small Hall)

17:45 E-2-5
Universal thermal activation process and current induced degradation on dielectric breakdown in HfSiO(N)
T. Yamaguchi[1], I. Hirano[1], K. Sekine[2], S. Inumiya[2], K. Eguchi[2], M. Takayanagi[2] and N. Fukushima[1], *[1]Adv. LSI Tec. and [2]Semiconductor Company, Toshiba Corp., Japan*

Room F (Training Room)

17:15 F-2-5
Low-Frequency Noise Generated From High-Field Region in AlGaAs/InGaAs HEMTs
M. Wada, T. Nakamoto, S. Hamayoshi and K. Higuchi, *Hiroshima Univ., Japan*

17:30 F-2-6
Characteristics of an InGaAs/InGaAsP Composite-Collector Heterojunction Bipolar Transistor (CCHBT)
J. Y. Chen, C. Y. Chen, S. I.Fu, C. Y. Chang, C. H. Tsai and W. C. Liu, *National Cheng-Kung Univ., Taiwan*

17:45 F-2-7
Substrate Parasitic Current in InGaP/GaAs HBTs??
Y. H. Chang[1, 2] and Y. J. Hsieh[1], *[1]National Yunlin Univ. of Science and Technology and [2]Taiwan Spin Phenomena Integrated Nanotechnology Research Center, Taiwan*

18:00 F-2-8
Extraction of Temperature Dependent Conduction Band Offset in InGaP/GaAs HBT Using 1-D Simulation
C. H. Liao, C. W. Gwan and C. P. Lee, *National Chiao Tung Univ., Taiwan*

Room H (303)

17:30 H-2-5
Charge polarization effect on single-hole-characteristics in a two-dimensional Si multidot structure
R. Nuryadi, H. Ikeda, Y. Ishikawa and M. Tabe, *Shizuoka Univ., Japan*

17:45 H-2-6
Large Threshold Voltage Shift and Narrow Threshold Voltage Distribution in Ultra Thin Body Silicon Nanocrystal Memories
K. Yanagidaira[1,2], M. Saitoh[1] and T. Hiramoto[1], *[1]Univ. of Tokyo and [2]Chuo Univ., Japan*

18:00 H-2-7
Charge-state control of phosphorus donors in SOI MOSFET
Y. Ono, K. Nishiguchi, H. Inokawa, S. Horiguchi and Y. Takahashi, *NTT Basic Research Labs., Japan*

Room I (307)

18:30-20:30 Banquet (TOUGEN FUKUJU 2F)

Thursday, September 16

Room A (ZUIUN)

Area 13: Organic Semiconductor Devices and Materials

A-3: Organic LED I
(9:15-10:45)
Chairs: M. Iwamoto (Tokyo Tech)
H. Okada (Toyama Univ)

9:15 A-3-1 (Invited)
Research and Development of Organic Electroluminescent Devices and Application for Plastic Information Devices
Y. Ohmori and H.Kaiji, *Osaka Univ., Japan*

9:45 A-3-2
Enhancement of luminance yield of blue light organic light emitting diode
C. Y. Su[1], S. J. Jhang[1], F. S. Juang[2] and Y. F. Chen[1], *[1]Kun Shan Univ. of Science and Technology and [2]National Huwei Univ. of Science and Technology, Taiwan*

10:00 A-3-3
Efficient red electrophosphorescent devices based on starburst molecules
Y. Hino, H. Kajii and Y. Ohmori, *Osaka Univ., Japan*

10:15 A-3-4
Phosphorescence Decay Time of $Ir(ppy)_3$ in Tetrahydrofuran at Magnetic Field
T. Tsuboi and N. Aljaloudi, *Kyoto Sangyo Univ., Japan*

Room B (HEIAN)

Area 3: Silicon Process/Materials Technologies

B-3: Silicide & Junction
(9:15-10:45)
Chairs: T. Noda (Matsushita Electric)
S. Saito (NEC)

9:15 B-3-1 (Invited)
Integrating Diffusionless Anneals Into Advanced CMOS Technologies
R. Surdeanu[1], R. Lindsay[2], S. Severi[2], A.Satta[2], B. J. Pawlak[1], A. Lauwers[2], C. J. J. Dachs[1], K. Henson[2], S. McCoy[3], J. C. Gelpey[3] and X. Pages[4], *[1]Philips Research Leuven, [2]IMEC and [3]Vortek Industries, ASM International, Belgium*

9:45 B-3-2
Formation of Nickel Self-Aligned Silicide by Using Cyclic Deposition Method
K. Terashima, Y. Miura, N. Ikarashi, M. Oshida, K. Manabe, T. Yoshihara, M. Tanaka and H. Wakabayashi, *NEC Corp., Japan*

10:05 B-3-3
Germanium-induced Modulation of Work Function and Impurity Segregation Effect in Fully-Ni-germanosilicide ($Ni(Si_{1-x}Ge_x)$) Gate
Y. Tsuchiya, A. Kinoshita and J. Koga, *Toshiba Corp., Japan*

10:25 B-3-4
Reverse $CoSi_2$ Thermal Stability and Digitized Sheet Resistance Increase in Sub-90nm Poly-Si Lines
C. Y. Lo, Y. C. Peng, Y. M. Chen, S. S. Lin and W. M. Chen, *Taiwan Semiconductor Manufacturing Company Ltd., Taiwan*

Room C (TOUGEN)

Area 5: New Materials and Characterization for Silicon LSIs

C-3: Gate Dielectrics Characterization I
(9:15-10:35)
Chairs: H. Satake (ASET)
R. Degraeve (IMEC)

9:15 C-3-1
Experimental Clarification of Hydrogen-related Mechanism in NBT Degradation
Y. Mitani and H. Satake, *Toshiba Corp., Japan*

9:35 C-3-2
Trapping/de-trapping gate bias dependence of Hf-silicate dielectrics with poly and TiN gate electrode
J. H. Sim[1], R. Choi[1], B. H. Lee[2], C. Young[1], P. Zeitzoff[1] and G. Bersuker[1], *[1]International Sematech and [2]IBM, USA*

9:55 C-3-3
Ultra-Short Pulse I-V Characterization of the Intrinsic Behavior of High-κ Devices
C. Young[1], Y. Zhao[2], M. Pendley[1], B. H. Lee[1,3], K. Matthews[1], J. Sim[1], R. Choi[1], G. Bersuker[1] and G. Brown[1], *[1]International Sematech , [2]Keithley Instruments and [3]IBM, USA*

10:15 C-3-4
Determination of Polysilicon Gate Doping in High-κ or Oxynitride MOSFETs with Gate Electrode Fermi-Level Pinning
K. Ahmed and P. Kraus, *Applied Materials Inc., USA*

Room D (FUKUJU)

Area 10: Non-Volatile Memory Technologies

D-3: Non-Volatile Memory Technologies II
(9:15-10:45)
Chairs: T. Nakanishi (Fujitsu Labs.)
H. Takada (Mitsubishi Electric)

9:15 D-3-1 (Invited)
Recent Development in Phase Change Memory
R. Bez, *STMicroelectronics, Italy*

9:45 D-3-2
Programming Characteristics of PRAM
Y. T. Kim, Y. N.Hwang, K. H. Lee, S. H. Lee, C. W. Jeong, S. J. Ahn, F. Yeung, G. H. Koh, H. S. Jeong W. Y. Chung, T. K. Kim, Y. K. Park, K. N. Kim and J. T. Kong, *Samsung Electronics Co. Ltd., Korea*

10:05 D-3-3
GST Confined Structure and Integration of 64Mb PRAM
F. Yeung, S. J. Ahn, Y. N. Hwang, C. W. Jeong, Y. J. Song, S. Y. Lee, S. M. Lee, K. C. Ryoo, J. H. Park J. M. Shin E. Y. Lee, W. C. Jeong, Y. T. Kim, K. H. Kon, G. T. Jeong, H. S. Jeong and K. N. Kim, *Samsung Electronics Co. Ltd., Korea*

10:25 D-3-4
Thermally Stable Magnetic Tunnel Junctions for High Density MRAM
S. Ikegawa[1], N. Ishiwata[2], M. Nagamine[1], T. Nagase[1], K. Nishiyama[1], H. Katsumata[3], T. Mitsuzuka[2], N. Ooshima[2], H. Honjo[2] T. Ueda[1], T. Kishi[1], Y. Asao[1], T. Tsuchida[1], H. Harada[2], T. Sugibayasi[2], S. Tahara[2] and H. Yoda[1], *[1]Toshiba Corp., [2]NEC Corp. and [3]Corporate Manufacturing Engineering Center, Toshiba Corp., Japan*

Room F (Training Room)

Area 12: System-Level Integration and Packaging Technologies

F-3: 3D&Interconnect
(9:15-10:45)
Chairs: K. Takahashi (ASET)

9:15 F-3-1 (Invited)
Process Realization for 3-D Ics using Fine Pitch Through Silicon Vias
L. Schaper, S.Spiesshoefer, S.Burkett, G.Vangara, Z.Rahman and S.Polamreddy, *Univ. of Arkansas, USA*

9:45 F-3-2
Application of High Reliable Silicon Thru-Via to Image Sensor CSP
K. Kameyama, Y. Okayama, M. Umemoto, A. Suzuki, H. Terao, M. Hoshino and K. Takahashi, *ASET, Japan*

10:00 F-3-3
Pyramid Bumps for Fine-Pitch Chip-Stack Interconnection
N. Watanabe and T. Asano, *Kyushu Institute of Technology, Japan*

10:15 F-3-4
Connection Test of Area Bump Using Active-Matrix Switches
N. Watanabe, S. Hasegawa and T. Asano, *Kyushu Institute of Technology, Japan*

Room G (401)

Area 11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

G-3: High Speed and Photonic Devices and IC's
(9:15-11:00)
Chairs: N. Suematsu (Mitsubishi Electric)
K. Oda (Hitachi)

9:15 G-3-1 (Invited)
Challenges to Achieve THz SiGe HBTs
G. Freeman, D. Greenberg, J.S. Rieh and A. Stricker, *IBM, USA*

9:45 G-3-2
Over-100-Gbit/s Multiplexing Operation of InP DHBT Selector IC Designed with High Collector-Current Density
K. Sano, K. Ishii, K. Murata, K. Kurishima, M. Ida, T. Shibata, T. Enoki and H. Sugahara, *NTT Corp., Japan*

10:00 G-3-3
W-band Waveguide Amplifier Module with InP-HEMT MMIC for Millimeter-wave Applications
T. Kosugi, T. Shibata, M. Tokumitsu, T. Enoki, M. Muraguchi, H. Ito and T. Ito, *NTT Photonics Labs., Japan*

10:15 G-3-4 (Invited)
Recent Developments in Photonic and mm-Wave Components for 60 GHz Fibre Radio
S. Iezekiel, *Univ. of Leeds, UK*

Room H (303)

Area 8: Novel Devices, Physics and Fabrication

H-3: Novel Devices and Characterization
(9:15-10:45)
Chairs: Y. Kuwahara (Osaka Univ.)
Y. Miyamoto (Tokyo Tech)

9:15 H-3-1
New Operation Mode of Nanocrystalline Silicon Ultrasonic Emitter for the Use as an Audio Speaker
A. Kiuchi and N. Koshida, *Tokyo Univ. of Agriculture and Technology, Japan*

9:30 H-3-2
Fabrication of single electron transistors with molecular tunnel barriers using AC dielectrophoresis technique
S. H. Hong[1], H. K. Kim[1,2], K. S. Jeon[1], J. S. Hwang[2], D. J. Ahn[1], S. W. Hwang[1,2] and D. Ahn[2], *[1]Korea Univ. and [2]Institute of Quantum Information Processing and Systems, Korea*

9:45 H-3-3
Electrical Transport Properties of Au-Doped DNA Molecules
J. S. Hwang[1], S. H. Hong[1,2], H. K. Kim[1,2], Y. W. Kwon[2], J. I. Jin[2], S. W. Hwang[1,2] and D. Ahn[1], *[1]Univ. of Seoul and [2]Korea Univ., Korea*

10:00 H-3-4
Structural Study of Metallic Growth on Yttria-Stabilized Zirconia Single Crystal by Coaxial Impact-Collision Ion Scattering Spectroscopy
A. Saito[1,2,3], K. Shimizu[1], S. Ohnisi[1], M. Akai-Kasaya[1,3], Y. Kuwahara[1,2,3] and M. Aono[1,3,4], *[1]Osaka Univ., [2]RIKEN Harima Institute, [3]Nanoscale Quantum Conductor Array Project, ICorp. and [4]Nanomaterials Lab., National Institute for Materials Science, Japan*

Room I (307)

Room A (ZUIUN)

10:30 A-3-5
Lifetime property of flexible organic light emitting diodes with plasma polymer barrier layers
S. Sohn, S. Kho, K. Kim and D. Jung, *Sungkyunkwan Univ., Korea*

Room B (HEIAN)

Room C (TOUGEN)

Room D (FUKUJU)

Room F (Training Room)

10:30 F-3-5
Interfacial Microstructure and Joint Properties of Copper Direct Bond Inserted by the Thin File of Indium
K. Taniguchi[1], T. Goto[1], K. Yasuda[2] and K. Fujimoto[2], *[1]Fuji Electric Advanced Technology Co.,Ltd and [2]Osaka Univ., Japan*

Room G (401)

10:45 G-3-5
Monolithic integration of UTC-PDs and InP HBTs using Be ion implantation
N. Kashio, S. Yamahata, M. Ida, K. Kurishima, K. Sano and T. Enoki, *NTT Photonics Labs., Japan*

Room H (303)

10:15 H-3-5
Formation of Nanometer-Scale Dislocation Network Sandwiched by Silicon-on-Insulator Layers
Y. Ishikawa[1], K. Yamauchi[1], H. Ikeda[1], Y. Ono[2], M. Nagase[2] and M. Tabe[1], *[1]Shizuoka Univ. and [2]NTT Corp., Japan*

10:30 H-3-6
Growth of High-Quality Carbon Nanotubes by Grid-Inserted Plasma-Enhanced Chemical Vapor Deposition for Field Emitters.
Y. Kojima, S. Kishimoto, Y. Ohno and T. Mizutani, *Nagoya Univ., Japan*

Room I (307)

Break

Area 13: Organic Semiconductor Devices and Materials

A-4-Organic LED II
(11:00-12:30)
Chairs: Y. Ohmori (Osaka Univ.)
H. Usui (Tokyo Univ. of Agriculture and Technol.)

11:00 A-4-1
Enhanced Luminance Efficiency from Organic Light-Emitting Diodes with 2D Photonic Crystal
M. Kitamura[1], S. Iwamoto[1,2] and Y. Arakawa[1,2], *[1]Research Center for Advanced Science and Technology, Univ. of Tokyo and [2]Institute of Industrial Science, Univ. of Tokyo, Japan*

11:15 A-4-2
The transfer of emission site in polymer LEDs with increasing voltages
N. Takada, K. Tsutsumi and T. Kamata, *AIST, Japan*

Area 2: Advanced Silicon Devices and Device Physics

B-4: Advanced Memory Technology
(11:00-12:20)
Chairs: S. Inaba (Toshiba)
C.C. Wu (TSMC)

11:00 B-4-1 (Invited)
Device Design Consideration for 50nm DRAM Using the Bulk FinFET
T. Park[1], K. R. Han[2], B. G. Choi[2], E. Yoon[1] and J. H. Lee[2], *[1]Seoul National Univ., [2]Kyungpook Univ., Korea*

11:30 B-4-2
Highly Manufacturable 64M bit Ultra Low Power SRAM Using a Novel 3-Dimensional S^3 (Stacked Single-crystal Si) Cell Technology
W. Cho, H. Lim, J. H. Jang, S. M. Jung, Y. H. Kang, J. H. Moon, C. D. Yeo, K. H. Kwak, B. H. Choi and B. J. Hwang, *Samsung Electronics Co. Ltd., Korea*

Area 5: New Materials and Characterization for Silicon LSIs

C-4: Strained Si/SiGe/Ge Devices&Materials
(11:00-12:30)
Chairs: J. Murota (Tohoku Univ.)
A. Sakai (Nagoya Univ.)

11:00 C-4-1 (Invited)
High-Perfection Approaches to Si-based Devices through Strained Layer Epitaxy
J. C. Sturm[1], H. Yin[1,2], R. L. Peterson[1], K. D. Hobart[3], F. J. Kub[3], *[1]Princeton Univ., [2]IBM Watson Reserch Center, [3]Naval Research Lab., USA*

11:30 C-4-2
Analysis and modeling of size dependent mobility enhancement due to mechanical stress
T. Tanaka, K. Goto, R. Nakamura and S. Satoh, *Fujitsu Ltd., Japan*

Area 10: Non-Volatile Memory Technologies

D-4: Non-Volatile Memory Technologies III
(11:00-12:30)
Chairs: T. Kobayashi (Hitachi)
K. Saito (NEC)

11:00 D-4-1 (Invited)
Future Trends in NAND-Type Flash Memory
R. Shirota, *Toshiba Corp., Japan*

11:30 D-4-2
A Highly Scalable Split-Gate SONOS Flash Memory with Programmable-Pass and Pure-Select Transistors for Sub-90-nm Technology
Y. K. Lee[1], B. Y. Choi[1], J. S. Sim[1], K. W. Song[1], J. D. Lee[1], B. G. Park[1], D. Park[2] and C. Chung[2], *[1]Seoul National Univ. and [2]Samsung Electronics Co. Ltd., Korea*

Area 12: System-Level Integration and Packaging Technologies

F-4: Wafer Level Integration
(11:00-12:15)
Chairs: T. Asano (Kyushu Inst. of Technol.)
M. Kimura (Renesas)

11:00 F-4-1 (Invited)
Wafer Level Package Integrated Functions
G. Carchon and E. Beyne, *IMEC, Belgium*

11:30 F-4-2
On-chip Spiral Inductors Integrated with Wafer-Level Package
M. Sato[1], K. Itoi[1], H. Abe[1], H. Sugawara[2], H. Ito[2], K. Okada[2], K. Masu[2] and T. Ito[1], *[1]Fujikura Ltd. and [2]Tokyo Tech, Japan*

Area 11: SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications

G-4: GaN Devices and their Applications
(11:15-12:00)
Chairs: H. Miyamoto (NEC)
K. Morizuka (Toshiba)

11:15 G-4-1 (Invited)
An Over 100 W GaN-HEMT High Power Transmitter Amplifier for Wireless Base Station with High Reliability
T. Kikkawa, *Fujitsu Labs. Ltd., Japan*

11:45 G-4-2
Strained Thick p-InGaN Layers for GaN/InGaN Heterojunction Bipolar Transistors on Sapphire Substrates
T. Makimoto[1], Y. Yamauchi[2], T. Kido[3], K. Kumakura[1], Y. Taniyasu[1], M. Kasu[1] and N. Matsumoto[1], *[1]NTT Basic Research Labs., [2]NEL TechnoSupport and [3]Shonan Institute of Technology, Japan*

Area 8: Novel Devices, Physics and Fabrication

H-4: Nanowires and Nanotubes
(11:00-12:30)
Chairs: K. Matsumoto (Osaka Univ.)
Y. Homma (Tokyo Univ. Sci.)

11:00 H-4-1 (Invited)
InP nanowires and nanotubes for bottom-up nanoelectronics
E. P. A. M. Bakkers[1], J. A. van Dam[2], S. D. Franceschi[2], L. P. Kouwenhoven[2], M. Kaiser[1], M. Verheijen[1], H. Wondergem[1] and P. van der Sluis[1], *[1]Philips Research Laboratories and [2]Delft Univ. of Technology, Netherlands*

11:30 H-4-2
Quantum dot transport of semiconducting single-wall carbon nanotubes
D. Tsuya[1,2], M. Suzuki[1,3], Y. Aoyagi[2] and K. Ishibashi[1,3], *[1]RIKEN, [2]Tokyo Tech and [3]CREST-JST, Japan*

Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications

I-4: N/MEMS for Bio-and Chemical Applications I
(11:00-12:15)
Chairs: M. Kamahori (Hitachi)
K. Shimoide (Asahi Kasei)

11:00 I-4-1 (Invited)
Integrated Microsensors
D.R.S. Cumming, P. A. Hammond and M. J. Milgrew, *Univ. of Glasgow, UK*

11:30 I-4-2
in-vivo Wireless Communication System for Bio MEMS Sensors
K. Okada[1], T. Yamada[1], T. Uezono[1], K. Masu[1], A. Oki[2] and Y. Horiike[2], *[1]Tokyo Tech and [2]National Institute for Materials Science, Japan*

Room A (ZUIUN)

11:30 A-4-3
VERTICAL TYPE ORGANIC LIGHT EMITTING TRANSISTOR USING THIN-FILM ZnO
H. Iechi[1,2,3], M. Sakai[2,3], M. Nakamura[2] and K. Kudo[2,3], *[1]Ricoh Co. Ltd, [2]Chiba Univ. and [3]Optoelectronic Industry Tech, Japan*

11:45 A-4-4
Preparation of polymer-based light-emitting field-effect transistors
T. Sakanoue[1], E. Fujiwara[2], R. Yamada[1,2] and H. Tada[1,2,3], *[1]The Graduate Univ. for Advanced Studies, [2]Institute for Molecular Science, NINS and [3]CREST-JST, Japan*

12:00 A-4-5
Organic Bi-Function Matrix Array
Y. Matsushita[1], H. Shimada[1], T. Miyashita[1], M. Shibata[1,2], S. Naka[1,2], H. Okada[1,2] and H. Onnagawa[1,2], *[1]Toyama Univ. and [2]Innovation Plaza Tokai, JST, Japan*

12:15 A-4-6
Theoretical Investigation of the Electronic Properties of PEDOT: PSS Conducting Polymer on Indium Tin Dioxide (ITO) Surface: an Accelerated Quantum Chemical Molecular Dynamics Method
C. Lv[1], X. Wang[1], A. Govindasamy[1], H. Tsuboi[1], M. Koyama[1], M. Kubo[1,2] and A. Miyamoto[1], *[1]Tohoku Univ., and [2]Japan Science and Technology, Japan*

Room B (HEIAN)

11:50 B-4-3
Re-examination of Impact of Intrinsic Dopant Fluctuations on SRAM Static Noise Margin
F. Tachibana and T. Hiramoto, *Univ. of Tokyo, Japan*

12:10 B-4-4
Improvements and Analysis of Neutron Induced Soft Error and Latch-up in High Speed Full CMOS 6T SRAM Products up to 65nm Technology
S. M. Jung, H. Lim, W. Cho, J. Jeong, Y. Rah, J. Park, K. Lee, J. Lee, K. Cha and C. Chang, *Samsung Electronics Co. Ltd., Korea*

Room C (TOUGEN)

11:50 C-4-3
Fabrication and Characteristics of Germanium-on-Insulator
Y. L. Chao[1], R. Scholz[2], M. Reiche[2], U. Gösele[2] and J. Woo[1], *[1]UCLA and [2]Max-Plank Institute of Microstructure Physics, USA*

12:10 C-4-4
Advantages of Ge (111) Surface for High Quality HfO_2/Ge Interface
M. Toyama, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

Room D (FUKUJU)

11:50 D-4-3
Flash EEPROM Tunneling Oxide Reliability Characterization under the test of FN Constant Current Stress and Program/Erase Cycling by using ISSG Nitrided Oxide.
C. W. Kuo[1], C. T. Huang[2], J. W. Chou[2], S. M. Tzeng[1], C. P. Lai[1], T. W. Tzeng[1], C. L. Liu[1], Y. E. Huang[1], W. Z. Wong[1], W. Z. Wong[1], H. C. Chang[2], H. C. Chang[2], C. S. Yang[1], S. Pittikoun[1], C. H. Chu[2] and C. C. Cho[1], *[1]Powerchip Semiconductor Corp. and [2]Ememory Technology Inc., Taiwan*

12:10 D-4-4
Impact of Co-salicide capping layer on GIDL in High Voltage devices for Embedded Flash memory
N. S. Kim, M. Mukho, J. Zhao, W. Y. Wong, K. J. How, Y. S. You, H. G. Yoon, D. Shukla, S. H. Han I. S. Goh, Q. Huang and Y. K. Ng, *System on Silicon Manufacturing Co. Ltd., Singapore*

Lunch

13:15-15:00 Poster Session (EXHIBITION HALL)

Room F (Training Room)

11:45 F-4-3
Small Area Snake Inductor on Si RF CMOS Chip
H. Sugawara, K. Okada and K. Masu, *Tokyo Tech, Japan*

12:00 F-4-4
Twisted Differential Transmission Line Structure for EMI Noise Reduction at Global Interconnect in Si LSI
H. Ito, S. Gomi, H. Sugita, K. Okada and K. Masu, *Tokyo Tech, Japan*

Room G (401)

12:00 G-4-3
Al_2O_3/Si_3N_4 Insulated Gate Channel-Doped AlGaN/GaN Heterostructure Field-Effect Transistors with Regrown Ohmic Layers: Low Gate Leakage Current with High Transconductance Operation
N. Maeda[1], T. Makimura[1], C. Wang[1], M. Hiroki[1], T. Makimoto[2], T. Kobayashi[1] and T. Enoki[1], *[1]NTT Photonics Labs. and [2]NTT Basic Research Labs., Japan*

Room H (303)

11:45 H-4-3
Ballistic Transport of Hole in p type Semiconductive Carbon nanotube
T. Kamimura[1,2], C. Hyon[2], A. Kojima[2], M. Maeda[2,3] and K. Matsumoto[1,2,4], *[1]Osaka Univ., [2]CREST-JST, [3]Univ. of Tsukuba and [4]AIST, Japan*

12:00 H-4-4
Growth Control of Carbon Nanotube for Electron Device Applications
M. Maeda[2,3], T. Kamimura[1,3], C. Hyon[3], A. Kojima[3] and K. Matsumoto[1,3], *[1]Osaka Univ., [2]Univ. of Tsukuba and [3]CREST-JST, Japan*

12:15 H-4-5
Fabrication of Peapod FETs Using Peapods Synthesized Directly on Si Substrate
Y. Kurokawa[1], Y. Ohno[1,2], T. Shimada[1], Y. Murakami[3], A. Sakai[1], M. Ishida[1], S. Kishimoto[1], T. Okazaki[1], S. Maruyama[3] and H. Shinohara[1,4,5], *[1]Nagoya Univ., [2]PRESTO-JST, [3]Tokyo Univ., [4]CREST-JST and [5]Institute for Advanced Research, Japan*

Room I (307)

11:45 I-4-3
Potentiometric Detection of Single Nucleotide Polymorphism Using Genetic Field Effect Transistor
T. Sakata and Y. Miyahara, *Biomaterials Center, National Institute for Materials Science, Japan*

12:00 I-4-4
Direct DNA detection using ion-sensitive field effect transistors (IS-FETs) based on peptide nucleic acid
T. Uno[1], T. Ohtake[1], H. Tabata[1,2] and T. Kawai[1,2], *[1]CREST- JST and [2]Osaka Univ., Japan*

Lunch

13:15-15:00 Poster Session (EXHIBITION HALL)

Room A (ZUIUN)

Area 2: Advanced Silicon Devices and Device Physics
A-5: Novel Device and Sensors
(15:15-16:30)
Chairs: N. Sugii (Hitachi)
H. Oda (Renesas)

15:15 A-5-1
Successful CMOS Operation of Dopant-Segregation Schottky Barrier Transistors (DS-SBTs)
A. Kinoshita[1], Y. Tsuchiya[1], A. Yagishita[2], K. Uchida[1] and J. Koga[1], *[1]Corporate R&D Center, Toshiba Corp. and [2]Semiconductor Company, Toshiba Corp., Japan*

15:35 A-5-2
Optimization of Low Power and High Speed DTM for Embedded RAM Applications
H. Tashiro, K. Tsunoda, A. Satoh, T. Nakanishi and H. Tanaka, *Fujitsu Labs. Ltd., Japan*

15:55 A-5-3
Realization of n-type and p-type Si-Microprobe Array Using *In-Situ* Doping with Selective Vapor-Liquid-Solid (VLS) Growth Method
M. S. Islam, H. Ishino, T. Kawano, H. Takao, K. Sawada and M. Ishida, *Toyohashi Univ. of Technology, Japan*

16:15 A-5-4
A New Well Capacity Adjusting Scheme for High Sensitivity, Extended Dynamic Range CMOS Imaging Pixel Sensors
C. H. Lai, Y. P. Yu and Y. C. King, *National Tsing-Hua Univ., Taiwan*

Room B (HEIAN)

Area 3: Silicon Process/Materials Technologies
B-5: Metal Gate Electrode
(15:15-16:35)
Chairs: H. Kitajima (SELETE)
K. Suguro (Toshiba)

15:15 B-5-1
Material Selection for the Metal Gate/High-k Transistors
Y. Akasaka[1], K. Miyagawa[1], A. Kariya[1], H. Shoji[1], T. Aoyama[1], S. Kume[1], M. Shigeta[1], O. Ogawa[1], K. Shiraishi[2, 3], A. Uedono[2, 3], K. Yamabe[2, 3], T. Chikyow[3], K. Nakajima[3], M. Yashuhira[1], K. Yamada[3, 4] and T. Arikado[1], *[1]SELETE, [2]Tsukuba Univ., [3]National Research Institute of Material Science and [4]Waseda Univ., Japan*

15:35 B-5-2
A Novel Dual-Metal Gate Integration Process for Sub-1nm EOT HfO$_2$ CMOS Devices
J. Kang[1, 2], C. Ren[2], H. Yu[2], X. Wang[2], M. F. Li[2], D. S. H. Chan[2], Y. C. Yeo[2], Y. Wang[1] and D. L. Kwong[3], *[1]Peking Univ., [2]National Univ. of Singapore and [3]Univ. of Texas, China*

15:55 B-5-3
Effect of Fluorine on Interface Characteristics in Low-temperature CMIS Process with HfO$_2$ Metal Gate Stacks
T. Sasaki, Y. Akasaka, K. Miyagawa, T. Hoshi, Y. Watanabe, F. Ootsuka, M. Yasuhira and T. Arikado, *SELETE, Japan*

16:15 B-5-4
Behavior of Effective Work Function in Metal/High-K Gate Stack under High Temperature Process
M. S. Joo[1], B. J. Cho[1], D. Z. Chi[2], N. Balasubramanian[3] and D. L. Kwong[4], *[1]National Univ. of Singapore, [2]Institute of Materials Research and Engineering, [3]Institute of Microelectronics and [4]Univ. of Texas, Singapore*

Room C (TOUGEN)

Area 4: Silicon-on-Insulator Technologies
C-5: SOI-Device Applications
(15:15-16:35)
Chairs: K. Inoh (Toshiba)
M. Terauchi (Hiroshima City Univ.)

15:15 C-5-1 (Invited)
SOI Floating Body Memories for Embedded Memory Applications
S. Okhonin, P. Fazan and M. Nagoga, *Innovative Silicon S.A., Switzerland*

15:45 C-5-2 (Invited)
Fully Depleted SOI Technology for Ultra Low Power Application
F. Ichikawa and S. Baba, *Oki Electric Industry Co,.Ltd., Japan*

16:15 C-5-3
A 90nm-node SOI Technology for RF Applications
T. Ikeda[1], Y. Hirano[1], T. Iwamatsu[1], D. Chen[2], T. Yoshimura[2], T. Ipposhi[1], S. Maegawa[1], M. Inuishi[1] and Y. Ohji[1], *[1]Renesas Technology Corp. and [2]Mitsubishi Electric Corp., Japan*

Room D (FUKUJU)

Area 6: Compound Semiconductor Materials and Devices
D-5: GaN Electronic Devices I
(15:15-16:30)
Chairs: H. Miyamoto (NEC)
T. Hashizume (Hokkaido Univ.)

15:15 D-5-1 (Invited)
Diamond MISFETs for high frequency applications
H. Umezawa, *Waseda Univ., Japan*

15:45 D-5-2
Source resistance reduction of AlGaN/GaN HFET using novel superlattice cap layer
T. Murata, A. Kanda, M. Hikita, Y. Hirose, Y. Uemoto, T. Tanaka, K. Inoue and D. Ueda, *Matsushita Electric Industrial Co. Ltd., Japan*

16:00 D-5-3
Multi channel AlGaN/GaN HEMTs for high breakdown voltage and low leakage current
S. C. Lee, J. C. Her, M. W. Ha, K. S. Seo and M. K. Han, *Seoul National Univ., Korea*

16:15 D-5-4
A Dual Gate AlGaN/GaN HEMT For High Voltage Switching Applications
M. W. Ha, S. C. Lee, J. C. Her, K. S. Seo and M. K. Han, *Seoul National Univ., Korea*

Room F (Training Room)

Area 7: Optoelectronic Devices and Photonic Crystal Devices
F-5: Photonic Crystal Fibers and Devices
(15:15-16:45)
Chairs: H. Yamada (NEC)
H. J. S. Dorren (Eindhoven Univ. of Technology)

15:15 F-5-1 (Invited)
Micro Structured Optical Fibers and Devices
M. Ogai[1], R. Bise[2] J. Fini[2] and D. J.Trevor[2], *[1]Furukawa Electric Co. and [2]OFS Labs., USA*

15:45 F-5-2 (Invited)
PBG Resonators and Waveguides in SOI Photonic Crystal Slabs
M. Notomi, A. Shinya, E. Kuramochi and S. Mitsugi, *NTT Corp., Japan*

16:15 F-5-3
A design of the photonic crystal directional coupler with a high extinction ratio and a short complete coupling length
N. Yamamoto, Y. Watababe and K. Komori, *AIST, Japan*

16:30 F-5-4
Photonic crystal thermo-optic switch
T. Chu[1], H. Yamada[1,2], S. Ishida[3] and Y. Arakawa[3], *[1]OITDA, [2]NEC Corp. and [3]Univ. of Tokyo, Japan*

Room G (401)

Room H (303)

Area 1: Advanced Silicon Circuits and Systems
H-5: Image Sensing and Processing
(15:15-16:35)
Chairs: M. Fujishima (Univ. of Tokyo)
M. Nagata (Kobe Univ.)

15:15 H-5-1
Retinal Prosthesis System with Telemetry Circuit Controlled by Human Eyelid Movement
J. Deguchi[1], T. Watanabe[1], K. Motonami[1], T. Sugimura[1], H. Tomita[2], J. Shim[1], H. Kurino[1], M. Tamai[3] and M. Koyanagi[1], *[1]Dep. of Bioengineering and Robotics, Tohoku Univ. [2]Biomedical Engineering Research Organization, Tohoku Univ. and [3]Graduate School of Medicine, Tohoku Univ., Japan*

15:35 H-5-2
A Flexible and Extendible Neural Stimulation Device with Distributed Multi-chip Architecture for Retinal Prosthesis
Y. Pan, T. Tokuda, A. Uehara, K. Kagawa, J. Ohta and M. Nunoshita, *Nara Institute of Science and Technology, Japan*

15:55 H-5-3
A High S/N Ratio Object Extraction CMOS Image Sensor with Column Parallel Signal Processing
T. Tate, S. Sugawa, K. Chiba, K. Kotani and T. Ohmi, *Tohoku Univ., Japan*

16:15 H-5-4
An Analog Edge-Filtering Processor Employing Only-Nearest-Neighbor Interconnects
Y. Nakashita, Y. Mita and T. Shibata, *Univ. of Tokyo, Japan*

Room I (307)

Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications
I-5: N/MEMS for Bio-and Chemical Applications II
(15:15-16:30)
Chairs: H. Tabata (Osaka Univ.)
T. Ichiki (Univ. of Tokyo)

15:15 I-5-1 (Invited)
New Method for Detection of Single DNA Molecules Si-based Nano-Scale Pore
T. Mitsui, *Harvard Univ., USA*

15:45 I-5-2
Selective deposition of gold nanoparticles on the oxide surface of Si nanowire
J. T. Sheu, C. C. Chen and P. C. Huang, *National Chi Nan Univ., Taiwan*

16:00 I-5-3
Fabrication of Microfluidic Channel Type Smart Electrochemical DNA Sensors with Operational Amplifiers
K. Sawada, C. Oda, H. Takao and M. Ishida, *Toyohashi Univ. of Technology, Japan*

16:15 I-5-4
Nanostructure Fabrication using PEG-based Polymers for Biomedical Applications
H. Otsuka[1], T. Satomi[1], A. Hirano[2], S. Suzuki[3], S. Enosawa[4], Y. Nagasaki[5], H. Kobayashi[1], J. Tanaka[1] and K. Kataoka[1,2], *[1]National Institute for Materials Science, [2]Univ. of Tokyo, [3]Human & Animal Bridging Research Organization, [4]National Research Institute for Child Health and Development and [5]Tokyo Univ. of Science, Japan*

Room A (ZUIUN)

Room B (HEIAN)

Area 3: Silicon Process/Materials Technologies
B-6: Advanced Process
(17:00-18:20)
Chairs: M. Hori (Nagoya Univ.)
T. Chikyo (NIMS)

17:00 B-6-1
Control of nitrogen profile in radical nitridation of SiO_2 films.
K. Kawase[1,3], H. Umeda[2], M. Inoue[2], S. Tsujikawa[2], Y. Akamatsu[2], A. Teramoto[4] and T. Ohmi[4], *[1]Mitsubishi Electric Corp., [2]Renesas Technology Corp., [3]Graduate School of Engineering, Tohoku Univ. and [4]New Industry Creation Hatchery Center, Tohoku Univ., Japan*

17:20 B-6-2
Effect of Kr Gas Dilution on O Atom Density in Surface Wave Excited Kr/O_2 Plasma for Low -Temperature and Damage-free Plasma Oxidation Processes
Y. Kubota, K. Yamakawa and M. Hori, *Nagoya Univ., Japan*

17:40 B-6-3
An Impurity-Enhanced Oxidation Assisted Doping Profile Evaluation for Three-Dimensional and Vertical-Channel Transistors
K. Kobayashi, T. Eto, K. Okuyama, K. Shibahara and H. Sunami, *Hiroshima Univ., Japan*

18:00 B-6-4
Suppression of Gate Depletion in p^+ Polysilicon Gated Sub-40nm PMOS Devices by Laser Thermal Process
T. Yamamoto[1], T. Kubo[1], K. Okabe[1], T. Sukegawa[1], Y. Wang[2], T. Lin[2], S. Talwar[2] and M. Kase[1], *[1]Fujitsu Ltd. and [2]Ultratech Inc., Japan*

Room C (TOUGEN)

Area 4: Silicon-on-Insulator Technologies
C-6: SOI-Device Characterization
(17:00-18:00)
Chairs: S. Okhonin (Innovative Silicon S.A)
Y. Kado (NTT)

17:00 C-6-1
Suppression of Self-Heating in Hybrid Trench Isolated SOI MOSFETs with Poly-Si plug and W plug
F. Komatsu[1], T. Iwamatsu[2], Y. Hirano[2], H. Takashino[2], T. Ipposhi[2], S. Maegawa[2], M. Inuishi[2] and Y. Ohji[2], *[1]Renesas Semiconductor Engineering and [2]Renesas Technology Corp., Japan*

17:20 C-6-2
Temperature Dependence of Off-Current in Bulk and FD SOI MOSFETs
K. Miyaji, M. Saitoh, T. Nagumo and T. Hiramoto, *Univ. of Tokyo, Japan*

17:40 C-6-3
Floating Body Accelerated Oxide Breakdown Progression in Ultra-Thin Oxide SOI pMOSFETs
C. T. Chan, C. H. Kuo, C. J. Tang, M. C. Chen and T. Wang, *National Chiao Tung Univ., Taiwan*

Room D (FUKUJU)

Area 6: Compound Semiconductor Materials and Devices
D-6: GaN Electronic Devices II
(17:00-18:00)
Chairs: K. Kojima (Mitsubishi Electric)
J. T. Hsu (OES/ITRI)

17:00 D-6-1
Gate Leakage Reduction Mechanism of AlGaN/GaN MIS-HFETs
D. Kikuta, R. Takaki, J. Matsuda, M. Okada, X. Wei, J. P. Ao and Y. Ohno, *Univ. of Tokushima, Japan*

17:15 D-6-2
Common - Emitter Current - Voltage Characteristics of Pnp AlGaN/GaN Heterojunction Bipolar Transistors
K. Kumakura[1], Y. Yamauchi[2] and T. Makimoto[1], *[1]NTT Corp. and [2]NEL TechnoSupport, Japan*

17:30 D-6-3
High Temperature and Low Frequency Noise of AlGaN/GaN/AlGaN Double Heterostructure MOS-HFETs with Photo-Chemical Vapor Deposition SiO_2 Oxide Layer
C. K. Wang[1], S. J. Chang[1], Y. K. Su[1], Y. Z. Chiou[2], C. H. Kuo[1], C. S. Chang[1], T. K. Lin[1], T. K. Ko[1] and J. J. Tang[2], *[1]National Cheng Kung Univ. and [2]Southern Taiwan Univ. of Technology, Taiwan*

17:45 D-6-4
Noise Analysis of AlGaN/GaN MOS-HFETs with Photochemical-Vapor Deposition SiO_2 Layer
Y. Z. Chiou[1], C. K. Wang[2], S. J. Chang[2], Y. K. Su[2], C. S. Chang[2], T. K. Lin[2], T. H. Fang[1] and J. J. Tang[1], *[1]Southern Taiwan Univ. of Technology and [2]National Cheng Kung Univ., Taiwan*

18:30-20:30 Rump Session (Room A, Room B)

Room F (Training Room)

Area 12: System-Level Integration and Packaging Technologies
F-6: System in Package
(17:00-18:15)
Chairs: M. Aoyagi (AIST)
H. Ezawa (Toshiba)

17:00 F-6-1 (Invited)
SIP drives a new business model of semiconductor
H. Kawamoto, *S&S Semicon Inc., Japan*

17:30 F-6-2
Transmission characteristics of Gaussian monocycle pulse for inter-chip wireless interconnection using integrated antenna
K. Kimoto and T. Kikkawa, *Hiroshima Univ., Japan*

17:45 F-6-3
Efficient Design of Integrated Antenna on Si for On-chip Wireless Interconnect
A. Rashid[1], M. Khan[2] and T. Kikkawa[3], *[1]Bangladesh Univ., [2]United International Univ. and [3]Hiroshima Univ., Bangladesh*

18:00 F-6-4
High-Speed Transmission Circuit for Micro Network on Si ULSI
S. Gomi, K. Nakamura, H. Ito, H. Sugita, K. Okada and K. Masu, *Tokyo Tech, Japan*

Room G (401)

Room H (303)

Area 1: Advanced Silicon Circuits and Systems
H-6: Memory Circuits
(17:00-18:00)
Chairs: Y. Kanno (Hitachi)
M. Fujishima (Univ. of Tokyo)

17:00 H-6-1
CMOS-process-based ultra high density Flash Memory Cell and Array Architecture
K. H. Lee, M. Y. Wu, S. H. Dai and Y. C. King, *National Tsing-Hua Univ., Taiwan*

17:20 H-6-2
Bank-Type Associative Memory for High-Speed Nearest Manhattan Distance Search in Large Reference-Pattern Space
T. Koide, Y. Yuji and H. J. Mattausch, *Hiroshima Univ., Japan*

17:40 H-6-3
Automatic Learning Based on Associative Memory and Short/Long term Storage Concept
Y. Shirakawa, M. Mizokami, T. Koide and H. J. Mattausch, *Hiroshima Univ., Japan*

Room I (307)

Area 14: Micro/Nano Electromechanical Devices for Bio- and Chemical Applications
I-6: N/MEMS for Bio-and Chemical Applications III
(17:00-18:00)
Chairs: M. Sasaki (Tohoku Univ.)
M. Sriyudthsak (Chulalongkorn Univ.)

17:00 I-6-1
Ultimate Functional Multi-Electrode System (UFMES) Based on Multi-Chip Bonding Technique
T. Watanabe, K. Motonami, K. Sakamoto, J. Deguchi, T. Fukushima, J. C. Shim, H. Mushiake, H. Kurino and M. Koyanagi, *Tohoku Univ., Japan*

17:15 I-6-2
A Silicon-Based Optical Thin-Film Biosensor Array for Real-time Measurement of Bio-molecular Interaction
T. Fujimura, K. Takenaka and Y. Goto, *Hitachi, Ltd., Japan*

17:30 I-6-3
A Pulse Modulation CMOS Image Sensor with 120dB Dynamic Range and $1nW/cm^2$ Resolution for Bioimaging Applications
D. Ng, H. Okamoto, T. Tokuda, K. Kagawa, J. Ohta and M. Nunoshita, *Nara Institute of Science and Technolgy, Japan*

17:45 I-6-4
Compact Triangulation Sensor Array Constructed by Folded Wafer
S. Endou, M. Sasaki and K. Hane, *Tohoku Univ., Japan*

18:30-20:30 Rump Session (Room A, Room B)

POSTER SESSION (13:15-15:00, Exhibition Hall)

P1
Advanced Silicon Circuits and Systems
(7 Papers)

P1-1
Low-Voltage-Signaling CMOS Receiver with Dynamic Threshold Control
K. Tsuda, Y. Arima and T. Asano, *Kyushu Institute of Technology, Japan*

P1-2
Mixed-Mode Circuit-Device simulation of ESD Protection Circuits with Feedback Triggering.
A. Shibkov and V. Axelrad, *Sequoia Design Systems Inc., USA*

P1-3
Efficient Analysis and Optimization of ESD Protection Circuits.
V. Axelrad[1], A. Balasinski[2], W. Baker[2] and A. Shibkov[1], *[1]Sequoia Design Systems Inc. and [2]Cypress Semiconductor, USA*

P1-4
A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter Chip Wireless Interconnection
P. K. Saha[1,2], N. Sasaki[1] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Bangladesh Univ. of Engineering and Technology, Japan*

P1-5
Chip Multiprocessor Based on Dual Instruction Multiple Data Architecture
M. Shimura and M. Fujishima, *Univ. of Tokyo, Japan*

P1-6
A Right-Brain/Left-Brain Integrated Associative Processor Employing Convertible MIMD Elements
H. Hayakawa, M. Ogawa and T. Shibata, *Univ. of Tokyo, Japan*

P1-7
Design of RFID Front-end Circuitry Enabling CDMA-based Collision Resistance
Y. Fukumizu, S. Ohno, M. Nagata and K. Taki, *Kobe Univ., Japan*

P2
Advanced Silicon Devices and Device Physics
(20 Papers)

P2-1
A Novel Explanation of Power-Law Model with Quantitative Hydrogen Mechanism for Ultra-Thin Oxide Breakdown
J. Shieh, *United Microelectronics Corp. (UMC), Taiwan*

P2-2
The Impact of Pad Test-Fixture for De-embedding on Radio-Frequency MOSFETs
L. C. Ming, *Institute of Microelectronics, National Cheng Kung Univ., Taiwan*

P2-3
Anomalous Behaviors of Random Telegraph Signals in Ultra-thin Gate Oxide MOSFETs
M. P. Lu and M. J. Chen, *National Chiao-Tung Univ., Taiwan*

P2-4
Understanding the Impact of Process Variations on Analog Circuit Performance with Halo Channel Doped Deep Sub-Micron CMOS Technologies
N. Kanike and R. Rao V, *Indian Institute of Technology, India*

P2-5
Improvements of Electrical Properties with Reduced Transient-Enhanced-Diffusion for 65nm-node CMOS Technology using Flash Lamp Annealing
A. Mineji, K. Yamashita, F. Ootsuka, M. Yasuhira and T. Arikado, *SELETE, Japan*

P2-6
Strain Dependence of Mobility Enhancement in Local Strain Channel nMOSFETs
T. S. Chao[1,2] and T. Y. Lu[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs., Taiwan*

P2-7
Effects of Gate Oxide Scaling and Gate Leakage Currents on Sample and Hold Circuits
M. Gupta and J. Woo, *UCLA, USA*

P2-8
Impact of Aggressively Shallow Source/Drain Extensions on the Device Performance
K. Kimoto[1], T. Tada[2] and T. Kanayama[2], *[1]MIRAI-ASET and [2]MIRAI-ASRC, AIST, Japan*

P2-9
Evaluations of Scaling Properties for GOI MOSFETs in Nano-Scale
G. Du, X. Liu, Z. Xia, Y. Wang, D. Hou, J. Kang and R. Han, *Institute of Microelectronics Peking Univ., China*

P2-10
Low frequency noise by mobility and number fluctuations in MOS structures
S. Hamayosi, T. Nakamoto, M. Wada and K. Higuchi, *Hiroshima Univ., Japan*

P2-11
Reduced Hot-Carrier Induced Degradation of NMOS I/O Transistors with Sub-micron Source-Drain Diffusion Length for 0.11 µm Dual Gate Oxide CMOS Technology
S. K. Seng[1, 2], L. W. Shing[1], L. Hong[2], L. J. Gon[2], Q. Elgin, K. Boone[2], T. K. Chok[2] and C. L. Hung[2], *[1]Nanyang Technological Univ. and [2]Chartered Semiconductor Manufacturing, Singapore*

P2-12
RTS amplitudes in decanano n-MOSFETs with conventional and high-k gate stacks
A. Lee, A. R. Brown, A. Asenov and S. Roy, *Univ. of Glasgow, UK*

P2-13
Interfacial Control in HfAlOx Gate Dielectric FETs with Improved Mobility for 65nm-node Low-Standby-Power Applications
H. Ohji, K. Torii, T. Kawahara, T. Maeda, H. Itoh, A. Mutoh, R. Mitsuhashi, A. Horiuchi, H. Kitajima, F. Ootsuka, M. Yasuhira and T. Arikado, *SELETE, Japan*

P2-14
Dependence of Analog and Digital Performances on Mechanical Film Stress of ILD Layer in Nano-Scale CMOSFETs.
S. H. Park[1], H. H. Ji[2], Y. G. Kim[2], H. D. Lee[2], H. S. Lee[1], Y. S. Kang[1], D. B. Kim[1] and J. W. Park[1], *[1]Hynix Semiconductor Inc. and [2]Chungnam National Univ., Korea*

P2-15
Damascene Gate CMOSFETs with 30 nm-Scale Gate Length
S. H. Kim, C. W. Oh and J. D. Choe, *Samsung Electronics Co. Ltd., Korea*

P2-16
Effectiveness of Optimum Body Bias for Leakage Reduction in High K CMOS Circuits
P. K. Chawda, A. Bulusu and R. Rao V, *Indian Institute of Technology, India*

P2-17
Monte Carlo simulation of nanoscale *n-i-n* diode: Influence of the hot-electron in drain region on ballistic transport
T. Kurusu and K. Natori, *Univ. of Tsukuba, Japan*

P2-18
Shot Noise Measurement in p-i-n Diode and Its Analysis
K. Hara, O. Matsushima, G. Suzuki, D. Navarro, K. Konno, Y. Isobe and M. Miura-Mattausch, *Hiroshima Univ., Japan*

P2-19
A Novel High Ruggedness Power MOSFET With a Planar Oxide Deep P+ Implant Structure
F. T. Chien[1], M. H. Lai[2], S. T. Su[2] and C. L. Cheng[2], *[1]Feng Chia Univ. and [2]Chino-Excel Technology Corp., Taiwan*

P2-20
Novel Nitrogen doped Ni SALICIDE Process for Nano-Scale CMOS Technology
S. Y. Oh[1], J. G. Yun[1], B. F. Huang[1], Y. J. Kim[1], H. H. Ji[1], U. S. Kim[2], H. S. Cha[2], S. B. Heo[2], J. G. Lee[2] and J. S. Wang[1], *[1]Chungnam National Univ. and [2]Hynix Semiconductor Inc., Korea*

P3
Silicon Process/Materials Technologies
(20 Papers)

P3-1
The development of TiN Bottom Electrodes Isolation Methods for the Fabrication of sub-micron DRAM Capacitor
Y. T. Cho, S. H. Cho, H. J. Lee, S. K. Kim, J. B. Park, J. M. Lee, B. H. Choi and J. W. Kim, *Hynix Semiconductor Inc., Korea*

P3-2
Effect of Post Thermal Processes on Nitride/W/WNx/poly-Si Gate Stack
H. J. Cho, S. A. Jang, Y. S. Kim, K. Y. Lim, J. G. Oh, J. H. Lee, T. S. Park, T. S. Back, J. M. Yang and H. S. Yang, *Hynix Semiconductor Inc., Korea*

P3-3
Electron Transport Model for Strained Silicon-Carbon Alloy
S. T. Chang[1] and C. Y. Lin[2], *[1]Chung Yuan Christian Univ. and [2]National Chung Hsing Univ., Taiwan*

P3-4
Control of UV Radiation Damages for the High Sensitive CCD Image Sensor
Y. Ishikawa[1], Y. Katoh[1], M. Okigawa[1,2] and S. Samukawa[1], *[1]Tohoku Univ. and [2]Sanyo Electric Company, Japan*

P3-5
First-Principles Calculation Software for Dielectric Response Study of High-k Materials
T. Hamada[1], T. Yamamoto[1], H. Momida[1], T. Uda[1,2] and T. Ohno[1,3], *[1]Univ. of Tokyo, [2]AdvanceSoft Corp. and [3]National Institute for Material Science, Japan*

P3-6
Workfunction Tuning Using Various Impurities for Fully Silicided NiSi Gate
K. Sano, M. Hino, N. Ooishi and K. Shibahara, *Hiroshima Univ., Japan*

P3-7
Investigation of CVD-Co Silicidation for the Improvement of Contact Resistance
H. S. Kim[1], J. H. Yun[1], K. J. Moon[1], W. H. Sohn[1], S. H. Cheong[1], S. W. Jung[1], G. H. Choi[1], S. H. Kim[2], N. J. Bae[2] and S. T. Kim[1], *[1]Samsung Electronics Co. Ltd. and [2]COMTECS, Korea*

P3-8
Improving Characteristics of Tantalum Oxide Thin Film Devices with Copper Electrodes
W. F. Wu[1], K. C. Tsai[2], C. P. Kuan[1], C. C. Wu[1] and C. C. Chao[1], *[1]National Nano Device Labs. and [2]National Chiao Tung Univ., Taiwan*

P3-9
Adsorption Behavior of Various Fluorocarbon Gases on the Silicon Wafer Surface
A. Hidaka[1], S. Yamashita[2], T. Kato[2], Y. Shirai[2] T. Ohmi[2], M. Kitano[2] and N. Tanahashi[2], *[1]Tohoku Univ. and [2]NICHe, Tohoku Univ., Japan*

P3-10
Work function control of Al-Ni alloy for metal gate application
T. Matsukawa, C. Yasumuro, H. Yamauchi, S. Kanemaru, M. Masahara, K. Endo, E. Suzuki and J. Itoh, *Nanoelectronics Research Institute, AIST, Japan*

P3-11
Poly-Si Comparable Fermi-Level Pinning of Fully Silicided Platinum Gates on HfO_2
M. Kadoshima[1], K. Akiyama[1], N. Mise[1], S. Migita[2], N. Yasuda[1], K. Iwamoto[1], H. Fujiwara[1], K. Tominaga[1], M. Ohno[1] and T. Nabatame[1], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo, Japan*

P3-12
Quantum Chemical Molecular Dynamics Simulation of Boron Diffusion and Si Implantation into Silicon Surface
T. Masuda[1], H. Tsuboi[2], M. Koyama[1], M. Kubo[1,3] and A. Miyamoto[1,2], *[1]Tohoku Univ., [2]NICHe, Tohoku Univ. and [3]JST-PRESTO, Japan*

P3-13
The mechanical properties of hydrophobic nanoporous silica low-k films investigated by utilizing X-ray reflectivity technology
C. W. Yen[1], A. T. Cho[1], H. Y. Hwang[1], F. M. Pan[3], J. Y. Chen[3] and K. J. Chaob[2], *[1]National Nano Device Labs., [2]National Tsinghua Univ. and [3]National Chiao Tung Univ., Taiwan*

P3-14
Theoretical Study of Chemical Mechanical Polishing of SiO_2 Surface
A. Rajendran[1], Y. Takahashi[1], H. Tshuboi[3], M. Koyama[1], M. Kudo[1,2] and A. Miyamoto[1,3], *[1]Tohoku Univ., [2]JST-PRESTO and [3]NICHe, Tohoku Univ., Japan*

P3-15
Optimization Technique of Number of Interconnect Layers and Circuit Area Based on Wire Length Distribution
T. Kyogoku, J. Inoue, H. Nakashima, K. Okada and K. Masu, *Tokyo Tech, Japan*

P3-16
Raised Source/Drain on Different Integration Schemes for Sub-micro CMOS
E. Cheng, Y. Y. Chiang and Y. C. Lee, *United Microelectronics Corp. (UMC), Taiwan*

P3-17
Depth Profile Prediction on Low Energy Boron Implantation Process by Tight-Binding Quantum Chemical Molecular Dynamics
H. Tsuboi[1], A. Sagawa[1], H. Iga[1], K. Sasata[1], M. Koyama[1], M. Kubo[1], H. Yabuhara[2] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]Toshiba corp., Japan*

P3-18
Design and fabrication of MOS device circuits with reticle-free exposure method
K. Wakasugi[1], S. Wakimoto[1], A. Nakada[1], I. Ohshima[1], H. Kubota[1] and K. Nakamura[2], *[1]Kumamoto Univ. and [2]Kumamoto Technology and Industry Foundation, Japan*

P3-19
Molecular Dynamics (MD) Calculation for Low-energy Ion Implantation Process with Dynamic Annealing Effect
O. Kwon, J. Seo, K. Kim and T. Won, *Inha Univ., Korea*

P3-20
Impact of Metal Gate/High-k Interface in Mo Metal Gated MOSFETs with HfO_2 Gate Dielectrics
T. Aoyama and Y. Nara, *Fujitsu Labs Ltd., Japan*

P4 Silicon-on-Insulator Technologies
(8 Papers)

P4-1
Lateral Graphoepitaxy of Germanium Controlled by Microholes on SiO_2 Surface
T. Numai, T. Koide, T. Minemoto, H. Takakura and Y. Hamakawa, *Ritsumeikan Univ., Japan*

P4-2
Width Effect on Hot-Carrier-induced Degradation for 90nm Partially Depleted SOI CMOSFET
C. M. Lai, *National Cheng Kung Univ., Taiwan*

P4-3
High-Performance Modified-Schottky-Barrier S/D p-Channel FinFETs
C. P. Lin[1] and B. Y. Tsui[1,2], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs., Taiwan*

P4-4
Nanoscale Strained Si/SiGe Heterojunction Tri-gate FETs
S. T. Chang[1] and S. H. Hwang[2], *[1]Chung Yuan Christian Univ. and [2]National Taiwan Univ., Taiwan*

P4-5
Novel properties of erbium-silicided *n*-type Schottky barrier MOSFETs
M. Jang, Y. Kim, J. Shin and S. Lee, *Electronics and Telecommunications Research Institute, Korea*

P4-6
Short Channel Characteristics of Variable Body Factor FD SOI MOSFETs
T. Ohtou, T. Nagumo and T. Hiramoto, *Univ. of Tokyo, Japan*

P4-7
A Selectable Logarithmic/Linear Response Active Pixel Sensor Cell with Reduced Fixed-Pattern-Noise Based on DTMOS Operation
M. Terauchi, A. Hamasaki and A. Suketa, *Hiroshima City Univ., Japan*

P4-8
Electrostatically Driven XY-stage Based on SOI-MEMS
F. Bouno, M. Sasaki and K. Hane, *Tohoku Univ., Japan*

P5 New Materials and Characterization for Silicon LSIs
(15 Papers)

P5-1
Mobility Enhancement of MOSFETs on p-Silicon (111) with In-situ HF-Vapor Pre-Gate Oxide Cleaning
T. S. Chao[1,2], Y. H. Lin[3] and W. L. Yang[3], *[1]National Chiao Tung Univ., [2]National Nano Device Labs and [3]Feng Chia Univ., Taiwan*

P5-2
Characterization of Pore Size Distributions in Ultralow-*k* Films
N. Hata[1, 2], N. Fujii[3], H. Miyoshi[3], X. Li[2] and T. Kikkawa[1, 4], *[1]MIRAI, AIST, [2]ASRC, AIST, [3]MIRAI-ASET, [4]Hiroshima Univ., Japan*

P5-3
Low-Temperature Formation of Poly-$Si_{1-x}Ge_x$ (x: 0-1) on SiO_2 by Au-Mediated Lateral Crystallization
H. Kanno, T. Aoki, A. Kenjo, T. Sadoh and M. Miyao, *Kyushu Univ., Japan*

P5-4
Transient charging and relaxation in high-k gate dielectrics and its implications
B. H. Lee[1], C. Young[1], R. Choi[1], J. H. Sim[1,2], G. Brown[1] and G. Bersuker[1], *[1]International SEMATECH and [2]Univ. of Texas, USA*

P5-5
Analysis of dislocations in strained-Si/SiGe devices by EBIC technique
Y. Anan[1], N. Sugii[1], Y. Kimura[1] and M. Nozoe[2], *[1]Central Research Lab., Hitachi Ltd. and [2]Hitachi High-Technologies Corp., Japan*

P5-6
Low Temperature Formation of Highly Thermal Immune Ni Germanosilicide Using NiPt Alloy with Co Over-layer in $Si_{1-x}Ge_x$ according to Different Ge Fractions (x)
J. G. Yun[1], S. Y. Oh[1], B. F. Huang[1], Y. J. Kim[1], H. H. Ji[1], Y. G. Kim[1], Y. C. Kim[2], S. H. Park[3], H. S. Lee[3], D. B. Kim[3], and H. D. Lee[1], *[1]Chungnam National Univ., [2]Korea Univ. of Technology and Education and [3]Hynix Semiconductor Incorp., Korea*

P5-7
Depth Profiling of $Si/Si_{1-x}Ge_x$ Structures by Micro-Raman Imaging
T. Mitani[1], S. Nakashima[1], H. Okumura[1] and A. Ogura[2], *[1]AIST and [2]Meiji Univ., Japan*

P5-8
Electrical Characterization of Strained Si/SiGe Wafers using Transient Capacitance Measurements
D. Wang[1], M. Ninomiya[2], M. Nakamae[2] and H. Nakashima[1], *[1]Kyushu Univ. and [2]Sumitomo Mitsubishi Silicon Corp., Japan*

P5-9
Thermal Stability and Electrical Properties of $(La_2O_3)_{1-x}(Al_2O_3)_x$ Composite Films
R. Fujitsuka, M. Sakashita, A. Sakai, S. Zaima and Y. Yasuda, *Nagoya Univ., Japan*

P5-10
Anomalous Behavior of Interface Traps of Si MOS Capacitors Contaminated with Organic Molecules
M. Suzuki and S. Yokoyama, *Hiroshima Univ. Japan*

P5-11
Precise Depth Profiling of Sub-keV Implanted Arsenic
T. Eto and K. Shibahara, *Hiroshima Univ., Japan*

P5-12
Post-deposition Annealing Effects on Interface States Generation in $HfO_2/SiO_2/Si$ MOS Capacitors
M. Sasagawa, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

P5-13
Contactless Characterization of Fixed Charge in HfO_2 Thin Film by Photoreflectance
M. Sohgawa[1], M. Yoshida[1], T. Naoyama[1], T. Tada[1], K. Ikeda[1], T. Kanashima[1], A. Fujimoto[2] and M. Okuyama[1], *[1]Osaka Univ. and [2]Wakayama National College of Technology, Japan*

P5-14
Effect of Hf metal predeposition on the electrical properties of HfO_2 films on tensile strained $Si_{0.9954}C_{0.0046}$ layers
Y. S. Liu[1], S. Maikap[2,3], P. S. Chen[3] and K. C. Liu[1], *[1]Chang Gung Univ., [2]NTU and [3]ERSO-ITRI, Taiwan*

P5-15
Influence of Thermal Annealing on Chemical Structure of Lanthanum oxide/Si Interfacial Transition Layer
H. Nohira[1], T. Yoshida[1], H. Okamoto[1], S. Shinagawa,[1] W. Sakai[2], K. Nakajima[2], M. Suzuki[2], K. Kimura[2], N. J. Aun[3] and Y. Kobayashi[3], *[1]Musashi Institute of Technology, [2]Kyoto Univ., [3]Frontier Collaborative Research Center, Tokyo Tech, [4]Tokyo Tech, [5]RIKEN/Spring-8 and [6]JASRI/Spring-8, Japan*

P6 Compound Semiconductor Materials and Devices
(4 Papers)

P6-1
Nitride-based light emitting diode and photodetector dual function
Devices with InGaN/GaN multiple quantum well structures
Y. T. Chou[1], C. H. Chen[2], S. J. Chang[1], Y. K. Su[1], P. C. Chang[3], P. C. Chen[3], H. Hung[1], S. M. Wang[1] and C. L. Yu[1], *[1]National Cheng Kung Univ., [2]Cheng Shiu Univ. and [3]Nan Jeon Institute of Technology, Taiwan*

P6-2
Characteristics of p-type InGaN grown by metalorganic chemical vapor deposition
K. S. Ryu[1], J. W. Ju[1], C. R. Lee[1], I. H. Lee[1], A. Fedorov[1], K. H. Park[2], Y. H. Lee[2] and J. W. Kim[3], *[1]Chonbuk National Univ., [2]Sysnex Co. and [3]Samsung Electro-Mechanics Co., Korea*

P6-3
Performance of AlGaN/GaN Heterostrucrure FETs Over Temperatures
C. C. Lee[1], C. F. Shih[1], C. P. Lee[1], C. R. Tu[2], C. C. Chuo[2] and J. Chi[2], *[1]National Chiao Tung Univ. and [2]Industrial Technology Research Institute, Taiwan*

P6-4
Characteristics of Pt/Schottky Diode s fabricated on the Cracked GaN Epitaxial Layer on (111) Silicon
S. J. Park[1], Y. W. Choi[1], H. B. Lee[1], W. L. Shan[2], S. J. Chua[2,3], J. H. Lee[1] and S. H. Hahm[1,3], *[1]Kyungpook National Univ., [2]Institute of Materials Research and Engineering and [3]National Univ. of Singapore, Korea*

P7 Optoelectronic Devices and Photonic Crystal Devices
(13 Papers)

P7-1
An Experimental Analysis of 1.55 μm Infrared Light Propagation in Integrated SOI Structure
M. Kawai[1], K. Endo[2], T. Tabei[1] and H. Sunami[1], *[1]Hiroshima Univ. and [2]Matsushita Semi-Conductor Engineering Corp., Japan*

P7-2
Theoretical study on the photonic crystal slabs with hexagonal optical atoms
L. Yang, J. Motohisa and T. Fukui, *Hokkaido Univ., Japan*

P7-3
Optical Polarization Properties of InAs/GaAs Quantum Dot Semiconductor Optical Amplifier
P. Jayavel[1], T. Kita[1], O. Wada[1], H. Ebe[2], M. Sugawara[2], J. Tatebayashi[2], Y. Arakawa[2], Y. Nakata[3] and T. Akiyama[3], *[1]Kobe Univ., [2]Univ. of Tokyo and [3]Fujitsu Labs. Ltd., Japan*

P7-4
Characteristics of back illumination type UV photodetector fabricated by $Al_xGa_{1-x}N$ heterostructure
K. S. Chae[1], D. W. Kim[1], H. S. Han[1], I. H. Lee[1], Y. J. Park[2] and C. R. Lee[1], *[1]Chonbuk National Univ. and [2]Samsung Advanced Institute of Technology (SAIT), Korea*

P7-5
Electron-Beam Lithography and Thermal Development to Fluorinated Polyarylate
M. Tomiki[1], N. Okamoto[1] and O. Sugihara[2], *[1]Shizuoka Univ. and [2]Tohoku Univ., Japan*

P7-6
Quantum Well Infrared Photodetector with pHEMT structure
J. H. Oum, U. H. Lee, Y. H. Kang, J. R. Yang and S. Hong, *Korea Advanced Institute of Science and Technology, Korea*

P7-7
Study of the Novel Polymer COC Waveguide Film
S. J. Hwang[1] and H. H. Yu[2], *[1]National United Univ. and [2]National Huwei Univ. of Science and Technology, Taiwan*

P7-8
Analysis of air waveguides in three-dimensional photonic crystal
Y. Watanabe[1], N. Yamamoto[1,2] and K. Komori[1], *[1]AIST and [2]CREST-JST, Japan*

P7-9
Depleted optical thyristor using vertical injection method for good isolation between input and output
W. K. Choi[1], D. G. Kim[1], Y. W. Choi[1], S. Lee[2], D. H. Woo[2] and S. H. Kim[2], *[1]Chung-Ang Univ. and [2]Korea Institute of Science and Technology, Korea*

P7-10
Semiconductor MMI Optical Isolator with Cladding of Ce:YIG
C. W. Son[1], S. J. Kim[1], J. W. Roh[1], J. H. Kim[1], T. Mizumoto[2], T. H. Yoon[3], Y. T. Byun[1], S. Lee[1], D.H. Woo[1] and S. H. Kim[1], *[1]Korea Institute of Science and Technology, [2]Tokyo Tech and [3]Pusan National Univ., Korea*

P7-11
Fabrication and Surface Plasmon Excitation in Thin Films of Fluorescent Microspheres with Polyvinyl alcohol
K. Shinbo, A. Ikarashi, M. Yamamoto, Y. Ohdaira, K. Kato and F. Kaneko, *Niigata Univ., Japan*

P7-12
Amorphous Silicon/Silicon-Carbide Separated Absorption and Multiplication Region Avalanche Photodiode with Additional Doped Superlattice
N. F. Shih[1], W. J. Chuang[2] and J. W. Hong[2], *[1]Hsiuping Institute of Technology and [2]National Central Univ., Taiwan*

P7-13
Improvement in GaN-based light-emitting diodes by surface texturization with natural lithography
R. H. Horng, C. C. Yang, C. E. Lee, D. S. Wuu, S. H. Huang and S. C. Hsu, *National Chung Hsing Univ., Taiwan*

P8 Novel Devices, Physics and Fabrication
(9 Papers)

P8-1
Silicon nanowires as a pH sensor
J. F. Hsu, B. R. Huang and H. L. Chen, *National Yunlin Univ., Taiwan*

P8-2
Change of Carbon Nanotube Structure by Ion Irradiation
M. Brzhezinskaya[1], E. Baitinger[1], V. Shnitov[2] and A. Smirnov[2], *[1]Chelyabinsk State Pedagogical Univ. and [2]Ioffe Physico-Technical Institute of the Russian Academy of Sciences, Russia*

P8-3
Nanoimprint Lithography Using Novolak Photoresist and Soft Mold at Room Temperature
T. Numai, T. Koide, T. Minemoto, H. Takakura and Y. Hamakawa, *Ritsumeikan Univ., Japan*

P8-4
Genetic Algorithm Approach to Functional Molecules for Nanoscale Devices
H. Mizuseki, N. Igarashi, R. V. Belosludov, A. A. Farajian and Y. Kawazoe, *Tohoku Univ., Japan*

P8-5
ADC and DAC Circuits Using Single Electron and MOS transistors
N. J. Wu, *Institute of Semiconductors, Chinese Academy of Sciences, China*

P8-6
Strain-Relief Mechanisms of Stepwise Ge composition Multilayer Buffers and High PVCR $Si/Si_{1-x}Ge_x$ ASDQW RTD Formed with Triple-Layer Buffer
H. Maekawa, Y. Sano and Y. Suda, *Tokyo Univ. of Agriculture and Technology, Japan*

P8-7
Magnetic and Electrical Properties of (La, Sr)MnO_3 Sputtered on $SrTiO_3$-buffered Si Substrate
T. Uemura, Y. Takagi, K. Sekine, K. Matsuda and M. Yamamoto, *Hokkaido Univ., Japan*

P8-8
Fabrication of Au Nano-ring Arrays Using Anodic Aluminum Oxide Film as RF-sputtering Mask
K. H. Jung[1], J. W. Yoon[1, 2], N. Koshizaki[2] and Y. S. Kwon[1], *[1]Dong-A Univ. and [2]National Institute of Advanced Industrial Science and Technology, Korea*

P8-9
Fabrication and Characterization of Lateral Field Emission Device Based On Carbon Nanotubes
C. P. Juan[1], *[1]National Chiao Tung Univ., [2]Institute of Atomic and Molecular Sciences, Academia Sinica, and [3]National Taiwan Univ., Taiwan*

P9
Quantum Nanostructure Devices and Physics
(12 Papers)

P9-1
Long Spin Relaxation Time Observed in a Lateral Quantum Dot
S. Sasaki[1], T. Fujisawa[1,2], T. Hayashi[1] and Y. Hirayama[1,3], *[1]NTT Basic Research Labs., [2]Tokyo Tech and [3]SORST-JST, Japan*

P9-2
Observation of bonding states in single pair of coupled quantum dots using micro-spectroscopy
K. Goshima[1,2], K. Komori[1,2], S. Yamauchi[1,2], I. Morohashi[1,2], A. Shikanai[1,2] and T. Sugaya[1,2], *[1]AIST and [2]CREST-JST, Japan*

P9-3
Transition Energies in Vertically Coupled Multilayer Nanoscale InAs/GaAs Semiconductor Quantum Dots with Different Structure Shapes
Y. Li, *National Chiao Tung Univ., Taiwan*

P9-4
Control of Self-Formed GaAs Nanoholes Combined with InAs Quantum Dots
T. Satoh and K. Yamaguchi, *Univ. of Electro-Communications, Japan*

P9-5
Characterization of GaInP/GaAs triple barrier resonant tunneling diodes fabricated by fast atom beam etching process
M. Fukumitsu, H. Horie, N. Asaoka, M. Suhara and T. Okumura, *Tokyo Metropolitan Univ., Japan*

P9-6
InGaN/GaN MQD P-N Junction Photodiodes
S. C. Hung[1] and L.W. Ji[2], *[1]National Cheng Kung Univ., [2]Kao Yuan Institute of Technology and [3]National Huwei Univ. of Science and Technology, Taiwan*

P9-7
Optical properties from amorphous GaN films deposited by a pulsed-laser ablation at room temperature
J. W. Yoon[1, 2], N. Koshizaki[3] and Y. S. Kwon[1, 2], *[1]Dept. of Electrical Engineering, Dong-A Univ. [2]CIIPMS, Dong-A Univ. and [3]AIST, Korea*

P9-8
Observation of large spectral blue-shift in photoluminescence spectra of Mg-doped gallium nitride Nanorods
Y. H. Chang, H. C. Hsueh, F. I. Lai, W. Y. Chang, C. C. Yu, W. H. Huang, C. F. Lin, H. C. Kuo and S. C. Wang, *Institute of Electro-Optical Engineering, National Chiao Tung Univ., Taiwan*

P9-9
Two-Dimensional Quantum Mechanical Modeling of Strained-Si FinFETs on SiGe-On-Insulator(SGOI)
I. S. Park, K. Kim and T. Won, *Inha Univ., Korea*

P9-10
Mode-coupling effects in NEGF device simulation
H. Takeda and N. Mori, *Osaka Univ., Japan*

P9-11
Electroluminescence Enhancement Assisted with Ballistic Electron Excitation in Nanocrystalline Silicon Diodes
B. Gelloz[1], T. Uchida[1], M. Niibe[1], A. Kojima[2] and N. Koshida[1], *[1]Tokyo Univ. of Agriculture and Technology and [2]Quantum 14 Co., Japan*

P9-12
Continuous-Wave and Time-Resolved Photoluminescence Analysis of Silicon Nanocrystals Formed by Thermal Annealing of Amorphous Silicon Oxides at Different Times
C. J. Lin[1], Y.L. Chueh[2], L. J. Chou[2], C. W. Chang[3], E. W. G. Diau[3], H. C. Kao[1] and G. R. Lin[1], *[1]Institute of Electro-Optical Engineering, National Chiao Tung Univ., [2]National Tsing Hua Univ. and [3]Dept. of Applied Chemistry, National Chiao Tung Univ., Taiwan*

P10
Non-Volatile Memory Technologies
(8 Papers)

P10-1
MFIS-structure Memory Device with High Quality Ferroelectric $Sr_2(Ta_{1-x}Nbx)_2O_7$ Formed by Physical Vapor Deposition and Oxygen Radical Treatment by Radical Oxygen Assisted Layer by Layer(ROALL) deposition
H. Sakurai, I. Takahashi, T. Isogai, K. Funaiwa, T. Tsunoda, T. Goto, M. Hirayama, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

P10-2
An Advanced HSPICE™ Macro-Model for Magnetic-Tunnel-Junction
H. Shin[1], S. Lee[1], S. Lee[1] and D. Kim[2], *[1]Ewha Womans Univ. and [2]Kookmin Univ., Korea*

P10-3
Reduction of the threshold voltage fluctuation in an electrical phase change memory device with a $Ge_1Sb_2Te_4$/TiN cell structure
D. H. Kang[1], T. G. Kim[1], H. J. Jung[1], T. S. Lee[1], I. H. Kim[1], K. S. Lee[1], W. M. Kim[1], B. K. Cheong[1], D. H. Ahn[2] M. H. Kwon[2], H. S. Kwon[2] and K. B. Kim[2], *[1]Korea Institute of Science and Technology and [2]Seoul National Univ., Korea*

P10-4
Indium selenide based phase change memory
H. Lee[1] and D. H. Kang[2], *[1]Korea Univ. and [2]Korea Institute of Science and Technology, Korea*

P10-5
Superior SONOS Flash Memory with Tapered-Bandgap Nitride Layer
K. H. Wu[1], T. S. Chen[1], C. H. Kao[1], H. C. Chien[1], T. K. Tsai[1], J. W. Chang[1], C. C. Chan[1], C. H. Chien[2], K. H. Lee[3] and Y. C. King[3], *[1]Chung-Cheng Institute of Technology, National Defense Univ., [2]National Nano Device Labs. and [3]National Tsing-Hua Univ., Taiwan*

P10-6
Distribution and Impact of Local Trapped Charges in SONOS Memory
L. Sun, L. Pan, Y. Zeng, H. Pang, J. Wang, Z. Zhang, X. Li and J. Zhu, *Tsinghua Univ., China*

P10-7
High Pressure H_2/D_2 Annealed SONOS Nonvolatile Memory Devices
S. Choi[1], M. Jang[1], H. Park[1], S. Jeon[2], J. Kim[2], C. Kim[2] and H. Hwang[1], *[1]Gwangju Institute of Science and Technology and [2]Samsung Advanced Institute of Technology (SAIT), Korea*

P10-8
Low Voltage and High Speed Efficient Flash Using Band-to-Band Tunneling Induced Substrate Hot Electron Injection (BBISHE) to Perform Programming
M. Y. Wu[1], K. H. Lee[1], S. H. Dai[1], S. F. Hu[2] and Y. C. King[1], *[1]National Tsing-Hua Univ. and [2]National Nano Device Labs., Taiwan*

P11
SiGe/III-V/III-N Devices and Circuits for Wireless and Optical Communications
(5 Papers)

P11-1
Comparison of AlGaN/GaN insulated gate heterostructure field-effect transistors with ultra-thin Al_2O_3/Si_3N_4 bilayer and with Si_3N_4 single layer
C. Wang[1], N. Maeda[1], M. Hiroki[1], T. Tawara[2], T. Saitoh[2], T. Makimoto[2], T. Kobayashi[1] and T. Enoki[1], *[1]NTT Photonics Labs. and [2]NTT Basic Research Labs., Japan*

P11-2
The low-k BCB passivation layer on the GaN HEMTs
W. K. Wang, C. H. Lin, P. C. Lin, C. K. Lin, F. H. Huang, Y. J. Chan, G. T. Chen and J. I. Chyi, *Taiwan National Central Univ., Taiwan*

P11-3
A new CML-type RTD/HBT Non-inverted/Inverted MOnostable-BIstable transition Logic Element(MOBILE) IC
T. Kim, S. Choi, B. Lee and K. Yang, *Korea Advanced Institute of Science and Technology, Korea*

P11-4
Pulsed IVT Characteristics of AlGaN/GaN HEMT on the Isothermal Conditions
J. C. Her[1], K. M. Lee[1], S. C. Lee[1], M. K. Han[1], J. E. Oh[2] and K. S. Seo[1], *[1]Seoul National Univ. and [2]Hanyang Univ., Korea*

P11-5
Large Conductance Modulation in Interdigital Gate HEMT Device due to Surface Plasma Wave Interactions and Its Device Application
A. M. Hashim, M. Takeuchi, S. Kasai, T. Hashizume and H. Hasegawa, *Hokkaido Univ., Japan*

P12
System-Level Integration and Packaging Technologies
(1 Papers)

P12-1
Ferromagnetic RF Integrated Spiral Inductor with Closed Magnetic Circuit
S. Bae[1], K. Kim[1], M. Yamaguchi[1], K. Tan[2], T. Kusumi[2] and K. Yamakawa[2], *[1]Tohoku Univ. and [2]Akita Institute of Technology, Japan*

P13
Organic Semiconductor Devices and Materials
(10 Papers)

P13-1
Improved performance of DB-PPV based Polymer Light Emitting Diodes by Thermal Annealing
M. L. Tu[1], Y. K. Su[1], T. H. Fang[2], W. H. Chen[1] and H. L. Yang[3], *[1]National Cheng Kung Univ., [2]Southern Taiwan Univ. of Technology and [3]Toppoly Optoelectronics Corp. Company, Taiwan*

P13-2
Interface Modification in Organic Thin Film Transistors
B. T. Wu, Y. K. Su, A. C. Wang, M. L. Tu and Y. S. Chen, *National Cheng Kung Univ., Taiwan*

P13-3
Preparation and Characterization of a Novel Flexible Substrate for OLED
H. H. Yu[1] and S. J. Hwang[2], *[1]National Huwei Univ. of Science and Technology and [2]National United Univ., Taiwan*

P13-4
Theoretical characterization of ground and low lying excited state of poly(3,4-ethylenedioxythiophene) and poly(4-styrenesulfonate)
A. Govindasamy[1], L. Chen[1], X. Wang[1], H. Ookawa[1], H. Tsuboi[2], M. Koyama[1], M. Kubo[1,3] and A. Miyamoto[1,2], *[1]Graduate School of Engineering, Tohoku Univ., [2]Tohoku Univ.,[3]Toshiba Corp., [4]NICHe, Tohoku Univ., and [5]JST-PRESTO, Japan*

P13-5
Top-Absorption Organic Photodiodes Suitable for Device Integration
H. Shimada[1], S. Naka[1,2], H. Okada[1,2] and H. Onnagawa[1,2], *[1]Toyama Univ. and [2]Innovation Plaza Tokai, JST, Japan*

P13-6
Amplified spontaneous emission under optical pumping from an organic semiconductor laser structure equipped with transparent carrier injection electrodes
H. Yamamoto[1], T. Oyamada[1,2], H. Sasabe[1,2] and C. Adachi[1,2], *[1]Chitose Institute of Science and Technology and [2]JST, Japan*

P13-7
Separately Doped Structures for Red Organic Light Emitting Diodes
C. Y. Yang[1], Y. S. Tsai[1], F. S. Juang[1], M. Y. Lin[1], D. Lin[2], C. H. Chu[3] and Y. T. Chiu[3], *[1]National Huwei Univ. of Science and Technology, [2]WindellCorp. and [3]Industrial Technology Research Institute, Taiwan*

P13-8
Effects of Doped-Zone Location on the CIE Value of Flexible White Organic Light Emitting Diodes
M. Y. Lin[1], F. S. Juang[1], Y. S. Tsai[1], C. Y. Yang[1], W. T. Wang[2] and C. Y. Shen[2], *[1]National Huwei Univ. of Science and Technology and [2]Industrial Technology Research Institute, Taiwan*

P13-9
Electrical Conduction Properties of Pentacene Thin Film
G. J. Kim and C. K.Song, *Dong-A Univ., Korea*

P13-10
The Analysis of Correlation between Pentacene TFTs and OLEDs
G. S. Ryu, K. S. Pyo and C. K.Song, *Donga-A Univ., Korea*

P14
Micro/Nano Electromechanical Device for Bio- and Chemical Applications
(5 Papers)

P14-1
Quasi-Static Capacitance-Voltage Measurement for DNA Hybridization Using Integrated Field Effect Devices
T. Sakata and Y. Miyahara, *Biomaterials Center, NIMS, Japan*

P14-2
Study on the Biosensor Using Surface Acoustic Wave sensor
C. U. Hong[1], G. B. Kim[1], W. S. Cheong[2], S. H. Kim[2], T. K. Kwon[1] and N. G. Kim[1], *[1]College of Engineering, Chonbuk National Univ. and [2]Graduate School, Chonbuk National Univ., Korea*

P14-3
Nano-Gap Device for Liquid Sensing
S. Morita, T. Takegawa, T. Hirokane, S. Urabe, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ., Japan*

P14-4
Potential Behavior of Bio-Chemically Modified Electrode for Extended Gate Field Effect Transistor
T. Sakata[1], S. Matsumoto[2], Y. Nakajima[2] and Y. Miyahara[1], *[1]Biomaterials Center, National Institute for Materials Science and [2]Ryokusei M.E.S Co., Ltd, Japan*

P14-5
Microreactor Array Chips for High-throughput Function Analysis of Biomolecules Using Magnetic Beads
Y. Hosoi[1], H. Aizawa[2], N. Nemoto[3] and T. Ichiki[1,4], *[1]Univ. of Tokyo, [2]Saitama Small Enterprise Promotion Corp., [3]National Institute of Advanced Industry Science and Technology and [4]PRESTO-JST, Japan*

Friday, September 17

Room A (ZUIUN)

Area 2: Advanced Silicon Devices and Device Physics

A-7: Advanced Gate Stack and DRAM
(9:15-10:35)
Chairs: K. Takeuchi (NEC)
Y. Momiyama (Fujitsu)

9:15 A-7-1
Investigation of Degradation model for Ultra-thin Gate Dielectrics
H. Mori[1], H. Ehara[1], N. Tamura[2], C. Kaneta[2], H. Matsuyama[1] and K. Shono[1], *[1]Fujitsu Ltd. and [2]Fujitsu Labs. Ltd., Japan*

9:35 A-7-2
Thermal Stability of Metal Gate Work Functions
H. Y. Yu[1], C. Ren[1], J. F. Kang[1, 3], Y. C. Yeo[1], D. S. Chan[1], M. F. Li[1,2] and D. L. Kwong[4], *[1]National Univ. of Singapore, [2]Institute of Microelectronics, [3]Peking Univ., China and [4]Univ. of Texas, Singapore*

9:55 A-7-3
Robust TiN/AHO/HSG-Cylinder Capacitor for High Density DRAMs
S. G. Kim, C. S. Hyun, D. Park, H. J. Moon, H. C. Kim, S. J. Kim, T. H. Cho, H. J. Kang, S. M. Jeong and S. W. Lee, K.Y. Lee, K. S. Oh, W. S. Lee, *Samsung Electronics Co., Ltd., Korea*

Room B (HEIAN)

Area 3: Silicon Process/Materials Technologies

B-7: High-K Gate Dielectric II
(9:15-10:15)
Chairs: Y. Tsunashima (Toshiba)

9:15 B-7-1
Effects of Base Oxide and Silicon Composition on Charge Trapping in HfSiO/SiO_2 High-k Gate Stacks
W. H. Wu[1], M. C. Chen[1], M. F. Wang[2], T. H. Hou[2], L. G. Yao[2], Y. Jin[2], S. C. Chen[2] and M. S. Liang[2], *[1]National Chiao Tung Univ. and [2]Taiwan Semiconductor Manufacturing Corp., Taiwan*

9:35 B-7-2
Hysteresis Phenomenon Improvements of HfO_2 by CF_4 Plasma Treatment
C. S. Lai[1], W. C. Wu[1], K. M. Fan[1], J. C. Wang[2] and S. J. Lin[2], *[1]Chang Gung Univ. and [2]Nanya Technology Corp., Taiwan*

9:55 B-7-3
Effects of post-deposition anneal on the electrical properties in HfSiO films grown by atomic layer deposition
H. J. Cho, H. R. Lee, H. B. Park, T. S. Jeon, S. G. Park, B. J. Jin, S. B. Kang, Y. G. Shin, U. I. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*

Room C (TOUGEN)

Area 4: Silicon-on-Insulator Technologies

C-7: SOI-Strained Technology
(9:15-10:35)
Chairs: O. Faynot (LETI)
T. Iwamatsu (Renesas)

9:15 C-7-1 (Invited)
SOI Transistor/Power Scaling and Scaling-Strengthened Strain
F. L. Yang, H.Y.Chen and C.Y.Chang, *Taiwan Semiconductor Manufacturing Company, Taiwan*

9:45 C-7-2 (Invited)
Development of SGOI and SSOI for High Volume Manufacturing
C. Mazure, I. Cayrefourcq, M. Kennard, F. Metral and B. Ghyselen, *SOITEC, France*

10:15 C-7-3
Study of Mobility in Strained Silicon and Germanium Ultra Thin Body MOSFETs
T. Low[1,3], C. Shen[1], M. F. Li[1,2], Y. C. Yeo[1], Y. T. Hou[1,2], C. X. Zhu[1], A. Chin[4], L. Chan[3] and D. L. Kwong[5], *[1]National Univ. of Singapore, [2]Institute of Microelectronics, [3]Chartered Semiconductor Manufacturing, [4]National Chiao Tung Univ. and [5]Univ. of Texas, Singapore*

Room D (FUKUJU)

Area 6: Compound Semiconductor Materials and Devices

D-7: GaN-Optical Devices
(9:15-10:30)
Chairs: M. Ikeda (Sony)
K. Kojima (Mitsubishi Electric)

9:15 D-7-1
Surface texturing for wafer-bonded GaN/mirror/Si light-emitting diodes
S. H. Huang[1], W. Y. Lin[1], D. S. Wuu[1], T. Y. Chen[2] and R. H. Horng[1], *[1]National Chung Hsing Univ. and [2]Advanced Epitaxy Technology Inc., Taiwan*

9:30 D-7-2
High Power GaN-Based LEDs with Transparent Indium-Zinc-Oxide Films
S. L. Chen[1], S. J. Wang[1], K. M. Uang[1,2], C. Wu[1] and T. M. Chen[2], *[1]National Cheng Kung Univ. and [2]Wu-Feng Institute of Technology, Taiwan*

9:45 D-7-3
Nitride based Power Chip with ITO p-Contact and Al back-side Reflector
C. S. Chang[1], S. J. Chang[1], Y. K. Su[1], W. S. Chen[1], C. F. Shen[1], S. C. Shei[2] and H. M. Lo[2], *[1]National Cheng Kung Univ. and [2]South Epitaxy Corp., Taiwan*

Room E (Small Hall)

Room F (Training Room)

Area 13: Organic Semiconductor Devices and Materials

F-7: Molecular Electronics
(9:15-10:30)
Chairs: M. Iwamoto (Tokyo Tech)
H. Tada (Okazaki National Research Inst.)

9:15 F-7-1 (Invited)
Development of Conducting Polymers towards Molecular Electronics
Y. W. Park[1], J. Park[1], K. Kim[2], J. I. Jin[2], S. Webster[3], R. Czerw[3] and D. L. Carroll[3], *[1]Seoul National Univ., [2]Korea Univ. and [3]Wake Forest Univ., Korea*

9:45 F-7-2
Electronic and Transport Properties of Molecular Wires: Theoretical Aspects for Realization of Nanoscale Interconnection
R. Belosludov, A. Farajian, Y. Kikuchi, H. Mizuseki and Y. Kawazoe, *Tohoku Univ., Japan*

10:00 F-7-3
Electrical Properties of Self-Assembled Monolayers Using STM
N. S. Lee, H. K. Shin and Y. S. Kwon, *Dong-A Univ., Korea*

Room G (401)

Area 9: Quantum Nanostructure Devices and Physics

G-7: Fabrication and Characterization
(9:15-10:30)
Chairs: R. Noetzel (Eindhoven Univ. of Technol.)
R. Knobel (Queens Univ.)

9:15 G-7-1 (Invited)
Monolithic, Defect-Free III-V on Si using Self-Assembled AlSb Quantum Dot Nucleation
D. L. Huffaker, G. Balakrishnan, S. Huang, L. R. Dawson, Y. C. Xin and P. Conlin, *Univ. of New Mexico, USA*

9:45 G-7-2
Cross-Sectional Evolution and Its Mechanism during Selective MBE Growth of GaAs Quantum Wires on (111)B Substrates
I. Tamai, T. Sato and H. Hasegawa, *Hokkaido Univ., Japan*

10:00 G-7-3
InGaN/GaN Multi-Quantum-Well Nanorods Fabricated by Plasma Etching Using Self-assembled Nickel Nano-masks
T. H. Hsueh, H. W. Huang, C. C. Kao, Y. H. Chang, O. Y. Miaochia, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ., Taiwan*

Room H (303)

Area 7: Optoelectronic Devices and Photonic Crystal Devices

H-7: Quantum Effect Photonic Devices
(9:15-10:30)
Chairs: H. Riechert (Infineon Technologies)
N. Suzuki (Toshiba)

9:15 H-7-1 (Invited)
High-Power Broadband Amplification and High-Speed Optical-Signal Processing by Quantum-Dot Semiconductor Optical Amplifiers
M. Sugawara[1], H. Ebe[1], N. Hatori[1], T. Akiyama[2, 3], M. Ekawa[2, 3], K. Kawaguchi[2, 3], H. Sudo[2, 3], A. Kuramata[2, 3] and Y. Arakawa[1], *[1]Univ. of Tokyo, [2]Fujitsu Ltd. and Fujitsu Labs. Ltd. and [3]Optoelectronic Industry and Technology Development Association (OITDA), Japan*

9:45 H-7-2
InAs Quantum Cascade Lasers Based on Coupled Quantum Well Structures
K. Ohtani, K. Fujita and H. Ohno, *Tohoku Univ., Japan*

10:00 H-7-3
InGaAs/AlGaAs quantum wire distributed feedback buried hetero-structure laser diode by one time selective metalorganic chemical vapor deposition on ridge substrate
Y. Takasuka[1,2], K. Yonei[2], H. Yamauchi[1] and M. Ogura[1], *[1]AIST and [2]Shibaura Institute of Technology, Japan*

Room A (ZUIUN)

Room B (HEIAN)

Room C (TOUGEN)

Room D (FUKUJU)

10:00 D-7-4
Fabrication of large-area GaN Vertical Light Emitting Diodes on Copper Substrates by Laser Lift-off
F. I. Lai[1], J. T. Chu[1], C. F. Chu[2], W. D. Liang[1], H. C. Kuo[1] and S. C. Wang[1], *[1]National Chiao Tung Univ. and [2]Highlink Corp., Taiwan*

10:15 D-7-5
High brightness InGaN/GaN blue LED realized by a 2” x 6 MOCVD system
J. W. Ju[1], K. S. Ryu[1], A. Fedorov[1], C. R. Lee[1], I. H. Lee[1], K. H. Park[2] and Y. H. Lee[2], *[1]Chonbuk National Univ. and [2]Sysnex Co., Korea*

Break

Area 2: Advanced Silicon Devices and Device Physics

A-8: Advanced Devices II
(10:45-12:05)
Chairs: N. Sugii (Hitachi)
K. Kurimoto (Matsushita Electric)

10:45 A-8-1 (Invited)
Ge and SiGe for High Performance MOSFETs and Integrated Optical Interconnects
K. C. Saraswat[1], C. O. Chui[1], T. Krishnamohan[1], A. K. Okyay[1], H. Kim[2] and P. McIntyre[2], *[1]Dept. of Electrical Eng. Stanford Univ., and [2]Dept. of Materials Science and Eng., Stanford Univ., USA*

11:15 A-8-2
A Novel STI Process from the View Point of Total Strain Process Design for 45nm Node Devices and Beyond
M. Ishibashi, K. Horita, M. Sawada, M. Kitazawa, M. Igarashi, T. Kuroi, T. Eimori, K. Kobayashi, M. Inuishi and Y. Ohji, *Renesas Technology Corp., Japan*

Area 3: Silicon Process/Materials Technologies

B-8: High-K Gate Dielectric III
(10:45-12:25)
Chairs: K. Eguchi (Toshiba)
K. Torii (SELETE)

10:45 B-8-1
High Performance fully silicided NiSi:Hf gate on $LaAlO_3$/GOI n-MOSFET with Little Fermi-level Pinning
D. S. Yu[1], C. F. Cheng[1], A. Chin[1], C. Zhu[2], M. F. Li[2] and D. L.Kwong[3], *[1]National Chiao Tung Univ., Univ. System of Taiwan, [2]National Univ. of Singapore and [3]Univ. of Texas, Taiwan*

11:05 B-8-2
Effects of high pressure hydrogen and deuterium annealing on nMOSFET with Hf-base gate dielectrics
H. Park[1], B. Lee[2], M. Gardner[2] and H. Hwang[1], *[1]Gwangju Institute of Science and Technology and [2]International SEMATECH, Korea*

Area 4: Silicon-on-Insulator Technologies

C-8: SOI-Materials
(10:45-12:05)
Chairs: C. Mazure (SOITEC)
T. Nakai (Sumitomo Mitsubishi Silicon)

10:45 C-8-1
New Strained SOI Fabricated By Laser Annealing Technology
Y. Mishima, H. Ochimizu and A. Mimura, *Fujitsu Labs. Ltd., Japan*

11:05 C-8-2
Improvement of Oxidation-Induced Ge Condensation Method by H^+ Implantation and Two-Step Annealing for Highly Stress-Relaxed SGOI
T. Sadoh[1], R. Matsuura[1], M. Ninomiya[2], M. Nakamae[2], T. Enokida[3], H. Hagino[3] and M. Miyao[1], *[1]Kyushu Univ., [2]SUMCO and [3]Fukuryo Semicon Engineering, Japan*

Area 6: Compound Semiconductor Materials and Devices

D-8: GaN-Crystal Growth
(10:45-12:15)
Chairs: T. Hashizume (Hokkaido Univ.)
T. Takahashi (Fujitsu Labs. Ltd.)

10:45 D-8-1
Low-dislocation AlGaN thin films grown using $Al_{1-x}Si_xN$ nano-disks (x= 0.07~0.17)
T. Akasaka, Y. Taniyasu, M. Kasu and T. Makimoto, *NTT Basic Research Labs., Japan*

11:00 D-8-2
Characteristic comparison of GaN epitaxy grown on patterned and unpatterned Si(111)
K. J. Kim, I. S. Seo and C. R. Lee, *Chonbuk National Univ., Korea*

Room E (Small Hall)

Room F (Training Room)

10:15 F-7-4
Electrical Properties of Tetrakis(alkylthio)tetrathiafulvalene Thin Film
M. Sakai, S. Maeda, M. Iizuka, M. Nakamura and K. Kudo, *Chiba Univ., Japan*

Room G (401)

10:15 G-7-4
Study of charge quantization in individual silicon quantum dots using Kelvin Probe Force Microscopy
M. Salem, Y. Tsuchiya, K. Usami, H. Mizuta and S. Oda, *Tokyo Tech, Japan*

Room H (303)

10:15 H-7-4
Observation of Light Emission at ~1.5 μm from InAs Quantum Dots in Photonic Crystal Microcavity
S. Iwamoto, J. Tatebayashi, T. Fukuda, T. Nakaoka, S. Ishida and Y. Arakawa, *Univ. of Tokyo, Japan*

Break

Area 13: Organic Semiconductor Devices and Materials

F-8: Organic Electronics
(10:45-12:15)
Chairs: K. Kato (Niigata Univ.)
A. Sugimura (Osaka Sangyo Univ.)

10:45 F-8-1
Solid State Solar Cells of Polythiophene-Porphyrin Composite Films
T. Akiyama[1], M. Matsushita[1], K. Kakutani[1], S. Yamada[1], K. Takechi[2], T. Shiga[2], T. Motohiro[2], H. Nakayama[3] and K. Kohama[3], *[1]Kyushu Univ., [2]Toyota Central R&D Labs., Inc. and [3]Toyota Motor Corp., Japan*

11:00 F-8-2
Effect of ligand carboxylation on adsorption and photosensitization in Ru(II) complex dye-sensitized nanocrystalline TiO_2 solar cell
T. Ishihara, T. Sano, N. Kobayashi, Q. Shen and T. Toyoda, *Univ. of Electro-Communications, Japan*

Area 9: Quantum Nanostructure Devices and Physics

G-8: Quantum Devices and Circuits
(10:45-12:15)
Chairs: P.V. Santos (Paul-Drude-Inst)
J. Motohisa (Hokkaido Univ.)

10:45 G-8-1 (Invited)
Rapid prototyping of quantum circuits using erasable electrostatic lithography
C. G. Smith, *Cambridge Univ., UK*

11:15 G-8-2
Resistance Oscillations by Electron-Nuclear Spin Coupling in Microscopic Quantum Hall Devices
G. Yusa[1], K. Hashimoto[2], K. Muraki[1], T. Saku[3] and Y. Hirayama[1,2], *[1]NTT Basic Research Labs., [2]SORST JST and [3]NTT Advanced Technology, Japan*

Area 7: Optoelectronic Devices and Photonic Crystal Devices

H-8: All-Optical Signal Processing
(10:45-12:15)
Chairs: S. Arahira (Oki Electric)
T. Mizumoto (Tokyo Tech)

10:45 H-8-1 (Invited)
All-optical Signal Processing Based on Ultrafast Nonlinearities in Semiconductor Optical Amplifiers
H.J.S. Dorren, X.Yang, E.Tangdiongga, S.Zhang, Z.Li, M.T.Hill, H.Ju, A.Mishra, Y.Liu, R.Geldenhuys, D.Lenstra and G.D.Khoe, *Eindhoven Univ. of Technology, Netherlands*

11:15 H-8-2 (Invited)
All-Optical Devices for Nx160Gb/s DWDM/OTDM Transmission Systems - Application to 8x160Gb/s-140km Unrepeatered Transmission
A. Suzuki, *FESTA Labs., Japan*

Room A (ZUIUN)

11:35 A-8-3
Theoretical Investigation of Electrical Performance and Band Structure of P-MOSFETs with $Si_{1-x}Ge_x$ Source/Drain Stressors
K. W. Ang[1], Y. T. Hou[2], J. Singh[2], M. F. Li[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Institute of Microelectronics, Singapore*

11:55 A-8-4
In-Plane Anisotropy of MOS Inversion Layer Mobility on Silicon (100), (110) and (111) surfaces
H. Irie, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

Room B (HEIAN)

11:25 B-8-3
Top-Surface Aluminized and Nitrided Hafnium Oxide Using Synthesis of Thin AlN and HfO_2 Stacked Layer
C. S. Park[1], B. J. Cho[1], L. J. Tang[2], W. Wang[3] and D. L. Kwong[4], *[1]The National Univ. of Singapore, [2]Institute of Microelectronics, [3]Institute of Materials Research Engineering and [4]Univ. of Texas, Singapore*

11:45 B-8-4
Cubic-HfN Formation in Hf-based High-k Gate Dielectrics with N-Incorp. and Its Impact on Electrical Properties of Films
M. Koyama, Y. Kamimuta, M. Koike, T. Ino and A. Nishiyama, *Toshiba Corp., Japan*

12:05 B-8-5
High Quality Hf-Silicate Gate Dielectrics Fabrication by Atomic Layer Deposition (ALD) Technology
S. Kamiyama, T. Miura, T. Aoyama, H. Kitajima and T. Arikado, *SELETE, Inc., Japan*

Room C (TOUGEN)

11:25 C-8-3
Development of Simulation Method for Buried Oxide Formation of SIMOX Structure During Post-Implantation Thermal Annealing
M. Nakao[1], K. Sudoh[2], H. Iikawa[1], H. Iwasaki[2] and K. Izumi[1], *[1]Osaka Pref. Univ. and [2]Osaka Univ., Japan*

Room D (FUKUJU)

11:15 D-8-3
Growth of AlGaN/GaN Quantum Wire Structures by RF-Radical Assisted Selective MBE on Pre-Patterned Substrates
T. Sato, T. Oikawa, T. Hashizume and H. Hasegawa, *Hokkaido Univ., Japan*

11:30 D-8-4
Growth of Perfect Crack-Free GaN/Si(111) Epitaxy Using CBL and Superlattice
D. W. Kim[1], I. S. Seo[1], K. J. Kim[1], K. S. Chae[1], I. W. Lee[1], Y. J. Park[2] and C. R. Lee[1], *[1]Chonbuk National Univ. and [2]Samsung Advanced Institute of Technology (SAIT), Korea*

11:45 D-8-5
Improvement of GaN Crystal Quality in RF-MBE Using Thin Low-Temperature-Grown GaN Buffer Layers
M. Shimizu[1], Y. Hirata[2], G. Piao[1] and H. Okumura[1], *[1]AIST and [2]Meiji Univ., Japan*

Lunch

Area 2: Advanced Silicon Devices and Device Physics

A-9: Nanoscale Device Physics
(13:45-15:05)
Chairs: M. Ogawa (Kobe Univ.)
K. Kurimoto (Matsushita Electric)

13:45 A-9-1 (Invited)
Nanoscale Device Simulation at the Scaling Limit and Beyond
G. Klimeck[1], A. Rahman[1], N. Vagidov[2], T. B. Boykin[3] and M. Lundstrom[1], *[1]Purdue Univ., [2]State Univ. of New York and [3]Univ. of Alabama, USA*

Area 3: Silicon Process/Materials Technologies

B-9: DRAM
(13:45-15:05)
Chairs: T. Kobayashi (Sony)
I. Asano (Elpida)

13:45 B-9-1
A Novel Cell Structure with Bit Line Cap Spacer (BCS) and Top Enlarged Storage Node Contact (TESC) for 90 nm DRAM Technology and Beyond
C. J. Yun, Y. K. Park, J. W. Lee, D. L. Bae, S. B. Kim, S. H. Shin, J. G. Lee, S. H. Lee, D. J. Lee and E. C. Lee, *Samsung Electronics Co. Ltd., Korea*

Area 5: New Materials and Characterization for Silicon LSIs

C-9: Gate Dielectrics Characterization II
(13:45-15:05)
Chairs: S. Miyazaki (Hiroshima Univ.)
S. Takagi (Univ. of Tokyo)

13:45 C-9-1
Difference between O_2 and N_2 Annealing Effects on CVD-SiO_2 Film Quality Studied by the Time-Dependent OCP Measurement
K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

Area 6: Compound Semiconductor Materials and Devices

D-9: Fe-Si
(13:45-15:15)
Chairs: N. Kobayashi (Univ. of Electro-Communications)
K. Ohtani (Tohoku Univ.)

13:45 D-9-1 (Invited)
Fabrication of p-Si/β-$FeSi_2$/n-Si Double-Heterostructure Light-Emitting Diode by Molecular Beam Epitaxy
M. Takauji, C. Li, T. Suemasu, and F. Hasegawa, *Univ. of Tsukuba, Japan*

Room E (Small Hall)

Room F (Training Room)

11:15 F-8-3
Photocurrent properties of *cis*–di (thiocyanato)–bis (4,4’–dicarboxy–2,2’ –bipyridine) ruthenium(II) monolayers on the gold surfaces
N. Terasaki[1], S. Nitahara[2], T. Akiyama[2] and S. Yamada[2], *[1]AIST and [2]Kyushu Univ., Japan*

11:30 F-8-4
Structure and Properties of Aluminum Phtalocyanine Chloride Thin Films Due to Vapor Treatments
K. Kato, T. Ito, Y. Saito, Y. Ohdaira, K. Shinbo and F. Kaneko, *Niigata Univ., Japan*

12:00 F-8-6
Vapor Deposition Polymerization of Polyimide Having Perylene Unit and its Characterization by Displacement Current Measurement
H. Usui, K. Hibi, M. Watanabe and K. Tanaka, *Tokyo Univ. of Agriculture and Technology, Japan*

Room G (401)

11:30 G-8-3
Room Temperature Operation of an Exclusive-OR Circuit Using a Highly-Doped Si Single-Electron Transistor
T. Kitade, K. Ohkura and A. Nakajima, *Hiroshima Univ., Japan*

11:45 G-8-4 (Invited)
Integrated Nanoscale Mechanics and Electronics
R. G. Knobel[1] and A.N. Cleland[2], *[1]Queen’s Univ. Canada and [2]Univ. of California, Santa Barbara, USA*

Room H (303)

11:45 H-8-3
Semiconductor asymmetrically coupled waveguides for tunable dispersion compensation
Y. Lee, A. Takei, T. Taniguchi and H. Uchiyama, *Hitachi, Ltd., Japan*

12:00 H-8-4
Simulation of Ultrafast Intersubband Optical Modulation Achieved in GaN/AlN Ridge Waveguide
N. Suzuki, N. Iizuka and K. Kaneko, *Toshiba Corp., Japan*

Lunch

Area 13: Organic Semiconductor Devices and Materials

F-9: Organic FET I
(13:45-15:15)
Chairs: K. Kudo (Chiba Univ.)
T. Someya (Univ. of Tokyo)

13:45 F-9-1
Investigation of the electrostatic phenomena at pentacene/metal interface; Electrical and optical approach for the study of FET operation
T. Manaka, Y. Suzue and M. Iwamoto, *Tokyo Tech, Japan*

Area 9: Quantum Nanostructure Devices and Physics

G-9: Control of Quantum State
(13:45-15:15)
Chairs: W.T. Masselink (Humbolt Univ.)
C.G. Smith (Cambridge Univ.)

13:45 G-9-1 (Invited)
Quantum Information Devices Based on Semiconductor Quantum Dots
T. Fujisawa, *NTT Corp., Japan*

Area 7: Optoelectronic Devices and Photonic Crystal Devices

H-9: Semiconductor Lasers
(13:45-15:15)
Chairs: S. Matsuo (NTT Photonics Labs.)
H. Shimizu (ATR International)

13:45 H-9-1 (Invited)
InGaAsN as a Material for Novel Long-Wavelength Lasers
H. Riechart, R. Averbeck, M. Galluppi, L. Geelhaar and G. Jaschke, *Infineon Technologies, Germany*

Room A (ZUIUN)

14:15 A-9-2
Nanoscale Quasi-Ballistic MOSFETs in Reflection-Transmission Model
K. Natori and T. Kurusu, *Univ. of Tsukuba, Japan*

14:35 A-9-3
Quantitative Understanding of Mobility Degradation in High Effective Electric Field Region in MOSFETs with Ultra-thin Gate Oxides
T. Ishihara[1], J. Koga[1] and S. Takagi[2], *[1]Toshiba Corp. and [2]Univ. of Tokyo, Japan*

14:55 A-9-4
Determination of tunnel mass and thickness of gate oxide including poly-Si/SiO_2 and Si/SiO_2 interfacial transition layers
H. Watanabe, D. Matsushita and K. Muraoka, *Toshiba Corp., Japan*

Room B (HEIAN)

14:05 B-9-2
Improvement of Contact Resistance of Ru electrode/TiN barrier at Ru/Crystalline-Ta_2O_5/Ru Capacitor for 50nm DRAM device
H. J. Lim, S. J. Chung, K. Lee, J. Lee, J. Y. Kim, C. Y. Yoo, S. T. Kim, U. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*

14:25 B-9-3
A 500°C fabrication process for MIM capacitors–based on a Ta_2O_5/Nb_2O_5 bilayer with high permittivity–for DRAM and SoC applications
Y. Matsui[1], M. Hiratani[1] and I. Asano[2], *[1]Hitachi, Ltd. and [2]Elpida Memory, Inc., Japan*

14:45 B-9-4
A New Divided Deposition Method of TiN Thin Films for MIM Capacitor Applications
S. Sakashita, T. Hayashi, T. Okudaira, K. Wakao, J. Tsuchimoto, K. Mori, K. Kobayashi and M. Yoneda, *Renesas Technology Corp., Japan*

Room C (TOUGEN)

14:05 C-9-2
Stable Observation of the Evolution of Leakage Spots in HfO_2/SiO_2 stacked structures by UHV-C-AFM
K. Kyuno, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*

14:25 C-9-3
Far Infrared Study of Structural Distortion and Transformation of HfO_2 by Introducing a Slight Amount of Si
K. Tomida, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

14:45 C-9-4
Evaluation of Electronic Defect States at Poly-Si/HfO_2 interface by Photoelectron Yield Spectroscopy
M. Sugimura, A. Ohta, H. Nakagawa, T. Shibaguchi, S. Higashi and S. Miyazaki, *Hiroshima Univ., Japan*

Room D (FUKUJU)

14:15 D-9-2
Growth and Characterization of Si-Based Light-Emitting Diode with β-$FeSi_2$-Particles/Si Multilayered Active Region by Molecular Beam Epitaxy
T. Sunohara, C. Li, Y. Ozawa, T. Suemasu and F. Hasegawa, *Univ. of Tsukuba, Japan*

14:30 D-9-3
Crystal Growth and Photoresponse of Al-doped β-$FeSi_2$/Si Heterojunctions
Y. Maeda[1], Y. Terai[2] and M. Itakura[3], *[1]Kyoto Univ., [2]Osaka Pref. Univ. and [3]Kyushu Univ., Japan*

14:45 D-9-4
Epitaxial Growth of β-$FeSi_2$ on Single Crystal Insulator
K. Akiyama[1], S. Kaneko[1] and H. Funakubo[2], *[1]Kanagawa Industrial Technology Research Institute and [2]Tokyo Tech, Japan*

15:00 D-9-5
Photoluminescence Enhancement in β-$FeSi_2$ by Annealing in Oxygen
Y. Terai[1] and Y. Maeda[2], *[1]Osaka Pref. Univ. and [2]Kyoto Univ., Japan*

Break

Room E (Small Hall)

Room F (Training Room)

14:00 F-9-2
Surface Spectroscopy of Organic FETs for the Estimation of Effective Mass of Organic Semiconductors
T. Shimada, *Univ. of Tokyo, Japan*

14:15 F-9-3
Pentacene TFTs Fabricated by High-aspect Ratio Metal Shadow Mask
S. H. Jin, S. M. Yi, K. D. Jung, C. B. Park, C. N. Chu, H. C. Shin, B. G. Park and J. D. Lee, *Seoul National Univ., Korea*

14:30 F-9-4
Complex Impedance Analysis and Photo-induced Effects of Semiconducting Pentacene Films
T. Nishimura, T. Yamada, T. Yokoyama, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

14:45 F-9-5
Grain Size Dependence of Field-Effect Mobility in Pentacene-Based Thin-Film Transistors
C. O. Tang, M. Kitamura and Y. Arakawa, *Univ. of Tokyo, Japan*

15:00 F-9-6
Pentacene TFTs using PVP as Gate Insulator
H. S. Byun, Y. X. Xu and C. K.Song, *Dong-A Univ., Korea*

Room G (401)

14:15 G-9-2
Long-range spin transport by acoustic fields in GaAs quantum wells
F. Iikawa[1,2], Y. Guang[1], R. Hey[1] and P. Santos[1], *[1]Paul-Drude-Institute and [2]Univ. of Campinas, Germany*

14:30 G-9-3
Electric-Field-Controllable Spin Interferometer Based on the Rashba Spin-Orbit Interaction
Y. Sekine[1], T. Koga[2,3] and J. Nitta[1,2], *[1]NTT Corp., [2]Japan Science and Technology, [3]Hokkaido Univ. and [4]CREST, Japan*

14:45 G-9-4
Carrier correlations in single pair of coupled quantum dots
S. Yamauchi[1,2], K. Komori[1,2], T. Sugaya[1,2], I. Morohashi[1,2] and K. Goshima[1,2], *[1]AIST and [2]CREST-JST, Japan*

15:00 G-9-5
Carrier Transport in Artificial Lattice of Self-Organized Gold Nano-Particles
S. Saito, T. Arai, H. Fukuda, D. Hisamoto, S. Kimura, T. Onai and R. Tsuchiya, *Hitachi, Ltd., Japan*

Room H (303)

14:15 H-9-2
Fabrication of High Speed Single Mode 1.27 µm InGaAs:Sb-GaAsP Quantum Wells Vertical Cavity Surface Emitting Laser
Y. H. Chang, H. C. Kuo, F. I. Lai, Y. A. Chang, P. T. Lee, S. C. Wang and L. H. Laih, *National Chiao Tung Univ., Taiwan*

14:30 H-9-3
Highly strained oxide confined InGaAs VCSELs emitting in the 1.3 µm regions
H. C. Yu[1], S. J. Chang[1], Y. K. Su[1], I. L. Chen[1], T. D. Lee[2], C. M. Lu[2], C. H. Chiou[2], Z. H. Lee[2], J. M. Wang[2] and C.P. Sung[2], *[1]National Cheng Kung Univ. and [2]Industrial Technology Research Institute, Taiwan*

14:45 H-9-4
GaInAs/InP Superlattice DBR for Long-Wavelength VCSELs
S. Ishida, T. Miyamoto and F. Koyama, *Tokyo Tech, Japan*

15:00 H-9-5
Dual Wavelength High Power Laser Diodes Fabricated by Selective Fluidic Self-Assembly Technique
T. Tojo[1], K. Yamanaka[1], B. P. Singh[1], K. Onozawa[1], D. Ueda[1], I. Soga[2], K. Maezawa[2] and T. Mizutani[2], *[1]Matsushita Electric Industrial Co. Ltd. and [2]Nagoya Univ., Japan*

Break

Room A (ZUIUN)

Area 2: Advanced Silicon Devices and Device Physics

A-10: Analog Devices and Compact Modeling
(15:30-16:50)
Chairs: H. Oda (Renesas)
K. Takeuchi (NEC)

15:30 A-10-1
Halo and LDD Engineering for Multiple V_T High Performance Analog Devices in 0.13μm CMOS Technology
J. C. Guo[1], W. Y. Lien[2], C. C. Liur[2] and C. M. Wu[2], *[1]National Chiao-Tung Univ. and [2]Taiwan Semiconductor Manufacturing Corp., Taiwan*

15:50 A-10-2
A Large-Signal MOSFET Model Based on Transient Carrier Response for RF Circuits
K. Watanabe[1], K. Kotani[1], A. Teramoto[2], S. Shigetoshi[1] and T. Ohmi[2], *[1]Graduate School of Engineering, Tohoku Univ. and [2]NICHe, Tohoku Univ., Japan*

16:10 A-10-3
A Quantum Mechanical Corrected SPICE Model for Ultrathin Oxide MOSFETs' Gate Tunneling Current Simulation
Y. Li[1,2], S. M. Yu[2] and J. W. Lee[1], *[1]National Nano Device Labs. and [2]National Chiao Tung Univ., Taiwan*

Room B (HEIAN)

Area 4: Silicon-on-Insulator Technologies

B-10: SOI-3D Structure
(15:30-16:50)
Chairs: A. Ogura (Meiji Univ.)
H. Matsuhashi (Oki Electric)

15:30 B-10-1
Scaling of Multiple-Gate Fully Depleted SOI transistors
O. Faynot[1], G. Barna[2], R. Ritzenthaler[1] and P. Gidon[1], *[1]CEA-LETI and [2]Texas Instruments, France*

15:50 B-10-2
Device design consideration for four-terminal double-gate MOSFET (4T-DGFET)
M. Masahara, Y. Liu, K. Sakamoto, K. Endo, T. Sekigawa, T. Matsukawa and E. Suzuki, *AIST, Japan*

16:10 B-10-3
Planar Double Gate CMOS transistors with 40nm metal gate for multipurpose applications
M. Vinet[1], T. Poiroux[1], J. Widiez[2], J. Lolivier[1], B. Previtali[1], C. Vizioz[1], B. Guillaumot[2], P. Besson[2], J. Simon[1] and F. Martin[1], *[1]CEA/DRT-LETI, [2]STMicroelectronics and [3]IMEP (UMR CNRS/INPG/UJF), France*

16:30 B-10-4
A Vertical SOI CMOS Technology with p-MOS on Si Film and n-MOS on Bulk Base
S. Zhang[1], X. Lin[2], R. Han[1], X. Wu[2] and M. Chan[2], *[1]Peking Univ. and [2]The Hong Kong Univ. of Science and Technology, China*

Room C (TOUGEN)

Area 5: New Materials and Characterization for Silicon LSIs

C-10: High-K Dielectrics
(15:30-16:30)
Chairs: Y. Awano (Fujitsu)
H. Watanabe (Osaka Univ.)

15:30 C-10-1
Dielectric Constant Increase of Yttrium-Doped HfO_2 by Structural Phase Modification
K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

15:50 C-10-2
Generalized Model of Oxidation Mechanism at HfO_2/Si Interface with Post-Deposition Annealing
H. Shimizu, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

16:10 C-10-3
Theoretical Analysis of Interstitial Boron Diffusion and Its Suppression Mechanism with Nitrogen in Amorphous HfO_2
M. Ikeda[1], G. Kresse[2], T. Nabatame[1] and A. Toriumi[3,4], *[1]MIRAI-ASET, [2]Univ. of Vienna, [3]MIRAI-ASRC and [4]Univ. of Tokyo, Japan*

Room D (FUKUJU)

Area 6: Compound Semiconductor Materials and Devices

D-10: Wide-Gap Materials
(15:30-16:45)
Chairs: K. Horikoshi (Waseda Univ.)
M. Ikeda (Sony)

15:30 D-10-1
High-temperature characteristics of strain in $Al_xGa_{1-x}N$/GaN heterostructures
D. Chen, B. Shen, K. Zhang, X. Wu, J. Xu, H. Zhao, R. Zhang and Y. Zheng, *Nanjing Univ., China*

15:45 D-10-2
The novel method to improve electrical characteristics of *p*-type GaN by using Ni catalysis
B. Huang[1], S. Wang[1], C. Chen[2], S. Chang[3], Y. Su[3], H. Hung[3] and Y. Chou[3], *[1]National Yunlin Univ. of Science and Technology, [2]Cheng Shiu Univ. and [3]National Cheng Kung Univ., Taiwan*

16:00 D-10-3
Effect of hydrogen irradiation during growth on molecular beam epitaxy of ZnO
M. Sano[1], K. Miyamoto[1], H. Kato[1] and T. Yao[2], *[1]Stanley Electric Co.,Ltd. and [2]Tohoku Univ., Japan*

16:15 D-10-4
Preparation and Characterization of ZnO and (Zn,Mg)O films doped with Al
H. Ryoken[1,2], I. Sakaguchi[1], T. Ohgaki[1], Y. Adachi[1], N. Ohashi[1], T. Takenaka[3] and H. Haneda[1,2], *[1]National Institute for Materials Science, [2]Kyushu Univ. and [3]Tokyo Univ. of Science, Japan*

16:30 D-10-5
Domain configuration in $Sn_2P_2S_6$ ferroelectrics-semiconductors
D. Kaynts, A. Grabar, A. Horvat, M. Gurzan and I. Stoika, *Uzhgorod Univ., Ukraine*

Room E (Small Hall)

Room F (Training Room)

Area 13: Organic Semiconductor Devices and Materials

F-10: Organic FET II
(15:30-16:15)
Chairs: T. Kamata (AIST)
T. Shimada (Univ. of Tokyo)

15:30 F-10-1
Array of Pentacene TFT's for Flexible AMOLED
C. K. Song and G. S. Ryu, *Dong-A Univ., Korea*

16:00 F-10-3
Bending and recovery tests of organic field-effect transistors
T. Sekitani, S. Iba, Y. Kato, H. Shinaoka and T. Someya, *Univ. of Tokyo, Japan*

Room G (401)

Area 9: Quantum Nanostructure Devices and Physics

G-10: Quantum Dots
(15:30-16:45)
Chairs: D.L. Huffaker (Univ. of New Mexico)
Y. Ohno (Tohoku Univ.)

15:30 G-10-1 (Invited)
Light-emitting diodes based on InP quantum dots in GaP
W.T. Masselink, *Humboldt Univ., Germany*

16:00 G-10-2
Single Electron Transistor Using Single Self-Assembled InAs Quantum Dots
M. Jung[1], D. Nakamura[1], K. Hirakawa[1], S. Ishida[2], Y. Arakawa[1,2], Y. Kawaguchi[3] and S. Komiyama[3], *[1]Institute of Industrial Science, [2]Reserch Center for Advanced Science and Technology and [3]Dept. of Basic Science, Univ. of Tokyo, Japan*

16:15 G-10-3
Continuous Wavelength Tuning of InAs/InP Quantum Dots in the 1.55 Micrometer Region by Inserting Ultra-thin GaAs and GaP Interlayers
R. Nötzel, Q. Gong and J. H. Wolter, *COBRA Inter-Univ. Research Institute, Eindhoven Univ. of Technology, Netherlands*

16:30 G-10-4
Precise Thermal Characterization of Confined Nanocrystalline Silicon By a 3ω Method
T. Kihara[1], T. Harada[1] and N. Koshida[2], *[1]Yamatake Corp. and [2]Tokyo Univ. of Agriculture and Technology, Japan*

Room H (303)

Area 7: Optoelectronic Devices and Photonic Crystal Devices

H-10: Optical Filters and Detectors
(15:30-16:45)
Chairs: T. Nishimura (Mitsubishi Electric)
S. Lee (Korea Inst. of Science and Technol.)

15:30 H-10-1
Novel Tunable Ladder-Type Filter for Widely Tunable Laser Diodes
S. Jeong, S. Matsuo, Y. Yoshikuni, T. Segawa, Y. Ohiso and H. Suzuki, *NTT Corp., Japan*

15:45 H-10-2
Race-Track Optical Ring Resonators with Groove Coupling
Y. Tanushi, M. Wake and S. Yokoyama, *Hiroshima Univ., Japan*

16:00 H-10-3
Integration of a HEMT and a MSM PD Using an InGaAsP (λ=1.3 μm) Buffer
J. H. Cha, J. Kim, C. Y. Kim, S. H. Shin and Y. S. Kwon, *Korea Advanced Institute of Science and Technology, Korea*

16:15 H-10-4
Reduced Mesa-Sidewall Leakage Current in InGaAs/InP MSM Photodetector by BCB Sidewall Process
W. Y. Chiu, F. H. Huang, Y. S. Wu, D. M. Lin, S. H. Chen, J. W. Shi, J. I. Chyi and Y. J. Chan, *Taiwan National Central Univ., Taiwan*

16:30 H-10-5
Carrier Transport Model for Lateral *p-i-n* Photodiodes at High-Frequency Operation
K. Konno, O. Matsushima, K. Hara, G. Suzuki, D. Navarro and M. Miura. Mattausch, *Hiroshima Univ., Japan*

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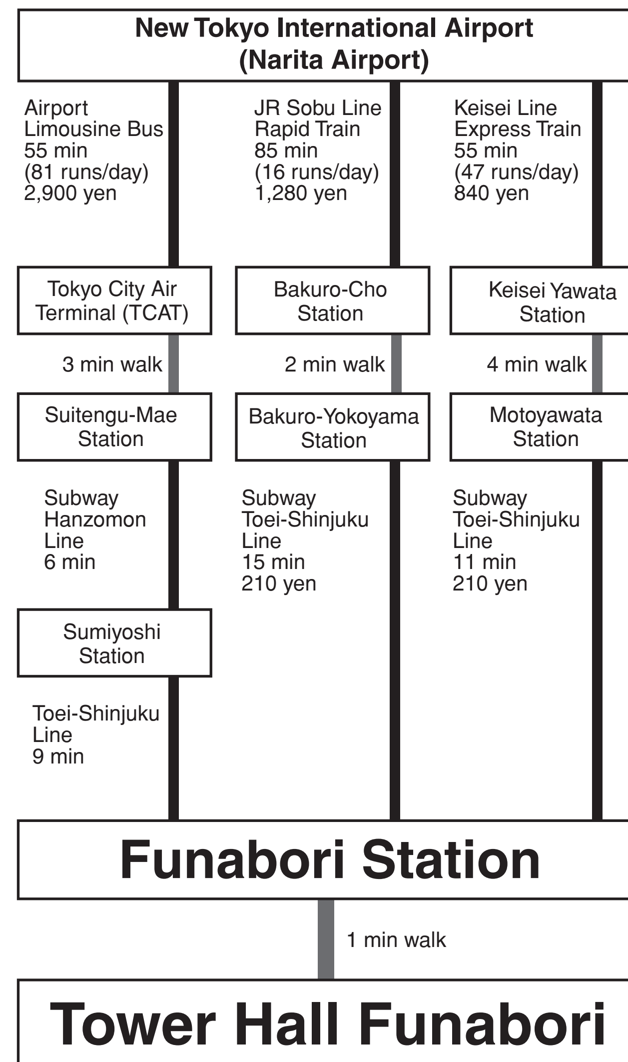

SSDM 2004 Floor Map, TOWER HALL FUNABORI

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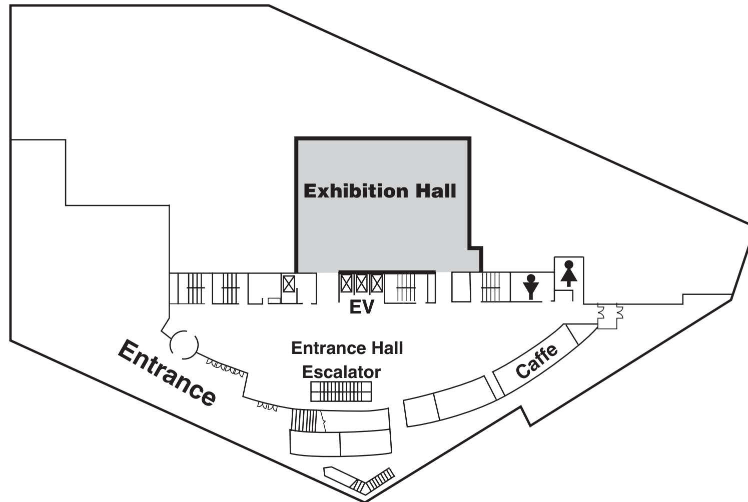

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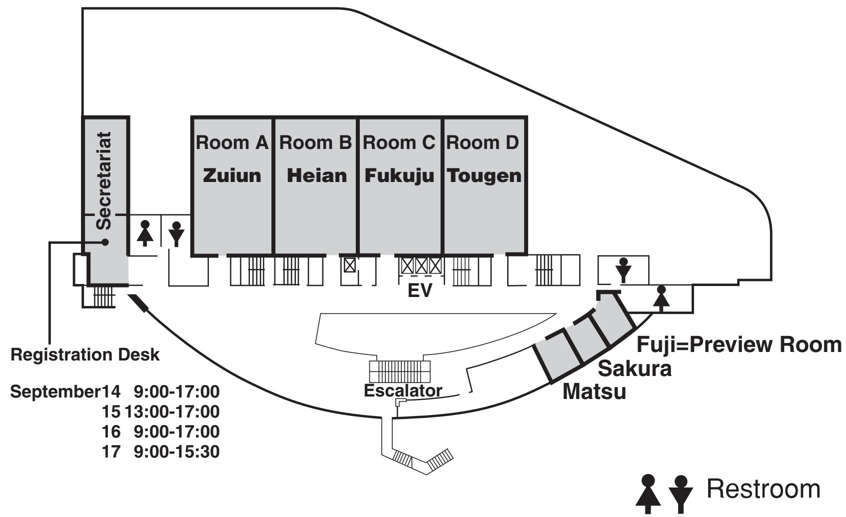

SSDM 2004 Floor Map, TOWER HALL FUNABORI

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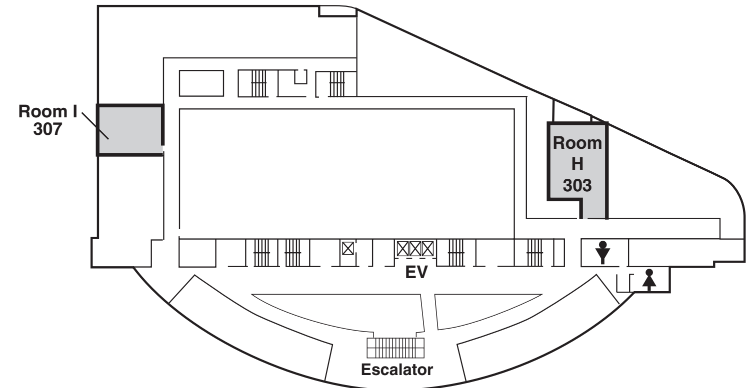

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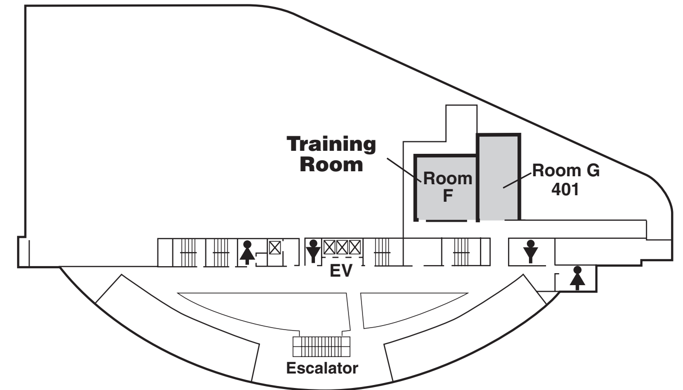

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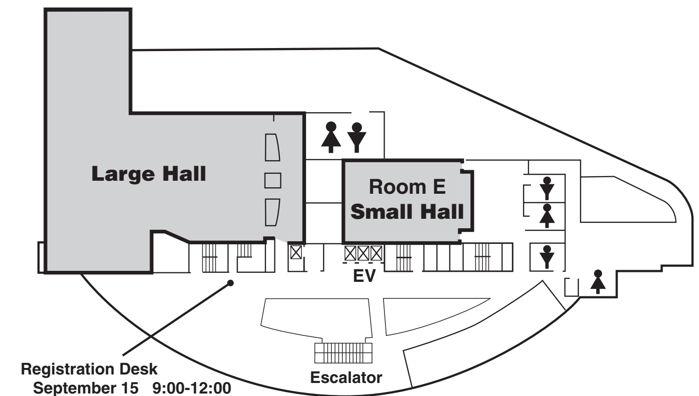

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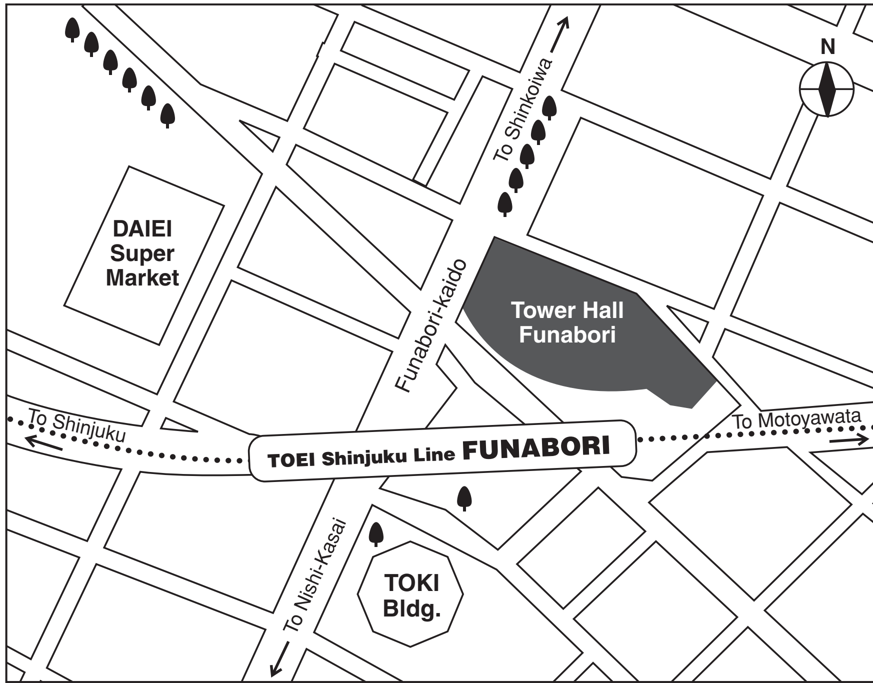

Rail Map