Call for Papers

2005 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference: September 13-15, 2005
Short Course (in Japanese): September 12, 2005

The 2005 International Conference on Solid State Devices and Materials (SSDM 2005) will be held from September 13 to September 15, 2005 at International Conference Center Kobe (Hyogo, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid-state devices and materials. For the 2005 conference, 11 program subcommittees have been organized covering circuits and systems, as well as devices and materials. A one-day short course is also scheduled prior to the conference, offering tutorial lectures on important aspects of the technology.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in July. More information about SSDM 2005 is available online at:

http://www. ssdm.jp

PLENARY SESSIONS

Plenary Speakers:

"Development of Clinical Chips for Home Medical Diagnostics" (tentative)

Y. Horiike (NIMS, Japan)

"Carbon Nanotube Electrical & Optical Devices"

P. Avouris (IBM, USA)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging them to discuss problems to be solved in these fields, new findings, new phenomena, and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate mutual understanding among people in the device and material fields and those in the circuit, system and packaging fields. For the 2005 conference, eleven program subcommittees have been organized in order to realize selection of higher quality papers and strengthen specific technology areas. The scope of each subcommittee is listed below.

Area 1

Advanced Gate Stack/Si Processing Science

(Chair: Y. Nara, Selete)

This subcommittee covers all the innovative front-end-of-line process technologies for advanced silicon-based LSI devices. Papers are solicited in the following areas (but are not limited to these areas): (1) advanced gate stack technologies, such as a SiON gate insulator, high-k gate insulator, and metal gate technologies, including device integration technology; (2) front-end-of-line process technologies that break through the scaling limit, such as a low-temperature process, shallow junction formation, novel diffusion/oxidation, and high-precision etching; (3) reliability physics and analysis; and (4) characterization and modeling of a Si process.

Invited speakers:

"Advanced Gate Stack Technology –Present Status and Challenges–" (tentative)

M. Niwa (Matsushita Electric, Japan)

"Current Status and Forecast toward hp45nm Node in CMOS Technology" (tentative)

T. Sugii (Fujitsu, Japan)

"Material and Process Characterization for Future CMOS Technology" (tentative)

S. Zaima (Nagoya Univ., Japan)

Area 2

Characterization and Materials Engineering for Device Integration

(Chair: S. Ogawa, Matsushita Electric)

In this session, technologies and sciences that cover a Si back-end-of-line process are discussed, including package technology. Low-k materials have been in practical use; however, they brought new, difficult issues with decreasing in size, especially in reliability and package areas, and these areas require different ideas from conventional interconnect in characterization, material, and process/structure technologies. Papers are solicited in the following areas (but are not limited to these areas): (1) characterization methodology for materials, mechanical and electrical properties in small geometry, and yield improvement; (2) materials and process technologies for advanced Cu/Low-k interconnect, including new dielectric and metal formation, planarization, and etching; (3) reliability phenomena and physics, such as EM, SIV, TDDB, and modeling/prediction; (5) packaging for Cu/Low-k chips; (4) new concepts and materials for future interconnects, such as a 3-D structure, a CNT interconnect, and wireless applications.

Invited speakers:

"Integration Challenges for Carbon Nanotubes"

F. Kreupl (Infineon, Germany)

"Cu/Low-k Process Integration for 65nm and 45nm SoC Devices"

N. Matsunaga (Toshiba, Japan)

"Nm-Order Structures of Porous Low-k Film and its Impact on Cu/Low-k Process"

M. Shimada (Selete, Japan)

Area 3

CMOS Devices/Device Physics

(Chair: K. Shibahara, Hiroshima Univ.)

The aim of this area is to discuss advanced silicon device

technologies and physics. Papers are solicited in the following areas: (1) sub-100-nm silicon CMOS devices and their integration technologies; (2) performance enhancement technologies, such as a strained-silicon channel and SiGe and Ge channels; (3) post-bulk-planar silicon device structures, including planar SOI, FinFET, and double gate FET; (4) device physics of advanced CMOS, including simulation and modeling on carrier transport and reliability; and (5) manufacturing and yield science.

Invited speakers:
"Perspective on Emerging CMOS Devices and their Impact on Scaling Technologies" (tentative)
S. Biesemans (IMEC, Belgium)
"45nm Conventional Bulk and Bulk+ Architectures for Low Cost GP/LP Applications" (tentative)
F. Boeuf (ST Microelectronics, France)
"Investigation of NBTI in Ultra-Thin Oxide p-MOSFETs" (tentative)
S. Mahapatra (IIT Bombay, India)

Area 4

Advanced Memory Technology

(Chair: A. Nitayama, Toshiba)

Advanced memory technologies are very much expected to explosively evolve SoC devices and digital information technologies toward "high speed and high density, broadband and mobile." Papers are solicited in the area of all advanced volatile or nonvolatile memory devices, such as DRAM, flash (including SONOS and nanocrystal devices), FeRAM, MRAM, phase change RAM, resistance RAM, one time programming memory, 3-D memory, and others. Topics include cell device physics and characterization, process integration and materials, tunneling dielectrics, ferroelectric and ferromagnetic materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, process control and yield enhancement, integrated circuits, new concept memories, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited speakers:
"Overview and Future Challenges of MONOS Technologies"
T. Ishimaru (Hitachi, Japan)

"Current Development Status and Future Challenge of FeRAM Technologies" (tentative)

S. Y. Lee (Samsung Electronics, Korea)

"Physical and Microscopic Understanding of Data Retention Time of DRAM"

K. Okonogi (Elpida, Japan)

"Overview and Future Challenge of MRAM Technologies"

S. Tehrani (Freescale, USA)

Area 5

Advanced Circuits and Systems

(Chair: H. Kobayashi, Gunma Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems in Si-ULSI, including SiGe, are solicited in subject areas that include, but not limited to the following: (1) advanced digital, analog, mixed-signal circuits as well as memory; (2) high-speed and high-frequency circuits; (3) wireless, wireline, and optical communication; (4) power management technology; (5) interconnection design for communication inside a chip as well as among chips; (6) technologies for systems on a chip (SoC) and system in a package (SiP); and (7) LSI testing technology.

Invited speakers:

"Design and Architecture Exploration for Image and Video Coding Systems"

L.-G. Chen (National Taiwan Univ., Taiwan)

"Issues of Mixed-Signal Circuit Design in 90nm CMOS LSI Technology"

T. Iida (Toshiba, Japan)

"The High Voltage Anti-Trend"

C. Mangelsdorf (Analog Devices Inc., Japan)

Area 6

Compound Semiconductor Circuits, Electron Devices and Device Physics

(Chair: M. Kuzuhara, Univ. of Fukui)

This session covers all aspects of advanced electron device and IC technologies based on compound semiconductors, including III-V, III-N, SiC, and other materials. Papers are solicited in the following areas: (1) FETs, HFETs, HBTs, and other novel device structures; (2) high-voltage or high-temperature electron devices and circuits; (3) microwave and millimeter-wave amplifiers,

oscillators, switches, and other ICs; (4) high-speed digital ICs and mixed-signal ICs; (5) theory and physics of electron devices; (6) characterization techniques for devices and ICs; (7) innovative device processing and packaging; (8) reliability issues; and (9) novel applications utilizing compound semiconductor devices and circuits. Contributions related to other interesting topics are also welcome.

Invited speakers:
"Insulated and Recessed Gate A1N/GaN/InN-based HEMTs on Different Substrates"
M. Shur (Rensselaer Polytechnic Inst., USA)
"Circuit Design for Super-Scaled InP HBTs" (tentative)
J. F. Jensen (Hughes Res. Labs., USA)
"Simulation of AlGaN/GaN Heterostructure Field Effect Transistors"
R. Mickevicius (Integrated Systems Engineering Inc., USA)
"Power Device Application of AlGaN/GaN HFETs on a Si Substrate"
T. Egawa (Nagoya Inst. of Tech., Japan)

Area 7

Photonic Devices and Device Physics

(Chair: M. Sugawara, Univ. of Tokyo)

The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices as well as device physics, which include: (1) laser diodes, LEDs, photodetectors, SOAs, and OEICs; (2) quantum nanostructure optical devices including quantum wells, quantum wires, or quantum dots; (3) photonic crystal materials and novel functional devices; (4) optical switches, modulators, and MEMS; (5) optical wavelength converters, nonlinear optical devices, and all-optical switches; (6) waveguide components, PLCs and integrated photonic circuits; (7) material and device processing and characterization techniques; (8) hybrid and monolithic integration, packaging and moduling; (9) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices; (10) linear and nonlinear optical properties, electronic band structures, and the relaxation mechanism of quantum nanostructures; and (11) novel phenomena and

applications including slow light, fast light, optical memory, and optoelectronic tweezers, etc.

Invited speakers:
"Recent Trend in High-Speed/Low-Power-Consumption Light Sources for MAN/Ethernet Applications"
M. Aoki (Hitachi, Japan)
"Slow Light Using Semiconductor Quantum Wells and Quantum Dots for Future Optical Networks"
S. L. Chuang (Univ. of Illinois at Urbana-Champaign, USA)
"Exciton-Photon Interactions in a Quantum Dot Microcavity"
A. Forchel (Univ. of Wüerzburg, Germany)

Area 8

Advanced Material Synthesis and Crystal Growth Technology

(Chair: H. Yamaguchi, NTT)

The scope of this subcommittee covers all kinds of synthesis, growth, and fabrication techniques of not only semiconducting but also novel functional materials and structures, including spintronic materials, nitride compounds, CNT, nanowires and nanoparticles, etc. The principle idea is to enhance mutual communication among people in different committees to share knowledge of commonly important key technologies in fabrication processes. Specific scopes are, but not limited to, the following: (1) novel material systems and structures; (2) materials and structures for spintronics; (3) nitride-related compound semiconductors; (4) novel synthesis, growth, and fabrication techniques; (5) carbon nanotubes; (6) nanowires and nanoparticles; (7) microscale- and nanoscale 3-D structures and mechanical systems; (8) characterization of fundamental properties.

Invited speakers:
"Revolution in Carbon Nanotube Synthesis –Super Growth–"
D. Futaba (AIST, Japan)
"Quantum Dots, Quantum Dot Molecules, and Quantum Dot Crystals"
O.G. Schmidt (Max-Planck-Inst., Germany)
"Spintronics Based on ZnO Thin Films"
H. Tabata (Osaka Univ., Japan)

"To be announced"
Z. K. Tang (Hong Kong Univ. of Sci. & Tech., China)

Area 9

Physics and Applications of Novel Functional Materials and Devices

(Chair: Y. Takahashi, Hokkaido Univ.)

This session covers applications and physics of novel functional devices and quantum nanostructures that are made mainly by using nanofabrication technology or self-organized phenomena. Papers are solicited in the following areas (but are not limited to these areas): (1) quantum phenomena in nanostructures; (2) quantum dots and single-electron devices; (3) solid-state quantum computing and communications; (4) spintronics; (5) carbon nanotube devices; (6) nanometer-scale characterization, such as SPM and SNOM, other novel devices, such as small superconducting devices, and resonant tunneling devices in nanoscale.

Invited speakers:
"Manipulation and Storage of Charge and Spin in Quantum Dot Devices"
G. Abstreiter (Walter Schottky Inst., Germany)
"Fabrication and Demonstration of Quantum-Dot Cellular Automata Systems"
G. H. Bernstein (Univ. of Notre Dame, USA)
"Optical Spin-Detection of Quasi-2D Charge Carriers: Experimental Evidence of the Spin Hall Effect"
J. Wunderlich (Hitachi Cambridge Lab., UK)

Area 10

Organic Materials Science, Device Physics, and Applications

(Chair: K. Kudo, Chiba Univ.)

This field covers organic materials, device physics, characterization, and applications to organic devices. Papers are solicited in the following areas (but are not limited to these areas): (1) organic transistors and circuits; (2) organic light emitting devices; (3) organic diodes, photodetectors, and photovoltaic devices; (4) chemical sensors and gas sensors; (5) molecular electronics; (6) fabrication and characterization of organic thin films; (7) electrical and optical properties of organic thin film and materials; (8) organic-inorganic hybrid systems; and (9)

interfacial phenomena, LC devices, etc.

Invited speakers:
"Organic Semiconductor Field-Effect Transistors and Circuits" (tentative)
J. Kanicki (Univ. of Michigan, USA)
"Recent Progresses of Organic Transistor Integrated Circuits for Large-Area Sensor Applications" (tentative)
T. Someya (Univ. of Tokyo, Japan)
"Organic Thin-Film Transistors Based on n-Channel Organic Semiconductors" (tentative)
S. Tokito (NHK, Japan)

Area 11

Micro/Nano Electromechanical and Bio-Systems

(Chair: H. Tabata, Osaka Univ.)

This session focuses on micro/nano electrnomechanical systems (MEMS/NEMS) and their applications, such as biosensors. Bio-M/NEMS devices are widely applied to biochemical, medical, and environmental fields in which many devices are studied, such as biochips, micro-TAS, lab on a chip, etc. Interdisciplinary research of microelectronic devices with materials and technique in the chemical, biological, and medical fields is expected to open the door to new scientific and business fields. Papers are solicited in the following areas (but are not limited to these areas): (1) micro/nano electromechanical systems (M/NEMS) for RF, optical, power and biomaterial fields, and others; (2) micro-TAS and lab on a chip; (3) various biochips and sensors; (4) fabrication technologies and surface/interface modification techniques, such as SAM for micro-TAS and/or biochips; and (5) new integrated micro/nanosystems for biochemical and medical applications.

Invited speakers:
"Bionanotechnology with Membrane Proteins: Mechanics and Electronics"
S. A. Contera (Univ. of Oxford, UK)
"Integrated Microfluidic Systems for Cell and Tissue Engineering"
T. Fujii (Univ. of Tokyo, Japan)
"Computational 3-D Microfabrication for MEMS"
O. Tabata (Kyoto Univ., Japan)

RUMP SESSIONS

Following two Rump Sessions have been organized on September 14 (Wednesday).

Session A

"Beyond the Scaling Limit—Innovative Devices and Materials—"

Organizer/Moderator :

Y. Hirayama (NTT, Japan)
K. Masu (Tokyo Tech., Japan)
H. Tabata (Osaka Univ., Japan)
S. Zaima (Nagoya Univ., Japan)

Within 10 years, device sizes will surely reach less than 10 nm and we will then face a problem called the scaling limit. As we approach or go beyond the scaling limit, we need innovative concepts in signal transfer and processing. We will also have to take into account quantum effects in addition to classical effects even at room temperature. In this rump session, we would like to discuss what will happen in this situation from technological and physical viewpoints and what will be necessary to overcome this near-future problem. Innovative device designs, process technologies and integration methods will be played up in this rump session. The introduction of innovative materials will be a key issue for future devices. Our discussions will not be limited to conventional silicon devices; they will extend to compound semiconductors and non-silicon based materials, i.e. oxides, carbon based compounds and molecules, as well. It is our hope that this rump session will get everyone thinking about the scaling-limit and that the discussions in this session become a starting point for new scaling concepts.

Session B

"Flexible Electronics –Is it Real?"

Organizer:

H. Matsuoka (Hitachi, Japan)

Moderator:

To be announced

Special attention has been paid to flexible electronics because of the remarkable progress of device technologies such as organic thin-film transistor and semiconductor

nanowire. Recently, many interesting applications have been proposed, such as wearable computers, flexible image scanners, flexible displays, etc. Flexible electronics has the potential to offer advantages over existing technologies and to open a new market. In this rump session, we would like to discuss the following issues;

(1) What kind of future does flexible electronics bring about?
(2) When will it become real?
(3) What features are required for a device technology? What are the candidates?
(4) What are the technical hurdles to overcome? Where are we now?

We hope you will gain an understanding of the present status and join in the discussion on the future prospects for this fascinating technology.

SHORT COURSE

Short Course entitled "Organic Semiconductor Devices with Attractive and Possible Properties" will be held on Monday, September 12. All lectures are given in Japanese.

SUBMISSION OF PAPERS

Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference web site at http://www.ssdm.jp.

Please note that submissions by post will NOT be accepted.

Deadline for Submission is May 12, 2005.

The two-page paper must be prepared in English in 8.5-×11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. The second page should be used to indicate figures, tables and photographs. Detailed format information will be posted on the conference web site. Two-byte characters such as Japanese, Chinese, Korean, etc. fonts cannot be used for either figures or texts. The paper should report original, previously unpublished work, including specific results.

Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed, without opportunity for further revision, in the extended abstracts that which will be distributed to conference participants during the conference.

Authors of papers accepted for presentation at SSDM 2005 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2006.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted through the conference web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

Late News Paper Deadline is July 29, 2005.

Notices of acceptance will be e-mailed by mid-August.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include a plenary session, along with technical sessions comprising solicited papers and those submitted for oral or poster presentations.

AWARDS

"SSDM Awards" will be given to outstanding papers presented at previous conferences.

SSDM Award
Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 1999.

SSDM Paper Award
Given for the best paper presented at the previous year's conference.

SSDM Young Researcher Award
Given for outstanding papers authored by young researchers and presented at the previous year's conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.
An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF).

BANQUET

The conference banquet will be held on the evening of Tuesday, September 13. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

REGISTRATION

Participants are required to register online at the conference web site http://www.ssdm.jp, in which the order forms for registration, short course and banquet will be available in the beginning of June, 2005.

The registration and banquet fees are:

	Registration Fee		Short Course (in Japanese)	Banquet
	On or before August 12	After August 12		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanied person				¥4,000

* Fees include tax.

VISA REQUIREMENT

All foreign participants must have a valid passport.
Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese Embassy or Consulate as soon as possible.
Concerning visa applications, generally, in applying for a visa each applicant is requested to submit the documents listed below:

(1) an invitation letter (an optional document written in English)
(2) a letter of guarantee (written in Japanese)
(3) documents certifying the purpose of the visit (written in Japanese)
(4) the applicant's schedule in Japan (written in Japanese)

Please ask the nearest Japanese Embassy to make sure what documents are required to obtain a visa first, and then contact the SSDM Secretariat. The Secretariat will send the Reply Form for Visa Application in order to obtain the required documents. Please complete the Reply Form for Visa Application and submit it to the secretariat. We will send you all the requested documents as soon as we receive the Reply Form.

LOCATION

SSDM 2005 will be held at International Conference Center Kobe.

6-9-1 Minatojima-Nakamachi, Chuo-ku, Kobe
650-0046, JAPAN

Phone: +81-78-302-5200
Fax: +81-78-302-6485

International Conference Center Kobe opened in 1981. Conveniently situated on Port Island, it effectively functions as the core of Kobe's well developed convention facilities.

A Limousine bus takes you from Kansai International Airport (KIX) to Kobe in 80 minutes. International Conference Center Kobe is only 10 minutes from the center of downtown Kobe by Port Liner.

For further information, see
http://www.kcva.or.jp/kcc/icck/e-index.html

OFFICIAL TRAVEL AGENT

JTB Corp.
Yokohama Group Tours Office
6F, 3-29-1 Tsuruya-cho, Kanagawa-ku,
Yokohama 221-0835, Japan
Fax: +81-45-316-5701
Phone: +81-45-316-4602
E-mail: jtb_convention@jtb.jp

Accommodations

JTB has blocked rooms at the following hotels in Kobe for the conference period. Reservations can be made through the conference website beginning in April. If the hotel of your first choice is fully booked, your second choice or a hotel of the same grade will be reserved.

Application and payment

Participants wishing to reserve hotels should access the Accommodation page of the conference website. The page will open early in April and reservations should be made by no later than August 19, 2005. (Confirmation sheet will be sent by JTB.)

Application should be accompanied by a remittance covering the total accommodation fee plus handling fee (¥525) due JTB.

No reservation will be confirmed in the absence of this payment. All payment must be in Japanese yen. If the remitter's name is different from the participant's name, or if the amount covers more than one person, please inform us of the details for the payment.

Hotel Name	**Kobe Portopia Hotel**
Room Rates	Single: ¥9,450 Twin: ¥16,800 (per room, per night) Single Use of Twin or Double Room: ¥12,600
Check-in/out	Check-in:13:00/Check-out:12:00
Address	6-10-1, Minatojima Nakamachi, Chuo-ku, Kobe, 650-0046, Japan
Phone	+81-78-302-1111
Access to Hotel	2 min. walk from Port Liner Shimin-Hiroba Sta.
To Conference site	next to the site

Hotel Name	**Hotel Pearl City Kobe**
Room Rates	Single: ¥9,975 Twin: ¥17,850 (per room, per night)
Check-in/out	Check-in:14:00/Check-out:11:00
Address	7-5-1, Minatojima Nakamachi, Chuo-ku, Kobe, 650-0046, Japan
Phone	+81-78-303-0100
Access to Hotel	2 min. walk from Port Liner Nakafutou Sta.
To Conference site	5 min. walk to the site

Hotel Name	**Quality Hotel Kobe**
Room Rates	Single: ¥7,500 Twin: ¥17,000 (per room, per night)
Check-in/out	Check-in:15:00/Check-out:10:00
Address	6-1, Minatojima Nakamachi, Chuo-ku, Kobe, 650-0046, Japan
Phone	+81-78-303-5555
Access to Hotel	5 min. walk from Port Liner Shimin Hiroba Sta.
To Conference site	5 min. walk to the site

Hotel Name	**Sannomiya Terminal Hotel**
Room Rates	Single: ¥8,820 Twin: ¥17,220 (per room, per night)
Check-in/out	Check-in:13:00/Check-out:11:00
Address	8-1-2, Kumoi-dori, Chuo-ku, Kobe, 651-0096, Japan
Phone	+81-78-291-0001
Access to Hotel	Connecting to JR Sannomiya Sta.
To Conference site	15 min. by Port Liner & walk to the site

Hotel Name	**Sanside Hotel**
Room Rates	Single: ¥6,090 Twin: not available
Check-in/out	Check-in:15:00/Check-out:10:00
Address	4-1-3, Kumoi-dori, Chuo-ku, Kobe, 651-0096, Japan
Phone	+81-78-232-3331
Access to Hotel	5 min. walk from JR Sannomiya Sta.
To Conference site	20 min. by Port Liner & walk to the site

Note: Room rates include tax and service charge. No meals are included.

Payment should be in the form of:
- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. AMEX
- A bank transfer to JTB Corp. (Message: SSDM)
  Account at the Bank of Tokyo Mitsubishi, Yokohama Branch #480, 3-27-1 Honcho, Naka-ku, Yokohama-shi, Kanagawa 231-0005, Japan (Account number: 0043079)

Cancellation policy for accommodations

In the event of cancellation, written notification should be sent to JTB. Do not contact hotels directly.
The following cancellation fees will be deducted before refunding.

Hotels: Up to 21 days before the arrival date ----------
¥525
2 to 20 days before ----------
20% of daily room charge (minimum ¥525)
1 day before ----------
80% of daily room charge
On the day of arrival or no notice given----------
100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Kobe is warm and sometimes humid in September. The temperature range is 18-30˚C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

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