

Call for Papers

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INTERNATIONAL CONFERENCE ON

# SOLID STATE DEVICES AND MATERIALS

**2006 International Conference  
on Solid State Devices and Materials (SSDM 2006)**

**SECRETARIAT**

c/o Inter Group Corp.  
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Conference—**September 13-15, 2006**  
Short Course—**September 12, 2006**  
Place—**Pacifico Yokohama  
(Kanagawa, Japan)**

Paper Deadline—**May 10, 2006**

Online submission through the conference website  
is available from the end of March.

Late News Paper Deadline—**July 31, 2006**

**Sponsored by  
THE JAPAN SOCIETY OF APPLIED PHYSICS  
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in cooperation with**

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The Institute of Image Information and Television Engineers  
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**2006**

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## Call for Papers

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### **2006 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS**

Conference: September 13-15, 2006  
Short Course (in Japanese): September 12, 2006

The 2006 International Conference on Solid State Devices and Materials (SSDM 2006) will be held from September 13 to September 15, 2006 at Pacifico Yokohama (Kanagawa, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid-state devices and materials. For the 2006 conference, 11 program subcommittees have been organized covering circuits and systems, as well as devices and materials. A one-day short course is also scheduled prior to the conference, offering tutorial lectures on important aspects of the technology.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in July. More information about SSDM 2006 is available online at:

**<http://www.ssdm.jp>**

## PLENARY SESSIONS

Plenary Speakers:

“Nano-CMOS & Emerging Technologies - Myths and Hopes”

T. Skotnicki (STMicroelectronics, France)

“MEMS as Key Components for Systems”

M. Esashi (Tohoku Univ., Japan)

## SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging them to discuss problems to be solved in these fields, new findings, new phenomena, and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate mutual understanding among people in the device and material fields and those in the circuit, system and packaging fields. For the 2006 conference, eleven program subcommittees have been organized in order to realize selection of higher quality papers and strengthen specific technology areas. The scope of each subcommittee is listed below.

### Area 1

#### *Advanced Gate Stack/Si Processing Science*

(Chair: Y. Nara, Selete)

This subcommittee covers all the innovative front-end-of-line process technologies and sciences for advanced silicon-based LSI devices. Not only the gate stack technology but all the new concepts on Si-based front-end process technologies are welcome. Papers are solicited in the following areas (but are not limited to these areas): (1) advanced gate stack technologies, such as a SiON gate insulator, high-k gate insulator, and metal gate technologies, including device integration technology; (2) front-end-of-line process technologies that break through the scaling limit, such as a low-temperature process, shallow junction formation, novel diffusion/oxidation, and high-precision etching; (3) reliability physics and analysis; and (4) characterization and modeling of a Si process.

Invited Speakers:

“Understanding of the Degradation and Breakdown of Sub-1nm EOT High k/Metal Gate Transistors”

G. Groeseneken (IMEC, Belgium)

“High-resolution RBS Analysis of Si-dielectrics Interfaces”  
K. Kimura (Kyoto Univ., Japan)  
Further invited speakers will be added.

## Area 2

### *Characterization and Materials Engineering for Interconnect Integration*

(Chair: S. Ogawa, Matsushita Electric)

Technologies and sciences that cover a Si back-end-of-line process are discussed, including package technology. Low-k materials have been in practical use; however, they brought new, difficult issues with decreasing in size, especially in reliability and package areas, and these areas require different ideas from conventional interconnect in characterization, material, and process/structure technologies. Papers are solicited in the following areas (but are not limited to these areas): (1) characterization methodology for materials, mechanical and electrical properties in small geometry, metrology and yield improvement; (2) materials and process technologies for advanced Cu/Low-k interconnect, including new dielectric and metal formation, planarization, and etching; (3) reliability phenomena and physics, such as EM, SIV, TDDDB, and modeling/prediction; (4) packaging for Cu/Low-k chips; (5) new concepts and materials for future interconnects, such as a 3-D structure, a CNT interconnect, and wireless applications. *A special session focused on advanced Cu/Low-k technologies is scheduled to highlight this area through unit processes, characterization, up to reliability.*

Invited Speakers:

“New Method of Probing Barrier Integrity and Low-k Stability”

C. U. Kim (U. T. Arlington, USA)

“Carbon Nanotube via Technologies for Advanced Interconnect Integration”

M. Nihei (Fujitsu, Japan)

“Si Nano-photonics for LSI On-chip Optical Interconnection”

K. Nishi (NEC, Japan)

“3D System Integration: Enabling Technologies and Applications”

P. Ramm (Fraunhofer IZM, Germany)

“Reliability Challenges for Advanced Copper Low-k Interconnects”

Z. Tokei (IMEC, Belgium)

“Challenges of Cu Metallization for 45nm and beyond”

M. H. Tsai (TSMC, Taiwan)

“Defects in Electroplated Cu and their Impact on Stress Migration Reliability”

A. Uedono (Univ. of Tsukuba, Japan)

“Design of New Ultra Low-dielectric Materials and Characterization”

D. Y. Yoon (Seoul National Univ., Korea)

### Area 3

#### *CMOS Devices/Device Physics*

(Chair: **K. Shibahara, Hiroshima Univ.**)

The aim of this area is to discuss advanced silicon device technologies and physics. Papers are solicited in the following areas: (1) sub-100-nm silicon CMOS devices and their integration technologies; (2) performance enhancement technologies, such as a strained-silicon channel and SiGe and Ge channels; (3) post-bulk-planar silicon device structures, including planar SOI, FinFET, and double gate FET; (4) device physics of advanced CMOS, including simulation and modeling on carrier transport and reliability; and (5) manufacturing and yield science.

Invited Speakers:

“Simulation of Atomic Scale Effects and Fluctuations in Nano-scale CMOS”

A. Asenov (Univ. of Glasgow, UK)

“Direct Silicon Bond (DSB) Mixed Orientation Substrates for High Performance Bulk CMOS Technology”

C.Y. Sung (IBM, USA)

“Sub-10-nm CMOS Devices”

H. Wakabayashi (NEC, Japan)

“MOSFET Performance Enhancement Using Lattice-mismatched Source/Drain Materials”

Y.-C. Yeo (National Univ. of Singapore, Singapore)

## Area 4

### *Advanced Memory Technology*

(Chair: **A. Nitayama, Toshiba**)

Advanced memory technologies are very much expected to explosively evolve SoC devices and digital information technologies toward “high speed and high density, broadband and mobile.” Papers are solicited in the area of all advanced volatile or nonvolatile memory devices, such as DRAM, flash (including SONOS and nanocrystal devices), FeRAM, MRAM, phase change RAM, resistance RAM, one time programming memory, 3-D memory, and others. Topics include cell device physics and characterization, process integration and materials, tunneling dielectrics, ferroelectric and ferromagnetic materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, process control and yield enhancement, integrated circuits, new concept memories, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited Speakers:

“Overview and Future Challenges of Floating Gate Flash Technologies”

F. Arai (Toshiba, Japan)

“Overview and Future Challenge of FeRAM Technologies”

Y. Kato (Matsushita Electric, Japan)

“Mechanisms of Resistance Switching Memory Effect in Oxides”

M. Kawasaki (Tohoku Univ., Japan)

“Overview and Future Challenges of e-DRAM Technologies”

H. Sugimura (NEC, Japan)

## Area 5

### *Advanced Circuits and Systems*

(Chair: **H. Kobayashi, Gunma Univ.**)

Original papers bridging the gap between materials, devices, circuits, and systems in Si-ULSI, including SiGe, are solicited in subject areas that include, but not limited to the following: (1) advanced digital, analog, mixed-signal circuits as well as memory; (2) high-speed and high-frequency circuits; (3) wireless, wireline, and optical communication circuits; (4) power management technology; (5) interconnection design for communication inside a chip as well as among chips; (6) technologies for systems on a chip (SoC) and system in a package (SiP); and (7) LSI testing technology.

Invited Speaker:

“A Practical, Systematic, Simple Method to Evaluate Speed/Bandwidth Potential of CMOS Processes for Analog Design and Related Practical Considerations”

K. Hadidi (Urmia Univ., Iran)

Further invited speakers will be added.

## **Area 6**

### ***Compound Semiconductor Circuits, Electron Devices and Device Physics***

**(Chair: M. Kuzuhara, Univ. of Fukui)**

This session covers all aspects of advanced electron device and IC technologies based on compound semiconductors, including III-V, III-N, SiC, and other materials. Papers are solicited in the following areas: (1) FETs, HFETs, HBTs, and other novel device structures; (2) high-voltage or high-temperature electron devices and circuits; (3) microwave and millimeter-wave amplifiers, oscillators, switches, and other ICs; (4) high-speed digital ICs and mixed-signal ICs; (5) theory and physics of electron devices; (6) characterization techniques for devices and ICs; (7) innovative device processing and packaging; (8) reliability issues; and (9) novel applications utilizing compound semiconductor devices and circuits. Contributions related to other interesting topics are also welcome.

Invited Speakers:

“Methods and Mechanisms for Ohmic Contacts on AlGaN/GaN HEMTs”

I. Adesida (Univ. of Illinois, USA)

“Recent Advances in GaN Power Devices”

T. Kachi (Toyota Central R&D Labs., Japan)

“Diamond-and GaN-based Electronics”

E. Kohn (Univ. Ulm, Germany)

“InP-based High-speed Transistors and their IC Applications”

K. Murata (NTT, Japan)

## Area 7

### *Photonic Devices and Device Physics*

(Chair: M. Sugawara, Fujitsu Labs.)

The scope of this subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices as well as device physics, which include: (1) laser diodes, LEDs, photodetectors, SOAs, and OEICs; (2) quantum nanostructure optical devices including quantum wells, quantum wires, or quantum dots; (3) photonic crystal materials and novel functional devices; (4) optical switches, modulators, and MEMS; (5) optical wavelength converters, nonlinear optical devices, and all-optical switches; (6) waveguide components, PLCs and integrated photonic circuits; (7) material and device processing and characterization techniques; (8) hybrid and monolithic integration, packaging and moduling; (9) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices; (10) linear and nonlinear optical properties, electronic band structures, and the relaxation mechanism of quantum nanostructures; and (11) novel phenomena and applications including slow light, fast light, optical memory, and optoelectronic tweezers, etc. *A special session focused on “Photonic crystals and Si nanophotonics” is scheduled to highlight this area through their concept, design, fabrication processes, and devices.*

#### Invited Speakers:

“Control of Light Emission and Propagation in Semiconductor Photonic Nanostructures”

T. Baba (Yokohama National Univ., Japan)

“Self-Assembled Quantum Dots: Engineered Gain Medium”

S. Oktyabrsky (Univ. at Albany-SUNY, USA)

“Single-photon Generators for Telecom Applications”

T. Usuki (Univ. of Tokyo, Japan)

“Optoelectronic Tweezers: Optical Manipulation Using LEDs and Spatial Light Modulators”

M. C. Wu (Univ. of California, Berkeley, USA)

“Fabrication of Sb-based QDs Structures for Long-wavelength VCSELs”

N. Yamamoto (National Inst. of Information and Communications Technology, Japan)

Further invited speakers will be added.



## **Area 8**

### ***Advanced Material Synthesis and Crystal Growth Technology***

**(Chair: H. Yamaguchi, NTT)**

The scope of this subcommittee covers all kinds of synthesis, growth, and fabrication techniques of not only semiconducting but also novel functional materials and structures, including spintronic materials, nitride compounds, CNT, nanowires and nanoparticles, etc. The principle idea is to enhance mutual communication among people in different committees to share knowledge of commonly important key technologies in fabrication processes. Specific scopes are, but not limited to, the following: (1) novel material systems and structures; (2) materials and structures for spintronics; (3) nitride-related compound semiconductors; (4) novel synthesis, growth, and fabrication techniques; (5) carbon nanotubes; (6) nanowires and nanoparticles; (7) microscale- and nanoscale 3-D structures and mechanical systems; (8) characterization of fundamental properties.

#### **Invited Speakers:**

“Probing Carbon Nanostructures Growth Mechanism Using an In-situ UHVTEM”

Y.-L. Foo (Inst. of Materials Research and Engineering, Singapore)

“Functions and Device Applications of Quantum-sized Silicon”

N. Koshida (Tokyo Univ. of Agri. and Tech., Japan)

“GaN-based Quantum Wires, Discs, and Dots with Novel Electronic Properties”

K. H. Ploog (Paul Drude Inst., Germany)

“Catalyst-free Metal-organic Chemical Vapor Deposition of ZnO Nanorods and their Device Applications”

G.-C. Yi (POSTECH, Korea)

## **Area 9**

### ***Physics and Applications of Novel Functional Materials and Devices***

**(Chair: Y. Takahashi, Hokkaido Univ.)**

This session covers applications and physics of novel functional devices and quantum nanostructures that are made mainly by using nanofabrication technology or self-organized phenomena. Papers are solicited in the following areas (but are not limited to these areas): (1)

quantum phenomena in nanostructures; (2) quantum dots and single-electron devices; (3) solid-state quantum computing and communications; (4) spintronics; (5) carbon nanotube devices; (6) nanometer-scale characterization, such as SPM and SNOM, other novel devices, such as small superconducting devices, and resonant tunneling devices in nanoscale.

Invited Speakers:

“Single-photon Detectors Based on Quantum Dots Devices”

B. Kardynal (Toshiba Research Europe, UK)

“Nanowire Field Effect Transistor”

L.-E. Wernersson (Lund Univ., Sweden)

“Single-Crystal Nanowire Transistor for Future Logic and Memory Applications”

B. Yu (NASA Ames Research Center, USA)

Further invited speakers will be added.

## Area 10

### *Organic Materials Science, Device Physics, and Applications*

(Chair: K. Kudo, Chiba Univ.)

This field covers organic materials, device physics, characterization, and applications to organic devices. Papers are solicited in the following areas (but are not limited to these areas): (1) organic transistors and circuits; (2) organic light emitting devices; (3) organic diodes, photodetectors, and photovoltaic devices; (4) chemical sensors and gas sensors; (5) molecular electronics; (6) fabrication and characterization of organic thin films; (7) electrical and optical properties of organic thin film and materials; (8) organic-inorganic hybrid systems; and (9) interfacial phenomena, LC devices, etc.

Invited Speakers:

“Highly Efficient Carrier Injection and Transport in Organic Light Emitting Diodes”

C. Adachi (Kyushu Univ., Japan)

“Organic Single Crystal Transistors and Interface Control”

Y. Iwasa (Tohoku Univ., Japan)

“TFT Technologies for Flexible Displays”

J. Jang (Kyung Hee Univ., Korea)

“Development of a Printed Dielectric Layer for Organic Transistors”

T. Kamata (AIST, Japan)

## **Area 11**

### ***Micro/Nano Electromechanical and Bio-Systems (Devices)*** **(Chair: H. Tabata, Osaka Univ.)**

This session focuses on micro/nano electromechanical systems (MEMS/NEMS) and their applications, such as biosensors. Bio-M/NEMS devices and bio-sensors are widely applied to biochemical, medical, and environmental fields in which many devices are studied, such as biochips, micro-TAS, lab on a chip, etc. Interdisciplinary research of microelectronic devices with materials and technique in the chemical, biological, and medical fields is expected to open the door to new scientific and business fields. Papers are solicited in the following areas (but are not limited to these areas): (1) micro/nano electromechanical systems (M/NEMS) for RF, optical, power and biomaterial fields, and others; (2) micro-TAS and lab on a chip; (3) various biochips and sensors; (4) fabrication technologies and surface/interface modification techniques, such as SAM for micro-TAS and/or biochips; and (5) new integrated micro/nanosystems for biochemical and medical applications.

#### **Invited Speakers:**

“Digital Microfluidics by Electro Wetting Technique”

R. L. Garrell (UCLA, USA)

“New Approach to Experimental Nano Mechanics for NEMS”

Y. Isono (Ritsumeikan Univ., Japan)

“New Application of Polymeric Microfluidic Chips”

S. H. Lee (Korea Univ., Korea)

“Physical Sensors in MEMS Technology”

K. Maenaka (Univ. of Hyogo, Japan)

## **RUMP SESSIONS**

Following two Rump Sessions have been organized on September 14 (Thursday).

### **Session A**

“Challenges for New Non-Volatile Memories: From Materials to Devices” (tentative)

Organizers/Moderators:

S. Zaima (Nagoya Univ., Japan)

T. Sakata (Hitachi, Japan)

### **Session B**

“Nanotechnology

–Impact on Electronics, Photonics, and Biology–”

Organizers/Moderators:

K. Ishibashi (RIKEN, Japan)

T. Ichiki (Univ. of Tokyo)

Nanotechnology research is expanding its field rapidly, ranging from electronics, photonics, and mechanics to biology, and so on. However, it is still uncertain how it can be used and give real impacts on the fields, except some limited examples. From the fabrication point of view, the bottom-up technology and the top-down technology appear to be still separated, although a technology to make a bridge between them is highly required. From the functionality point of view, the single electronics, spintronics and quantum computing, et al., those discussed in terms of emerging research devices need nanotechnology to fabricate elemental devices for them. What are the new functionality of them? Can these new functional devices be fabricated in reality? Do they help the difficulty that the present silicon devices are facing? What are the biological application, and how it relates to electronics? There are many questions, most of which are difficult to answer. The rump session will begin with presentations from some panelists, followed by free discussions on these issues. We are grateful if audience may find their own answer through the session.

## SHORT COURSE

Short Course entitled “Understanding Basic Physics of Scaled MOSFETs” will be held on Tuesday, September 12. All lectures are given in Japanese.

## SUBMISSION OF PAPERS

Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference web site at <http://www.ssdm.jp>.

**Please note that submissions by post will NOT be accepted.**

*Deadline for Submission is  
24:00, May 10, 2006 (Japan time).*

The two-page paper must be prepared in English in 8.5- $\times$ 11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. The second page should be used to indicate figures, tables and photographs. Detailed format information will be posted on the conference web site. Two-byte characters such as Japanese, Chinese, Korean, etc. fonts cannot be used for either figures or texts. The paper should report original, previously unpublished work, including specific results. Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

## POSTER SESSIONS

Some of the papers will be presented in the Poster Session. All authors of poster presentations are required to give short (2 minutes) presentations.

## EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be printed, without opportunity for further revision, in the extended abstracts which will be distributed to conference participants during the conference.

## **SPECIAL ISSUE in JJAP**

Authors of papers accepted for presentation at SSDM 2006 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2007.

## **AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS**

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

## **LATE NEWS PAPERS**

Late news papers describing important new developments may be submitted through the conference web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

<p><i>Late News Papers Deadline is 24:00, July 31, 2006 (Japan time).</i></p>
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Notices of acceptance will be e-mailed by mid-August.

## **CONFERENCE FORMAT**

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include a plenary session, along with technical sessions comprising solicited papers and those submitted for oral or poster presentations.

## **AWARDS**

“SSDM Awards” will be given to outstanding papers presented at previous conferences.

### **SSDM Award**

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 2000.

### **SSDM Paper Award**

Given for the best paper presented at the previous year's conference.

## **SSDM Young Researcher Award**

Given for outstanding papers authored by young researchers and presented at the previous year's conference.

## **FINANCIAL SUPPORT**

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: [ssdm@intergroup.co.jp](mailto:ssdm@intergroup.co.jp)) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

## **TRAVEL GRANT**

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.

An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF).

## **BANQUET**

The conference banquet will be held on the evening of Wednesday, September 13. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

## **REGISTRATION**

Participants are required to register online at the conference web site <http://www.ssdm.jp>, in which the order forms for registration, short course and banquet will be available in the beginning of June, 2006.

The registration and banquet fees are:

	Registration Fee		Short Course (in Japanese)	Banquet
	On or before 24:00, Aug. 12 (Japan time)	On or After Aug. 13		
Regular	¥ 40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanied person				¥4,000

\* Fees include tax.

## **VISA REQUIREMENT**

All foreign participants must have a valid passport.

Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese Embassy or Consulate as soon as possible.

Concerning visa applications, generally, in applying for a visa each applicant is requested to submit the documents listed below:

- (1) an invitation letter (an optional document written in English)
- (2) a letter of guarantee (written in Japanese)
- (3) documents certifying the purpose of the visit (written in Japanese)
- (4) the applicant's schedule in Japan (written in Japanese).

Please ask the nearest Japanese Embassy to make sure what documents are required to obtain a visa first, and then contact the SSDM Secretariat. The Secretariat will send the Reply Form for Visa Application in order to obtain the required documents. Please complete the Reply Form for Visa Application and submit it to the Secretariat.

We will send you all the requested documents as soon as we receive the Reply Form.

## **LOCATION**

SSDM 2006 will be held at Pacifico Yokohama.

1-1-1 Minatomirai, Nishi-ku, Yokohama

220-0012, Japan

Phone: +81-45-221-2155

Fax: +81-45-221-2136

Pacifico Yokohama, located in Yokohama's new and growing waterfront development Minato Mirai 21 area, is an integrated convention center on a world class scale. Since its opening in 1991, Pacifico Yokohama has hosted a variety of gatherings amid the magnificent surroundings of the international port city of Yokohama, Japan's historic window to the outside world.

It takes less than 2 hours from Tokyo international airport to Pacifico in limousine bus or train. From central Tokyo area, a 30 minutes ride on train will take you to Pacifico.

For further information, see

[http://www.pacifico.co.jp/index\\_e.html](http://www.pacifico.co.jp/index_e.html)



## **OFFICIAL TRAVEL AGENT**

Kinki Nippon Tourist Co., Ltd. (KNT)  
Global Business Management Branch  
Tokyo Kintetsu Bldg. 6F  
19-2 Kanda-Matsunaga-cho, Chiyoda-ku  
Tokyo 101-8641, Japan  
Phone: +81-3-5256-1581  
Fax: +81-3-5256-1588  
E-mail: [ssdm2006-gb@or.knt.co.jp](mailto:ssdm2006-gb@or.knt.co.jp)

## **Hotel Accommodations**

KNT has blocked rooms at following hotels in Yokohama for the conference period.

Reservations can be made through the conference website beginning in June.

If the hotel of your first choice is fully booked, your second choice or a hotel in the same grade will be reserved.

Hotel Name	<b>Yokohama Grand Inter-continental Hotel</b>
Room Rates	Single: ¥23,100 Twin: ¥11,550 (per person, per night) * ¥2,100 will be added to the above rates on Sep. 15 (Fri).
Hotel Deposit	¥20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	1-1-1 Minato Mirai, Nishi-ku, Yokohama, Kanagawa 220-8522, Japan
Phone	+81-45-223-2222
Access to Hotel	2 min. walk from Minato Mirai Line Minato Mirai Sta.
To Conference site	Next to the site

Hotel Name	<b>Pan Pacific Hotel Yokohama</b>
Room Rates	Single: ¥21,000 Twin: ¥12,600 (per person, per night) * ¥3,150 for a single and ¥2,100 for a twin will be added to the above rates on Sep. 15 (Fri).
Hotel Deposit	¥20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	2-3-7 Minato Mirai, Nishi-ku, Yokohama, Kanagawa 220-8543, Japan
Phone	+81-45-682-2222
Access to Hotel	1 min. walk from Minato Mirai Line Minato Mirai Sta.
To Conference site	1 min. walk to the site

Hotel Name	<b>Navios Yokohama</b>
Room Rates	Single: ¥11,445 (per person, per night) * ¥1,050 will be added to the above rates on Sep. 15 (Fri).
Hotel Deposit	¥10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	2-1-1 Shinko, Naka-ku, Yokohama, Kanagawa 231-0001, Japan
Phone	+81-45-633-6000
Access to Hotel	3 min. walk from Minato Mirai Line Bashamichi Sta.
To Conference site	7 min. walk to the site

Hotel Name	<b>Yokohama Sakuragicho Washington Hotel</b>
Room Rates	Single: ¥11,550 Twin: ¥8,925 (per person, per night)
Hotel Deposit	¥10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	1-1-67 Sakuragicho, Naka-ku, Yokohama, Kanagawa 231-0062, Japan
Phone	+81-45-683-3111
Access to Hotel	3 min. walk from Minato Mirai Line Bashamichi Sta.
To Conference site	10 min. walk to the site

Hotel Name	<b>San-ai Yokohama Hotel</b>
Room Rates	Single: ¥9,240 (per person, per night)
Hotel Deposit	¥10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	3-95 Hanasakicho, Naka-ku, Yokohama, Kanagawa 231-0063, Japan
Phone	+81-45-242-4411
Access to Hotel	5 min. walk from JR Sakuragicho Sta.
To Conference site	15 min. walk to the site

Note: All room rates are per person per night, including breakfast, 10% service charge and 5% consumption tax.

## **Application and payment**

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website.

The page will be opened in early April and reservations should be made by no later than August 18, 2006 (Japan time).

\* Confirmation sheet will be sent by KNT after the application deadline.

Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment.

All payment must be paid only in Japanese yen by one of the following methods

### 1) Credit Card:

(VISA, MasterCard, Diners Club, AMEX or JCB only)

\* Please fill in the necessary items with your signature in the credit card section of the application form.

### 2) Bank Transfer:

Sumitomo Mitsui Banking Corp.

Suzuran Branch

SWIFT Code: SMBCJPJT

Account Number: 6103515

Account Name: Kinki Nippon Tourist Co., Ltd.

## **Cancellation**

In case of cancellation, a written notification should be sent to KNT to avoid any trouble.

The cancellation charges are:

Up to 14 days before the arrival date .....No Charge

13-7 days before .....10 % of daily room charge

6-2 days before .....40 % of daily room charge

Less than 2 days, or no notice given

.....100 % of daily room charge

## **Refund**

Refunds will be made during or after the conference after deducting bank and/or credit card service charges and the cancellation penalties.

If payment was made by credit card, refund will be made to the same credit card.

If the payment was made by bank transfer, please inform us your bank account.

\* Communication fee of 500 JPY is not refundable.

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