Call for Papers

2009 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Green Technology

-Nanodevices Toward Environmental-Friendly Society-

Conference — October 7-9, 2009

Short Course & Workshop — October 6, 2009

Place — Sendai Kokusai Hotel

Paper Deadline — May 8, 2009

Late News Paper Deadline — July 27, 2009

Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS
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Web Site_http://www.ssdm.jp

2009 International Conference on Solid State Devices and Materials (SSDM 2009)

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Call for Papers

2009 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference: October 7-9, 2009
Short Course / Workshop: October 6, 2009

The 2009 International Conference on Solid State Devices and Materials (SSDM2009) will be held from October 7 to 9, 2009 at Sendai Kokusai Hotel (Sendai, Miyagi, Japan). Since 1969, the conference has provided an excellent opportunity to discuss key aspects of solid-state devices and materials. For the 2009 conference, 14 program subcommittees have been organized covering circuits and systems, as well as devices and materials. In SSDM 2009, a one-day short course and workshop are also scheduled prior to the conference. The short course offers tutorial lectures on important aspects of the technology. The workshop offers advanced discussion on topical device technologies, "green technology" in SSDM 2009.

Original, unpublished papers will be accepted after review by the Program Committee. Several invited speakers will cover topics of current interest. An Advance Program will appear in August. More information about SSDM2009 is available online at:

http://www. ssdm.jp

PLENARY SESSIONS

Plenary Speakers:

"Moore's Law Past 32nm: the Challenges in Physics and Technology Scaling"

K. Kuhn (Intel Corp., USA)

"The Third Generation of Solar Photovoltaic Electricity"

T. Tomita (Univ. of Tokyo, Japan)

SCOPE OF CONFERENCE

The conference aims at providing a forum for synergistic interactions among research scientists and engineers working in the fields related to solid state devices and materials and encouraging them to discuss problems to be solved in these fields, new findings, new phenomena, and state-of-the-art technologies related to devices and materials. The conference also aims to facilitate mutual understanding among people in the device and material fields and those in the circuit, system and packaging fields. For the 2009 conference, fourteen program subcommittees have been organized in order to realize selection of higher quality papers and strengthen specific technology areas. The scope of each subcommittee is listed below.

Area 1

Advanced Gate Stack / Si Processing & Material Science

(Chair: J. Yugami, Selete)

This subcommittee covers all the innovative front-end-of-line process technologies and sciences for advanced silicon-based LSI devices. Not only the gate stack technology but all the new concepts on Si-based front-end process technologies are welcome. Papers are solicited in the following areas (but are not limited to these areas): (1) advanced gate stack technologies, such as a SiON gate insulator, high-k gate insulator, metal gate, and high-mobility channel materials, including device integration technology; (2) front-end-of-line process technologies that break through the scaling limit, such as a low-temperature process, shallow and conformal junction formation, novel diffusion/oxidation, high-precision dry/wet etching and highly controlled surface preparation technique for nm

scale fabrication; (3) reliability physics and analysis; and (4) Material characterization and modeling for a Si process..

Invited Speakers:
"Development of high-k / metal gate CMOS technology in Selete"
K. Ikeda (Selete, Japan)
"Microscopic Characterization of Devices by Scanning Transmission Electron Microscopy: From single atom imaging to macroscopic properties"
S. J. Pennycook (Oak Rigde National Lab., USA)
"Process Condition Dependence of Random VT Variability in NFETs and PFETs"
T. Tunomura (Selete, Japan)
"Characteristics and Integration Challenges of FinFET-based Devices for sub-32nm technology nodes Circuit applications"
A.Veloso (IMEC, Belgium)

Area 2
Characterization and Materials Engineering for Interconnect Integration

(Chair: M. Matsuura, Renesas Tech. Corp.)

Technologies and sciences that cover a Si back-end-of-line (BEOL) process are discussed, including 3-D interconnects and packaging technologies. These areas require new innovations and different ideas from conventional interconnect in characterization, material, and process/structure technologies. Papers are solicited in the following areas: (1) characterization methodology for materials, mechanical and electrical properties in small geometry, metrology and yield improvement; (2) materials, process and packaging technologies for advanced Cu/Low-k interconnect; (3) reliability phenomena and physics, such as EM, SIV, TDDB, and modeling/prediction; (4) passive components for RF or High-speed operations; (5) new structures and materials on future interconnects, such as a 3-D interconnect with TSV, a CNT interconnect, an on-chip optical interconnect, and BEOL-based memory applications, i.e. MRAM and PRAM.

Invited Speakers:
"Through-Si-Via Technology Solutions for 3D System Integration"
E. Beyne (IMEC, Belgium)
"Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status and Prospects"
K. Banerjee (Univ. of California-Santa Barbara, USA)
"Patterning and metallization options for 22nm node contact module integration"
S. Demuynck (IMEC, Belgium)
"Wireless interconnection by electro-magnetic coupling of open-ring resonators and its application to system integration"
Y. Ohno (Univ. of Tokushima, Japan)
"The Helium Ion Microscope for Device Imaging, Failure Analysis and Circuit Modification Applications"
W. Thompson (Carl Zeiss, USA)

Area 3
CMOS Devices /Device Physics
(Chair: H. Wakabayashi, Sony Corp.)

The aim of this area is to discuss advanced silicon device technologies and physics. Papers are solicited in the following areas: (1) sub-100-nm silicon CMOS devices and their integration technologies; (2) performance enhancement technologies, such as a strained-silicon channel or any high-mobility channels; (3) post-bulk-planar silicon device structures, including planar SOI, FinFET, multi-channels, or nano-wires; (4) device physics of advanced CMOS, including simulation and modeling on carrier transport and reliability; and (5) manufacturing and yield science in conjunction with the increasing variability of device parameters, fluctuations of fabrication parameters or the intrinsic atomistic nature.

Invited Speakers:
"Ultrathin Body and BOX SOI for Low Power Application at the 22nm node and below"
F. Andrieu (CEA-LETI, France)
"Advanced device architectures"
J. Woo (UCLA, USA)

Area 4

Advanced Memory Technology

(Chair: A. Nitayama, Toshiba Corp.)

Advanced memory technologies are very much expected to explosively evolve SoC devices and digital information technologies toward ‘‘high speed and high density, broadband and mobile.’’ Papers are solicited in the area of all advanced volatile or nonvolatile memory devices, such as DRAM, flash (including SONOS and nanocrystal devices), FeRAM, MRAM, phase change RAM, resistance RAM, one time programming memory, 3-D memory, and others. Topics include cell device physics and characterization, process integration and materials, tunneling dielectrics, ferroelectric and ferromagnetic materials, reliability, failure analysis, quality assurance and testing, modeling and simulation, process control and yield enhancement, integrated circuits, new concept memories, and new applications and systems (solid state disks, memory cards, programmable logic, etc.).

Invited Speakers:

"Electrical defects in dielectrics for flash memories studied by Trap Spectroscopy by Charge Injection and Sensing (TSCIS)"

R. Degraeve (IMEC, Belgium)

"Overview and Future Challenges of Capacitor-less DRAM Technologies for High Density Memory Applications"

P. Fazan (Innovative Silicon, Switzerland)

"Overview and Future Challenge of High Density FeRAM"

I. Kunishima (Toshiba Corp., Japan)

"Current Status and Future Challenge of PRAM"

Y-H. Shih (Macronix Int'l Co., Ltd., Taiwan)

"Switching Mechanism of TaOx ReRAM"

Z. Wei (Panasonic Corp., Japan)

"Advancements and Future Challenge of Spin torque MRAM"

H. Yoda (Toshiba Corp., Japan)

Area 5

Advanced Circuits and Systems

(Chair: S. Kawahito, Shizuoka Univ.)

Original papers bridging the gap between materials, devices, circuits, and systems in Si-ULSI, including SiGe, are solicited in subject areas that include, but not limited to the following: (1) advanced digital, analog, and mixed-signal circuits as well as memory; (2) high-speed and high-frequency circuits; (3) wireless, wireline, and optical communication circuits; (4) power devices and circuits as well as power management technology; (5) interconnection design for communication inside a chip as well as among chips; (6) technologies for systems on a chip (SoC) and system in a package (SiP); (7) LSI testing technology; (8) three-dimensional IC technology; (9) MEMS (passive) devices as well as circuits, RF MEMS; (10) sensor devices and circuits; (11) thin film transistors and circuits; and (12) organic transistors and circuits.

Invited Speakers:

"CMOS Circuit Design Techniques for Millimeter-Wave Applications"

R. Fujimoto (Toshiba Corp., Japan)

"Recent Topics in Power Management"

H. Kobayashi (Gunma Univ., Japan)

"Wireless CMOS TSV"

T. Kuroda (Keio Univ., Japan)

"Recent Progress in High-Resolution and High-Speed CMOS Image Sensor Technology"

I. Takayanagi (Aptina Japan, LLC., Japan)

Area 6

Compound Semiconductor Circuits, Electron Devices and Device Physics

(Chair: T. Hashizume, Hokkaido Univ.)

This session covers all aspects of advanced electron device and IC technologies based on compound semiconductors, including III-V, III-N, SiC, oxide semiconductors and other materials. Papers are solicited in the following areas: (1) FETs, HFETs, HBTs, and other novel device structures;

(2) high-voltage or high-temperature electron devices; (3) microwave and millimeter-wave amplifiers, oscillators, switches, and other ICs; (4) III-V high-mobility transistors and high-speed digital ICs; (5) advanced sensor devices; (6) theory and physics of electron devices; (7) processing and characterization techniques for devices and ICs; (8) stability and reliability issues; and (9) novel applications utilizing compound semiconductor devices and circuits. Contributions related to other interesting topics are also welcome.

Invited Speakers:
"Materials and Strain Issues in AIGaN/GaN HEMT Degradation"
E. Munoz (Univ. Politécnica de Madrid, Spain)
"SiC power MOSFETs"
J. Palmour (Cree,USA)
"Performance Projection of III-V and Ge Channel MOSFETs"
H. Tsuchiya (Kobe Univ., Japan)
"Advances of GaN Power Transistors"
Y. Wu (Transphorm Inc.,USA)
"High-performance inversion-mode III-V MOSFETs enabled by atomic-layer-deposited migh-k dielectrics"
P. D. Ye (Purdue Univ., USA)

Area 7
Photonic Devices and Device Physics
(Chair: H. Yamada, Tohoku Univ.)

This subcommittee covers all aspects of emerging technologies in active, passive, and integrated optoelectronic and photonic devices as well as device physics, which include: (1) laser diodes, LEDs, optical amplifiers, and photodetectors; (2) quantum nanostructure optical devices including quantum wells, quantum wires, or quantum dots; (3) photonic nanostructures including photonic crystals; (4) functional optical devices including optical switches, modulators, or optical MEMS; (5) nonlinear optical devices including wavelength converters or all-optical switches; (6) waveguide devices and photonic integrated circuits with silica, silicon, or polymer

materials; (7) photonic devices and integration with silicon photonics; (8) material and device processing and characterization techniques; (9) packaging and moduling for photonic devices; (10) optical communication, interconnection and signal processing applications of optoelectronic and photonic devices; (11) linear and nonlinear optical properties, electronic band structures, and the relaxation mechanism of quantum nanostructures; and (12) novel phenomena and applications including slow light, fast light, optical memory, and optoelectronic tweezers, etc.

Invited Speakers:
"Quantum Dot Lasers. Commercial challenges and opportunities"
A. Kovsh (Innolume, Inc., Germany)
“Active Ge based Devices for Si Photonics”
J. Michel (MIT, USA)
"Optical Gain in Ultra-Thin Silicon Resonant Cavity Light-Emitting Diode"
S. Saito (Hitachi, Ltd., Japan)

Area 8

Advanced Material Synthesis and Crystal Growth Technology

(Chair: A. Yamada, Tokyo Tech.)

The scope of this subcommittee covers all kinds of synthesis, growth, and fabrication techniques of not only semiconducting but also novel functional materials and structures, nitride compounds, CNT, nanowires and nanoparticles, etc. The principle idea is to enhance mutual communication among people in different committees to share knowledge of commonly important key technologies in fabrication processes. Specific scopes are, but not limited to, the following: (1) novel material systems and structures; (2) nitride-related compound semiconductors; (3) novel synthesis, growth, and fabrication techniques; (4) carbon nanotubes; (5) nanowires and nanoparticles; (6) microscale and nanoscale 3-D structures; (7) characterization of fundamental properties.

Invited Speakers:
"High throughput combinatorial materials exploration for advanced magneto-electronics"
T. Fukumura (Tohoku Univ., Japan)
"Growth and electronic structure of epitaxial graphene on silicon carbide"
K. Horn (Fritz-Haber-Institut der Max-Planck-Gesellschaft, Germany)
"III-V Nanowires grown by MOCVD for Optoelectronic Applications"
H. H. Tan (The Australian National Univ., Australia)
"Recent advances in InN-based III-nitrides towards novel nanostructure photonic devices"
A. Yoshikawa, S.-B. Che, Y. Ishitani, N. Hashimoto, and A. Yuki (Chiba Univ., Japan)

Area 9
Physics and Applications of Novel Functional Materials and Devices

(Chair: T. Fujisawa, Tokyo Tech.)

This session covers physics, applications and fabrication techniques of novel functional devices and materials. We strongly encourage novel, pioneering, and fundamental research works that would be influential in various solid state devices of materials (semiconductors, metals, superconductors, magnetic and organic materials, etc.). Specific topics are (1) quantum phenomena in nanostructures; (2) transport and optical characteristics of low-dimensional structures; (3) devices dealing with single electron, hole, excition, photon, and other quanta; (4) solid-state quantum computing and communications; (5) nanometer-scale characterization with spanning probe techniques; (6) nanofabrication techniques and self-organized phenomena; and (7) other novel functional devices, but are not limited to these subjects.

Invited Speakers:
"Spin Read-Out of Donors in Silicon"
M. Brandt (Walter Schottky Inst., Germany)
"Electromechanical Systems for Memory and Logic Devices"
I. Mahboob (NTT Basic Res. Labs., Japan)

"From single-atom spectroscopy to lifetime enhanced triplet transport in MOSFETs"

S. Rogge (Delft Univ. of Tech., Netherlands)

"AFM nanolithography of grapheme"

L. Rokhinson (Purdue Univ., USA)

Area 10

Organic Materials Science, Device Physics, and Applications

(Chair: K. Kato, Niigata Univ.)

This field covers organic materials, device physics, characterization, and applications to organic devices. Papers are solicited in the following areas (but are not limited to these areas): (1) organic transistors and circuits; (2) organic light emitting devices; (3) organic diodes, photodetectors, and photovoltaic devices; (4) chemical sensors and gas sensors; (5) molecular electronics; (6) fabrication and characterization of organic thin films; (7) electrical and optical properties of organic thin film and materials; (8) organic-inorganic hybrid systems; and (9) interfacial phenomena, LC devices, etc.

Invited Speakers:

"Roll-to-Roll Printed 13.56 MHz Operated RFID Tags on Plastic Foils"

G. Cho (Sunchon National Univ., Korea)

"Efficient organic p-i-n solar cells having very thick codeposited i-layer consisting of highly purified organic semiconductors"

M. Hiramoto (IMS, Japan)

"Environmental and Electrical Stability of Organic Transistors"

D. Knipp (Jacobs Univ. Bremen, Germany)

"Organic TFT-Driven Flexible Displays"

K. Nomoto (Sony Corp., Japan)

"Surface selective deposition of molecular semiconductors for solution-based integration of organic field-effect transistors"

K. Tsukagoshi (MANA-NIMS, Japan)

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Area 11
Micro/Nano Electromechanical and Bio-Systems (Devices)

(Chair: I. Yamashita, NAIST)

This session focuses on micro/nano electromechanical systems(MEMS/NEMS) and their applications, such as biosensors. Bio-M/NEMS devices and bio-sensors are widely applied to biochemical, medical, and environmental fields in which many devices are studied, such as biochips, micro-TAS, lab on a chip, etc. Interdisciplinary research of microelectronic devices with materials and technique in the chemical, biological, and medical fields is expected to open the door to new scientific and business fields. Papers are solicited in the following areas (but are not limited to these areas): (1) micro/nano electromechanical systems(M/NEMS) for RF, optical, power and biomaterial fields, and others; (2) micro-TAS and lab on a chip; (3) various biochips and sensors; (4) fabrication technologies and surface/interface modification techniques, such as SAM for micro-TAS and/or biochips; and (5) new integrated micro/nanosystems for biochemical and medical applications.

Invited Speakers:
"Silicon and glas microfabricated cell separation systems using ultrasonic standing wave forces"
T. Laurell (Lund Univ., Sweden)
"Bio-transducers for biomedical applications"
K. Mitsubayashi (Tokyo Medical & Dental Univ., Japan)
"Soft Bio-materials in Solid State Devices"
K. Shiba (Japanese Foundation for Cancer Res., Japan)

Area 12
Spintronic Materials and Devices

(Chair: K. Ando, AIST)

This field covers spintronic materials (metals, semiconductors, insulators, hybrid structures, and nanostructures), spin-related phenomena, and device

applications. Papers are solicited in the following areas (but are not limited to these areas): (1) ferromagnetic and/or half-metallic materials; (2) hybrid structures and nanostructures in which spin effects are apparent and important; (3) spin-dependent optical and transport phenomena; (4) spin dynamics; (5) spintronics devices and systems including magnetic tunnel junctions and TMR devices, nonvolatile memory, magnetic sensors, spin-transistors, optical isolators, optical switches etc; (6) quantum information processing using spin states.

Invited Speakers:
"Spin Injection, Transport, and Control in Silicon"
I. Applebaum (Univ. of Maryland, USA)
"Spin transfer microwave emission in metallic nanopillars and magnetic tunnel junctions"
J. Grollier (UMP CNRS-Thales, France)
"Silicon spintronic devices"
R. Jansen (Univ. of Twente, Netherland)
"Non-volatile logic based on MTJ"
T. Hanyuu (Tohoku Univ., Japan)
"High-speed Magnetic Memory based on Spin-Torque Domain Wall Motion"
N. Ishiwata (NEC Corp., Japan)
"Graphene Spintronics"
M. Shiraishi (Osaka Univ., Japan)

Area 13

Applications of Nanotubes and Nanowires

(Chair: K. Ishibashi, RIKEN)

All kinds of applications using nanotubes & nanowires are included in the scope of this sub-committee. Nanotubes & nanowires, e.g., carbon nanotube, BN nanotube, Si nanowire, compound semiconductor nanowire, layered nanowire, etc. are all included. Molecular nanostructures are also within our scope. Applications using nanotubes & nanowires in the scope are as follows; 1) Active electronic and optical devices, e.g., FET, HEMT, optical transistor, optical switch, and quantum devices including single electron transistor(SET), SET logics, resonant tunneling devices, quantum computing devices and so on. 2) All

kinds of sensors, e.g., bio sensors, gas sensors, pressure sensors, acceleration sensors and so on. 3) Application for passive elements, e.g., wiring & via technology for future LSI and so on. 4) Nanomechanical application, e.g., probe applications for STM/AFM, tweezers, motors, oscillators and so on. 5) Fundamental research related to those applications of nanotube & nanowire, e.g., new growth technology, analysis of growth mechanism, new device fabrication process and so on. 6) New evaluation technology, e.g., TEM, SEM, Raman scattering, photo luminescence and so on. 7) Theoretical analysis of device physics, new physics in the nanotube & nanowire, e.g., Tomonaga liquid, one dimensional quantum transport and so on.

Invited Speakers:
"Giant g-factors, Kondo physics, and anomalous spin-correlated blockade in few-electron InSb nanowire quantum dots"

H.Q.Xu (Lund Univ., Sweden)

"Metal-free Elementary Semiconductor Nanowires: Synthesis and Device Applications"

D. Whang (Sungkunkwan Univ., Korea)

Area 14

Power Electronics

(Chair: M. Ishiko, Toyota Central R&D Labs., Inc.)

This session focuses on energy conversion devices such as solar cells and power devices which are key devices to contribute to the greenhouse gas reduction as well as energy resource saving, and the scope covers all aspects of energy conversion device technologies and applications. Papers are solicited in the following areas (but are not limited to these areas): (1) materials and processes for Solar cells based on crystalline silicon, amorphous/microcrystalline silicon, CIS, III-V, CdTe, and organic molecules; (2) processes and characterization of solar cells and power devices including crystal growth, doping, etching, passivation and lithographic techniques; (3) device physics and modeling including novel device concept, power ICs (isolation techniques, SOI, monolithic

vs. hybrid, ESD;etc.), high & low power devices, RF power devices; (4) CAD/simulation including novel device, device & circuit design, layout, verification tools; (5)packaging, module and interconnection technologies including photovoltaic systems, stress & thermal simulation, reliability analyses & measurements (solder, etc.), integration methodology; (6) applications including photovoltaic systems and their components, power supply, motor control, power management, evaluation methods.

Invited Speakers:

"Towards a better understanding of heterojunction solar cells: key parameters and overestimated ones."

J. Damon-Lacoste (EPFL, Switzerland)

"Technology Trends of CZ-Silicon Substrates for Power Devices"

K. Kashima (Covalent Materials Corp., Japan)

"Current Status and Technology Trends of Grid-Interactive Inverter for PV Application"

S. Nishi (Sharp Corp., Japan)

“Silicon Carbide Wafer Technologies for Power Devices”

S. Nishizawa (AIST, Japan)

"Defect characterization of CIS-related compound solar cells by admittance spectroscopy and DLTS"

P. Zabierowski (Warsaw Univ. of Tech., Poland)

RUMP SESSIONS

Following two Rump Sessions have been organized on October 8 (Thursday).

Session A

"Novel Lithography for more Moore/beyond CMOS and More than Moore"

Organizer: K. Masu (Tokyo Tech., Japan)
Moderator: H. Wakabayashi (Sony Corp., Japan)
M. Hane (NEC Corp., Japan)

Based on the discussion of orthodox lithography technology for ultimate CMOS, future of beyond CMOS technology is discussed then the novel lithography technology is foreseen with glances of beyond CMOS devices. Furthermore, lithography for toward more than Moore, such as 3D integration, MEMS integration, etc. are discussed.

Session B

"Solar Cells for Electronics: from In-Vehicle to Ubiquitous"

Organizer: K. Ohashi (NEC Corp., Japan)
Moderator: M. Ishiko (Toyota Central R&D Labs., Inc, Japan)
N. Usami (Tohoku Univ., Japan)

Mass production of solar cells has boosted their market growth from several MW to more than 1 GW in the past quarter century. These cells present great promise as a clean, inexpensive electric power source for portable electronics applications. Future inexpensive lightweight photo voltaic devices are expected to change the electronic systems more ubiquitous ones by eliminating unnecessary electric wires. In this rump session, we will invite presenters representing application and technology sides from all the areas of the 41th SSDM to provide a vision of "How new photovoltaic systems change the electronics and human societies".

SHORT COURSE

"From Basic Theory to Newest Application in MOS Devices"

Organizer: Y. Uraoka (NAIST, Japan)
N. Matsunaga (Toshiba Corp., Japan)

Short Course will be held on Tuesday, October 6. Short Course offers tutorial lectures on important aspects of the technology. All lectures are given in English.

Topics:
"Advanced LSI Technology"
T. Hiramoto (Univ. of Tokyo, Japan)
"Gate Stack Technology"
M. Niwa (Panasonic Corp., Japan)
"Nano Fabrication Technology"
K. Ueno (Shibaura Inst. of Tech., Japan)
"Analysis Technique of LSI device"
S. Miyazaki (Hiroshima Univ., Japan)
"Nano device design by Theoretical Approach"
K. Shiraishi (Univ. of Tsukuba, Japan)

WORKSHOP

"Green Technology"

Organizer: T. Endoh (Tohoku Univ., Japan)
T. Shinada (Waseda Univ., Japan)

Workshop will be held on Tuesday, October 6. Workshop offers advanced discussion on topical device technologies. All presentations are given in English.

Topics:
"Advanced Photovoltaic Cell Technologies and Future Perspectives"
M. Kondo (AIST, Japan)
"Low Power Organic Light Emitting Devices"
C. Adachi (Kyushu Univ., Japan)
"Low Power IC Technology"
T. Kuroda (Keio Univ., Japan)
"Ultra-Low Power IC Technology Integrated with Innovative Materials"
T. Hanyuu (Tohoku Univ., Japan)
"Leading-Edge Power Devices and Future Prospective"
H. Ohashi (AIST, Japan)
"Micro-System Technologies for Energy Saving"
M. Esashi (Tohoku Univ., Japan)

SUBMISSION OF PAPERS

Prospective authors must submit a two-page camera-ready paper with all figures and tables to the conference web site at http://www.ssdm.jp.

Please note that submissions by post will NOT be accepted.

Deadline for Submission is 24:00, May 8, 2009 (Japan time).

The two-page paper must be prepared in English in 8.5- ×11-inch or A4-format and submitted as a PDF file of less than 1 megabyte. The first page must include the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address, and article text. Detailed format information will be posted on the conference web site. Two-byte characters such as Japanese, Chinese, Korean, etc. fonts cannot be used for either figures or texts. The paper should report original, previously unpublished work, including specific results.

Papers to be presented at the conference will be selected by each subcommittee on the basis of suggested areas and content.

Authors of accepted papers will be notified by e-mail before mid-July and requested to give either a 15- to 20-minute oral presentation or a poster presentation.

POSTER SESSIONS

Some of the papers will be presented in the Poster Session. All authors of poster presentations are requested to give a short oral presentation.

EXTENDED ABSTRACTS AND PUBLICATION

Accepted papers will be published, without opportunity for further revision, in the extended abstracts CD-ROM which will be distributed to conference participants during the conference.

SPECIAL ISSUE in JJAP

Authors of papers accepted for presentation at SSDM 2009 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April, 2010.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

LATE NEWS PAPERS

Late news papers describing important new developments may be submitted through the conference web site. A two-page paper must be sent in the same camera-ready format as regular papers. Accepted papers will be included in the extended abstracts.

Late News Papers Deadline is 24:00, July 27, 2009 (Japan time).

Notices of acceptance will be e-mailed in mid-August.

CONFERENCE FORMAT

The conference has been organized to provide as much interaction and discussion among the participants as possible. The program will include plenary sessions, along with technical sessions comprising solicited papers and those submitted for oral or poster presentations.

AWARDS

"SSDM Awards" will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented in or before 2003.

SSDM Paper Award

Given for the best paper presented at the previous year's conference.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at the previous year's conference.

FINANCIAL SUPPORT

Limited financial support will be available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm_secretariat@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

BANQUET

The conference banquet will be held on the evening of Wednesday, October 7. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

REGISTRATION

Participants are required to register online at the conference web site http://www.ssdm.jp, in which the forms for registration, short course, workshop and banquet will be available in the beginning of June, 2009.

The registration fees are:

•Conference

	Registration Fee		Banquet
	Before 24:00, Aug 16 (Japan Time)	After 0:00, Aug. 17 (Japan Time)	
Register	¥50,000	¥55,000	¥7,000
Student	¥20,000		¥4,000
Accompanied person			¥4,000

•Short Course / Workshop

	Short Course (in English)	Work Shop (in English)	Short Course and Work Shop
Register	¥15,000	¥15,000	¥20,000
Student	¥3,000	¥3,000	¥5,000

*Fees include tax.

VISA REQUIREMENT

Overseas participants who require a visa should consult the nearest Japanese Embassy. Please note that obtaining a visa may take much longer than you anticipate, and we strongly recommend that you commence the application process as soon as possible. If your visa application requires an invitation to attend the SSDM conference, please contact SSDM Secretariat, ssdm_secretariat@intergroup.co.jp.(*Invitation letter for visa will be limited issue for only authors whose abstracts are accepted.)

LOCATION

SSDM2009 will be held at Sendai Kokusai Hotel.

4-6-1 Chuo, Aoba-ku, Sendai City, Miyagi
980-0021, Japan

Phone: +81-22-268-1111
Fax: +81-22-268-1113

Sendai Kokusai Hotel is one of the biggest major hotels in Sendai, Japan. The hotel has been greatly contributed with many kinds of international conferences in Sendai. Sendai Kokusai Hotel is located in just 5 munities walk from Sendai Station and 40 munities by taxi from Sendai Airport where the center of Sendai City and its attractions. All the hotel rooms are provided with free Internet access. For further information, see
http://www.tobu-skh.co.jp/

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F
19-2 Kanda-Matsunaga-cho, Chiyoda-ku
Tokyo 101-8641, Japan
Phone: +81-3-5256-1581
Fax: +81-3-5256-1588
E-mail: ssdm2009-gb@or.knt.co.jp

Hotel Accommodations

KNT has blocked rooms at following hotels in Sendai for the conference period.
Reservations can be made through the conference website beginning in June.
If the hotel of your first choice is fully booked, your second choice or a hotel in the same grade will be reserved.

Hotel Name	**Sendai Kokusai Hotel**
Room Rates	Single: ¥10,000 Twin ¥8,500 (per person, per night)
Hotel Deposit	¥15,000
Check-in/out	Check-in: 13:00 / Check-out: 12:00
Address	4-6-1, Chuo, Aoba-ku, Sendai City, Miyagi Pref., 980-0021, Japan
Phone	+81-22-268-1111
Access to Hotel	5 min. walk from JR Sendai Sta.
To Conference site	0 min.

Hotel Name	**Chisun Hotel Sendai**
Room Rates	Single: ¥6,900 (per person, per night)
Hotel Deposit	¥10,000
Check-in/out	Check-in: 15:00 / Check-out: 10:00
Address	4-8-7, Chuo, Aoba-ku, Sendai City, Miyagi Pref., 980-0021, Japan
Phone	+81-22-262-3211
Access to Hotel	5 min. walk from Sendai Sta.
To Conference site	2 min. walk.

Hotel Name	**Hotel Richfield Aoba Do-ri**
Room Rates	Single: ¥7,980 (per person, per night)
Hotel Deposit	¥10,000
Check-in/out	Check-in: 13:00 / Check-out: 11:00
Address	2-3-18 Chuo, Aoba-ku, Sendai City, Miyagi Pref., 980-0021, Japan
Phone	+81-22-262-1355
Access to Hotel	7 min. walk from Sendai Sta.
To Conference site	5 min. walk

Hotel Name	**Hotel Sunroute Sendai**
Room Rates	Single: ¥8,000 (per person, per night)
Hotel Deposit	¥10,000
Check-in/out	Check-in: 14:00 / Check-out: 10:00
Address	4-10-8, Chuo, Aoba-ku, Sendai City, Miyagi Pref. 980-0021, Japan
Phone	+81-22-262-2323
Access to Hotel	5min. walk from Sendai Sta., west exit
To Conference site	3 min. walk

Hotel Name	**Hotel Monterey Sendai**
Room Rates	Single: ¥12,600 (per person, per night)
Hotel Deposit	¥15,000
Check-in/out	Check-in: 14:00 / Check-out: 11:00
Address	4-1-8 Chuo Aoba-ku Sendai City, Miyagi Pref., 980-0021, Japan
Phone	+81-22-265-7110
Access to Hotel	3 min. walk from Sendai Sta.
To Conference site	5 min. walk

Hotel Name	**Hotel Metropolitan Sendai**
Room Rates	Single: ¥13,900 (per person, per night)
Hotel Deposit	¥15,000
Check-in/out	Check-in: 14:00 / Check-out: 12:00
Address	1-1-1, Chuo, Aoba-ku, Sendai City, Pref., 980-8477, Japan
Phone	+81-22-268-2525
Access to Hotel	1min. walk from Sendai Sta.
To Conference site	5 min. walk

Hotel Name	**Sendai Royal Park Hotel**
Room Rates	Single: ¥12,600 Twin: ¥11,550 (per person, per night)
Hotel Deposit	¥15,000
Check-in/out	Check-in: 14:00 / Check-out: 12:00
Address	6-2-1, Teraoka, Izumi-ku, Sendai City, Miyagi Pref., 981-3204, Japan
Phone	+81-22-377-1111
Access to Hotel	30 min. by car from Sendai Sta.
To Conference site	30 min. by car

Notes:

All room rates are per person per night including breakfast, 10% service charge, and consumption tax.

Application and Payment

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website.

The page will be opened in early June and reservations should be made by no later than September 24, 2009 (Japan time).

*Confirmation sheet will be sent by KNT after the application deadline.

Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment.

All payment must be paid only in Japanese yen by one of the following method.

1) Credit Card by Online
(VISA, MasterCard, American Express, Diners Club or JCB only.).
*Please fill in the necessary items in the credit card section of the application form.

2) Bank Transfer:
Sumitomo Mitsui Banking Corp.
Suzuran Branch
SWIFT Code: SMBCJPJT
Account Number: 6103515
Account Name: Kinki Nippon Tourist Co., Ltd.

Cancellation

In case of cancellation, a written notification should be sent to KNT to avoid any troubles.

The cancellation charge are:

Up to 14 days before the arrival date--------- No Charge
13 - 7 days before----------10 % of daily room charge
6 - 2 days before-----------40 % of daily room charge
Less than 2 days, or no notice given-----100% of daily room charge

Refund

Refunds will be made during or after the conference after deducting bank and/or credit card service charges and the cancellation penalties.

If payment was made by credit card, refund will be made to the same credit card.

If the payment was made by bank transfer, please inform us of your bank account.

*Communication fee of 500 JPY is not refundable.

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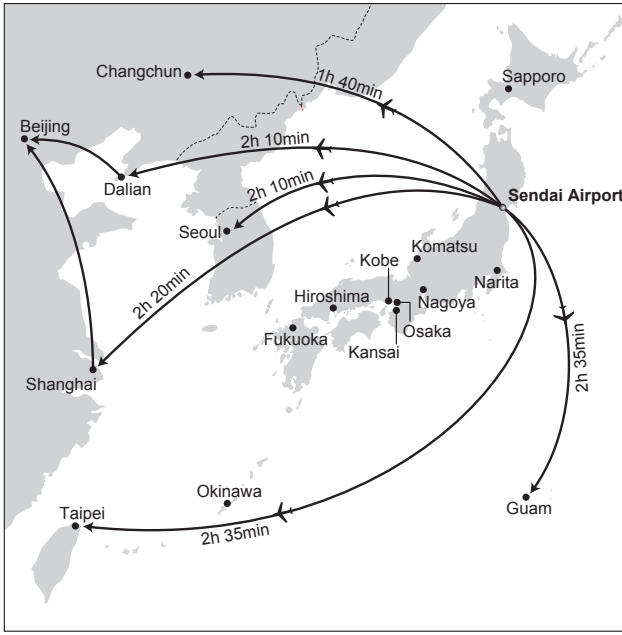
Access to Sendai

Sendai is 350 kilometers north of Tokyo, Japan's capital. If you are coming from abroad, you can fly directly or transfer to a domestic flight to Sendai Airport. You can arrive in Sendai by air or train from any cities in Japan.

Flying in to Sendai Airport from Abroad

Flights to Sendai Airport from overseas are as shown below. Connecting flights from Seoul and China (e.g. Beijing) fly daily to connect Sendai with other countries. Chartered flights fly out of several cities such as Hong Kong and Bangkok. Domestic flights connect ten cities in Japan to Sendai. Passengers landing at Narita, Nagoya or Kansai can transfer to a domestic flight to connect directly to Sendai.



ACCESS TO SENDAI KOKUSAI HOTEL