TECHNICAL PROGRAM

Wednesday, September 22

Opening & Plenary Sessions (Yasuda Auditorium)

Opening Session (10:00-10:30)
Chair: S. Takagi, Univ. of Tokyo

10:00
Welcome Address
Y. Arakawa, Univ. of Tokyo

Award Ceremony

Plenary Sessions (10:30-12:00)
Chair: K. Masu, Tokyo Tech

10:30 PL-1-1
Nanotechnology for Sustainable Society
M. Nakamura, Hitachi Ltd., Japan

The primary role of nanotechnology is to provide disruptive technologies for social sustainability and industrial revitalization. The theme of this presentation is to discuss the future direction of nanotechnology R&D in a global society.

11:15 PL-1-2
More Moore and More Than Moore meeting for 3D in the 21st century
S. Deleonibus, CEA-LETI, France

Co-integrating More than Moore devices with CMOS to interface the outside Multiphysics world brings Functional Diversification. 3D integration will address at wafer level device to packaging technologies capable to reduce cost and improve system performance.

12:00-13:00 Lunch

1F 211

A-1: Organic Device Physics (Area 10)
(13:00-14:15)
Chairs: T. Shimada (Hokkaido Univ.)
M. Nakamura (Chiba Univ.)

13:00 A-1-1 (Invited)
Electronic Structures and Electric Properties of Rubrene Single Crystal Studied By Photoemission, Time-of-Flight, and Displacement Current Measurements
H. Ishii, Chiba Univ. (Japan)
Rubrene single crystal has attracted much attention because it has the highest hole mobility of organic semiconductors so far reported. By overcoming charging problem by laser irradiation, we have succeeded to directly observe the band-dispersion relation. On the basis of the photoemission results as well as time-of-flight mobility measurement, the carrier transport mechanism will be discussed.

13:30 A-1-2
Carrier Propagation Dependence on Applied Potentials in Pentacene OFET Investigated by Impedance Spectroscopy and Electrical Time-of-Flight Techniques
J. Lin[1], M. Weis[2], D. Taguchi[1], T. Manaka[1] and M. Iwamoto[1], [1]Tokyo Tech and [2]Slovak Aca. Sci (Japan)
Impedance spectroscopy and electrical time-of-flight techniques were used for the evaluation of carrier propagation dependence on various applied potentials in a pentacene OFET. These techniques are based on carrier propagation, thus isolates the effect of charge density. The results agree well with our developed model.

1F 212

B-1: Ge MOS Technology 1 (Area 1)
(13:00-14:10)
Chairs: J. Yugami (Renesas Electronics Corp.)
O. Nakatsuka (Nagoya Univ.)

13:00 B-1-1 (Invited)
Defect-Free GOI (Ge on Insulator) by SiGe Mixing-Triggered Liquid-Phase Epitaxy
M. Miyao[1], K. Toko[1,2], M. Kurosawa[1,2] and T. Sadoh[1,2], [1]Kyushu Univ. and [2]JSPS (Japan)
The present paper reviews our recent progress in the novel GOI growth technique. Following subjects will be discussed: (1) Basic idea for SiGe mixing-triggered rapid melting growth, (2) Defect-free giant GOI (~1 cm length) with high carrier mobility (~ 1200 cm2/Vs), (3) Possible application to 3D-LSI, thin film transistors, and spin-transistors.

13:30 B-1-2
Advantage of High-pressure Oxidation for Ge/GeO_2 Stack Formation
C. H. Lee[1], T. Nishimura[1,2], T. Tabata[1], S. Wang[1], K. Nagashio[1,2], K. Kita[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
The PDA for Ge/GeO2 stack has been systematically investigated, and it has been revealed that LOA is quite important for passivating Ge/GeO2 interface. However, GeO2 bulk properties are different between APO- and HPO-grown GeO2 films.

1F 213

C-1: Low Frequency Noise (Area 3)
(13:00-14:20)
Chairs: T. Hiramoto (Univ. of Tokyo)
T. Tanaka (Fujitsu Semiconductor Ltd.)

13:00 C-1-1
Contributions of Interface-Trap and Minority-Carrier Responses to C-V characteristics of Al_2O_3/InGaAs Capacitors
Y, Urabe[1], N. Miyata[1], T. Yasuda[1], H. Yamada[2], M. Hata[2], N. Taoka[3], T. Hoshii[3], M. Takenaka[3] and S. Takagi[3], [1]AIST, [2]Sumitomo Chemical Co., Ltd. and [3]Univ. of Tokyo (Japan)
We clarified the contribution of minority-carrier response to the C-V and conductance characteristics of ALD-Al_2O3/InGaAs MIS capacitor using the temperature-dependent measurement. As a result, we found that the Gp/ω ridge structure measured at -50°C is mainly composed of the interface-trap responses.

13:20 C-1-2
New Insights into Flicker Noise Improvement Mechanism Using Random Telegraph Signal Technique
T. L. Li, S. Y. Huang, B. Hung, C. Y. Tzeng and S. Chou, United Microelectronics Corp. (Taiwan)
This work demonstrated that the improvement of low-frequency noise using F-incorporation and H2-sintering can be attributed to the relaxed trap-to-carrier influence and reduced trap density, respectively.

2F 221

D-1: Nonlinear Optics (Area 7)
(13:00-14:15)
Chairs: K. Akiyama (Mitsubishi Electric Corp.)
H. Yamada (Tohoku Univ.)

13:00 D-1-1 (Invited)
Roadmap of ultrafast energy-saving optical semiconductor devices to Year 2025
Y. Ueno, Univ. of Electro-Communications (Japan)
Evolution in energy efficiency of many-core parallel processors through year 2025 looks unclear, because the serial speed of new electronic cores has stopped to evolve. With reviewing application-research activities in opto-electronics, instead, the author estimates what possibilities the still-crude 100-times-faster serial processors (e.g. 200-Gb/s) will contribute through year 2025.

13:30 D-1-2
Quasi-Phase-Matched Difference Frequency Generation at 3.4 µm in High-Quality GaAs/AlGaAs Waveguides
K. Hanashima, I. Ohta, J. Ota, T. Matsushita and T. Kondo, Univ. of Tokyo (Japan)
We have succeeded in fabricating high-quality periodically-inverted GaAs/AlGaAs waveguides, and achieved the lowest propagation loss ever reported and reasonable high efficiency in quasi-phase matched difference frequency generation at 3.4 µm.

4F 241

E-1: DRAM (Area 4)
(13:00-14:20)
Chairs: K. Hamada (Elpida Memory, Inc.)
S. Miura (NEC Corp.)

13:00 E-1-1
Performance Improvement of a Novel Capacitor-less 1T-DRAM Based on a Lateral p Type Doped Region
G. Guegan[1], G. Molas[1], S. Puget[2] and C. Raynaud[1], [1]CEA-LETI/MINATEC and [2]STMicroelectronics (France)
A novel architecture is proposed on a standard PD-SOI in order to facilitate the formation of a deep body potential. This new device with significant memory performance improvement, is a promising candidate for future embedded 1T-DRAM.

13:20 E-1-2
Characterization of junctionless Z-RAM cell
C. W. Lee[1], S. Okhonin[2], M. Nagoya[2], A. Kranti[1], I. Ferain[1], N. Dehdashti Akhavan[1], P. Razavi[1], R. Yu[1], R. Yan[1] and J. P. Colinge[1], [1]Tyndall National Inst. and [2]Innovative Silicon (Ireland)
We fabricated the silicon nanowire JunctionLess(JL) proposed for capacitorless 1T DRAM. The JL-MuGFET has more advantage such as a very low leakage current, a low turn-on voltage, extremely easy processing. We believe that this JL based Z-RAM memory will use in sub-nano scale regime.

4F 242

F-1: Graphene Structures and Transport (Area 9)
(13:00-14:15)
Chairs: T. Machida (Univ. of Tokyo)
Y. Kawano (RIKEN)

13:00 F-1-1 (Invited)
STS Observations of Topological Dirac Fermion on Graphite Surafaces
T. Matsui, K. Tagami, M. Tsukada and H. Fukuyama, [1]Univ. of Tokyo and [2]Advanced Coropration (Japan)
Surface states of graphite in magnetic field were studied both theoretically and experimentally with scanning tunneling spectroscopy to show that the property of massless Dirac fermion in Graphene is appeared on graphite surfaces.

13:30 F-1-2 (Invited)
Electronic Transport Properties in Graphene Nanoribbons and Junctions
K. Wakabayashi[1,2], [1]NIMS and [2]PRESTO, JST (Japan)
We focus theoretically on the electronic transport properties of graphene nanoribbons and nanojunctions. The presence of a perfectly conducting channel in disordered graphene nanoribbons is pointed out. Nanojunctions are shown to have the zero-conductance anti-resoances associated with the edge states. The condition of the resonances is discussed.

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12:00-13:00 Lunch

4F 243

G-1: RF Circuits and Systems (1) (Area 5)
(13:00-14:10)
Chairs: M. Ikebe (Hokkaido Univ.)
H. Takao (Kagawa Univ.)

13:00 G-1-1 (Invited)
Evolution of Transceiver Architectures toward Software-Defined and Cognitive Radios
T. Tsukahara, T. Tsushima and H. Ito, Univ. of Aizu (Japan)
The evolution of CMOS transceiver architectures is described, especially focusing on SDR and CR applications. After explaining some examples of transceiver designs, we propose a high-precision complex quadrature modulator suitable for SDR and CR transmitters. It features an inherent correction mechanism of phase and amplitude errors.

13:30 G-1-2
A 6-10 GHz CMOS Tunable Power Amplifier for Reconfigurable RF Transceivers
J. Y. Hong, D. Imanishi, K. Okada and A. Matsuzawa, Tokyo Tech (Japan)
A CMOS power amplifier with a tunable output impedance matching is proposed for a multi-standard transceiver that operates at frequency band from 6 to 10GHz. The output 1-dB compression point, saturated output power and maximum PAE are larger than 15.5.dBm, 19.8dBm and 7.1%, respectively.

4F 244

H-1: New Functional Materials (Area 8)
(13:00-14:15)
Chairs: H. Hibino (NTT Basic Res. Labs.)
B. H. Hong (Korea Univ.)

13:00 H-1-1 (Invited)
Let us update the present status of research on magnetic semiconductors
H. Munekata, Tokyo Tech (Japan)
Present status at to research on III-V-based, oxide-based, and group-IV based magnetic semiconductors will be discussed, together with potential, future applications which may not be restricted within the limit of devices for electrical computers.

13:30 H-1-2
In situ Observation of Fe growth on GaAs(001) and InAs(001) by X-ray diffraction
S. Fujikawa and M. Takahasi, JAEA (Japan)
We evaluated Fe films on GaAs(001) and InAs(001) by in-situ X-ray diffraction measurements with increasing Fe thickness. While the Fe/InAs was strained even at 30 ML, Fe/GaAs was already relaxed at 4 ML.

4F 245

I-1: III-V High-Speed and High-FrequencyTransistors (Area 6)
(13:00-14:15)
Chairs: S. Tanaka (Shibaura Inst. of Tech.)
S. Yamahata (NTT Corp.)

13:00 I-1-1 (Invited)
Adding Value to CMOS through Heterogeneous Integration
Y. Royter, P. R.. Patterson, J. C. Li, K. R. Elliot, T. Hussain, M. F. Boag-O'Brien, J. R. Duvall, M. C. Montes, D. A. Hitko, M. Sokolich, D. H. Chow and P. D. Brewer, HRL Laboratories, LLC (USA)
Technology capable of wafer-scale device-level integration of InP HBTs and CMOS has been developed, making full simultaneous utilization of III-V device speed and CMOS circuit complexity possible. Resulting circuits maintain maximum CMOS integration density and HBT performance without significant CMOS or HBT degradation, and produce high yield heterogeneous interconnects with < 5um length.

13:30 I-1-2
InP/InGaAs MOSFET with Back-Electrode Structure Bonded on Si Substrate Using a BCB Adhesive Layer
T. Kanazawa, R. Terao, Y. Yamaguchi, S. Ikeda, Y. Yanai and Y. Miyamoto, Tokyo Tech (Japan)
We demonstrated InP/InGaAs/InP channel MOSFET with a back-metal gate on Si using the BCB bonding. In the I-V measurement with dual-gate operation, the drain current of 880 mA/mm and transconductance of 450 mS/mm were achieved.

4F 246

J-1: Carbon Nanotube Devices (Area 13)
(13:00-14:15)
Chairs: Y. Ohno (Nagoya Univ.)
S. Suzuki (NTT Corp.)

13:00 J-1-1 (Invited)
Synthesis and dry depositon of SWCNT networks for flexible, transparent conductors and field effect transistors
A. Kaskela[1], A. G. Nashibulin[1], M. Y, Zavodchikova[1], B. Aitchison[2], Y. Tian[1], Z. Zhu[1], H. Jiang[1], D. P. Brown[2] and E. I. Kauppinen[1], [1]Aalto University and [2]Canatu Oy (FINLAND)
We present the floating Fe catalyst synthesis of high quality SWCNTs from CO. Methods for SWCNT dry deposition onto polymeric substrates at ambient temperature to manufacture transparent thin film FETs and conducting films are discussed.

13:30 J-1-2
Characterization of Carbon Nanotube Thin Film Transistors by Scanning Probe Microscopy
Y. Okigawa, Y. Ohno, S. Kishimoto and T. Mizutani, Nagoya Univ. (Japan)
We measured carbon nanotube (CNT) - thin-film transistors in detail by Kelvin probe force microscopy, point-contact current-imaging AFM, and scanning gate microscopy. Non uniform images which correlated each other ware obtained even in the randomly- oriented 2D networks of CNTs.

2F 222

K-1: Modeling of Power LDMOSFET (Area 14)
(13:30-14:00)
Chairs: T. S. Chow
(Rensselaer Polytechnic Institute)
M. Ishiko (Toyota Central R&D Labs., Inc.)

13:45 K-1-2
Modeling of RESURF LDMOS for Accurate Prediction of Junction Condition on Device Characteristics
T. Saito[1,2], T. Tanaka[1], T. Hayashi, K. Kikuchihara, T. Kanamoto, [2]H. Masuda, M. Miyake, [1]S. Amakawa, H. J. Mattausch and M. Miura-Mattausch, [1]Renesas Electronics Corp. and [2]Hiroshima Univ. (Japan)
The compact model for high-voltage MOSFETs HiSIM_HV was extended to RESURF structure. The model considers the influence of the dynamically varying depletion width at the drain/substrate junction, causing the resistance modification and the expansion effect of impact ionization.

2F 223

L-1: Biosensors (Area 11)
(13:00-14:15)
Chairs: K. Ajito (NTT Corp.)
S. Contera (Univ. of Oxford)

13:00 L-1-1 (Invited)
Detection of biomolecular recognition using Bio-transistors
Y. Miyahara, C. Hamai-Kataoka, A. Matsumoto T. Goda and Y. Maeda, NIMS (Japan)
We have been investigating direct interaction between biomolecular charges and charged carriers in semiconductor materials. Field effect transistors have been used to detect biomolecular recognition based on electrostatic interaction. The platform based on the bio-transistors is suitable for a simple and inexpensive system for clinical research and diagnostics.

13:30 L-1-2
Sensitivity Improvement of Biosensors Using Si Ring Optical Resonators
M. Fukuyama, Y. Amemiya, Y. Abe, Y. Onishi, A. Hirowatari, K. Terao, T. Ikeda, A. Kuroda and S. Yokoyama, Hiroshima Univ. (Japan)
The sensitivity of antigen detection using Si ring optical resonators is found to be in the order of 10-6 g/ml. Using the variety of approach it was suggested that the sensitivity of the biosensor will be improved by factor of 100. Then the practical Si ring biosensor will be realized.

Wednesday, September 22

1F 211

A-1: Organic Device Physics (Area 10)

13:45 A-1-3
Transient Absorption Decay Characteristics at Visible Wavelength Region for NMe$_2$-Silole:Fluorene Blend Film
T. Fukuda[1], A. Furube[2], R. Kobayashi[1], N. Kamata[1] and K. Hatano[1], [1]Saitama Univ. and [2]AIST (Japan)
We investigated charge carrier dynamics in a silole doped F8BT blend film by measuring transient absorption decay at a visible wavelength region. The transient absorption characteristics are useful to understand carrier dynamics in organic material, and they were measured by femtosecond pump-probe technique.

14:00 A-1-4
Computational Analysis of Electron Injection on Light-Emitting Polymer/Cathode Interface
I. Yamashita, H. Onuma, R. Nagumo, R. Miura, A. Suzuki, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo and A. Miyamoto, Tohoku Univ. (Japan)
We simulated the electron injection on the light-emitting polymer/cathode interface by using a quantum chemistry calculation and Monte Carlo method. We investigated the relationship between structure of the interface and electron injection properties.

1F 212

B-1: Ge MOS Technolosy 1 (Area 1)

13:50 B-1-3
Nature of Interface Traps in Ge MIS Structures with GeO$_2$ Interfacial Layers
N. Taoka[1], W. Mizubayashi[1], Y. Morita[1], S. Migita[1], H. Ota[1] and S. Takagi[1,2], [1]MIRAI-NIRC and [2]Univ. of Tokyo (Japan)
Ge MIS interface properties with GeO2 interfacial layers have been systematically investigated. It is found that the natures of the interface traps depend on oxidation temperatures, and that acceptor-like traps are widely distributed in bandgap.

1F 213

C-1: Low Frequency Noise (Area 3)

13:40 C-1-3
Drastic reduction of the low frequency noise in Si(100) p-MOSFETs
P. Gaubert, A. Teramoto, R. Kuroda, Y. Nakao, H. Tanaka and T. Ohmi, Tohoku Univ. (Japan)
On the account of new fabrication processes, we demonstrate in this paper that very efficient ways for reducing the 1/f noise in MOSFETs have been achieved. Moreover, a drop down to almost 4 decades can be expected regarding the Si(100) p-MOSFETs.

14:00 C-1-4
Layout Dependent STI Stress Effect on High Frequency Performance and Flicker Noise in Nanoscale CMOS Devices
K. L. Yeh, C. Y. Ku and J. C. Guo, National Chiao Tung Univ. (Taiwan)
The impact of MOSFET layout dependent stress on high frequency performance and flicker noise is investigated. Donut MOSFETs, attributed to the suppression of STI transverse stress and excess traps can realize the lowest flicker noise and improved f$_T$.

2F 221

D-1: Nonlinear Optics (Area 7)

13:45 D-1-3
Experimental Observation of Self-Phase Modulation in ZnO Channel Waveguides
E. Y. Morales Teraoka[1], D. H. Broaddus[2], T. Kita[1], A. Tsukazaki[1,3], M. Kawasaki[1,3,4], A. L. Gaeta[2] and H. Yamada[1], [1]Tohoku Univ., [2]Cornell Univ., [3]PRESTO, Japan Science and Technology Agency, [4]WPI Advanced Institute for Materials Research and [5]CRESTO, Japan Science and Technology Agency (Japan)
We demonstrate spectral broadening of femtosecond pulses due to SPM in the fabricated ZnO waveguides. Using the obtained measurements, we estimate the nonlinear strength parameter and the nonlinear refractive index.

14:00 D-1-4
Remarkable Enhancement of Optical Kerr Signal by increasing Quality Factor in a GaAs/AlAs Multilayer Cavity
K. Morita, T. Takahashi, T. Kitada and T. Isu, Univ. of Tokushima (Japan)
The spectral widths of the laser pulses were tuned to the cavity modes and the Q dependent optical Kerr signal was investigated using GaAs/AlAs multilayer cavity structure. We have revealed that the optical Kerr signal was remarkably enhanced by Q (proportional to Q4) in our cavity.

4F 241

E-1: DRAM (Area 4)
(13:00-14:20)

13:40 E-1-3
A Study of a Data Retention Characteristic for Various Schemes of Gate Oxide Formation in Sub-50-nm Saddle-Fin Transistor DRAM Technology
S. W. Ryu, S. K. Chun, T. Jang, B. Lee, D. Lee, M. Yoo, S. Cha, J. G. Jeong and S. J. Hong, Hynix Semiconductor Inc. (Korea)
A data retention characteristic has been investigated for different gate oxide formation schemes with saddle-Fin transistor DRAM. It was confirmed that the Interface traps by charge pumping method strongly affected the data retention time.

14:00 E-1-4
An analysis of Conduction Mechanism and Reliability Characteristics of MIM Capacitor with Single ZrO$_2$ Layer
H. M. Kwon[1], I. S. Han[1], S. U. Park[1], J. D. Bok[1], Y. J. Jung[1], H. S. Shin[1], C. Y. Kang[2], B. H. Lee[3], R. Jammy[2] and H. D. Lee[1], [1]Chungnam National Univ., [2]SEMATECH and [3]GIST (Korea)
In this paper, current transport mechanism and reliability of MIM capacitor with single zirconium oxide layer are characterized in depth.

4F 242

F-1: Graphene Structures and Transport (Area 9)

14:00 F-1-3
Field-Effect in Multiple Graphene Layer Structures
M. Ryzhii[1,3], T. Otsuji[2,3], V. Mitin[4], M. S. Shur[5] and V. Ryzhii[1,3], [1]Univ. of Aizu, [2]Tohoku Univ., [3]J. Sci. Technol. Agency, [4]Univ. at Buffalo and [5]Rensselaer Polytech. Inst. (Japan)
The field effect in gated multiple-graphene layer structures is studied. The distributions of the potential, Fermi energy, and electron density over the graphene layers are calculated.

Coffee Break (2F Forum)

A-2: Electric Characterization of Organic Semiconductors (Area 10)
(14:45-15:45)
Chairs: M. Yoshida (AIST)
E. Itoh (Shinshu Univ.)

14:45 A-2-1 (Invited)
Non-Contact Measurement of Charge Carrier Mobility in Inorganic and Organic Semiconductor Materials
S. Seki[1,2], A. Asano, Y. Honsho[1] and A. Saeki[1,2], [1]Osaka Univ. and [2]PRESTO, JST (Japan)
Intrinsic charge carrier mobility in inorganic and organic semiconductor materials is determined by non-contact microwave measurement technique as the short-range transport properties of charge carriers, and discussed in relation to the values by several conventional techniques.

15:15 A-2-2
Probing of Transient Electric Field Distribution in ITO/PI/P3HT/Au Using Time-Resolved Second Harmonic Generation Measurement
R. Miyazawa, D. Taguchi, T. Manaka and M. Iwamoto, Tokyo Tech (Japan)
The discovery of highly conducting organic materials, e.g., pentacene, polythiophene, etc. has resulted in studies of their possible application to organic electronics devices, such as organic electroluminescent devices (OLEDs), organic solar cells and organic field-effect transistors (OFETs).

B-2: Ge MOS Technology 2 (Area 1)
(14:45-16:05)
Chairs: S. Miyazaki (Nagoya Univ.)
T. Nabatame (NIMS)

14:45 B-2-1
Effects of GeO$_2$-Metal Interaction on V$_{FB}$ of GeO^2 MIS Gate Stacks
F. I. Alzakia[1], K. Kita[1,2], T. Nishimura[1,2], k. Nagashio[1,2] and A. ToriumiToriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
The flatband voltages (VFB) of GeO2 gate stacks with various metals have been investigated. The metal-GeO2 interaction, which is pronounced for high work function metals, significantly affects the VFB of GeO2 MIS stacks.

15:05 B-2-2
Single-Crystalline (100) Ge Stripes with High Mobilities Formed on Insulating Substrates by Rapid-Melting-Growth with Artificial Single-Crystal Si Seeds
K. Toko, T. Sakane, H. Yokoyama, M. Kurosawa, T. Sadoh and M. Miyao, Kyushu Univ. (Japan)
Orientations of single-crystal Ge stripes are controlled to (100) planes on insulating substrates by SiGe-mixing triggered melting-growth combined with the Si (100) micro-seed technique. In addition, defect-free Ge with the high hole mobility is demonstrated.

C-2: Transport Physics (Area 3)
(14:45-16:05)
Chairs: Y. Nishida (Renesas Electronics Corp.)
N. Mori (Osaka Univ.)

14:45 C-2-1
Abrupt Source Heterostructures with Lateral-Relaxed/Strained Layers for Quasi-Ballistic CMOS Transistors using Lateral Strain Control Technique of Strained Substrates
T. Mizuno[1,2], M. Hasegawa[1], K. Ikeda[3], M. Nojiri[4] and T. Horikawa[2], [1]Kanagawa Univ., [2]MIRAI-NIRC, [3]MIRAI-Toshiba and [4]AIST (Japan)
We have experimentally studied abrupt source relaxed-/strained-layers heterojunction structures for quasi-ballistic CMOS, by a local O+ ion implantation induced relaxation technique of strained substrates with SiO2 mask patterns.

15:05 C-2-2
Impact of Transistor Layout Configuration on Current Drive Performance in (100)/<110> and (100)/<100> SiGe channel pMOSFETs: Comparative Study to Si channel
K. Nakatsuka, H. Okamoto, H. Itokawa, K. Okano, T. Izumida, M. Kondo, T. Morooka, I. Mizushima, A. Azuma, N. Aoki, S. Inaba and Y. Toyoshima, Toshiba Corp. (Japan)
We systematically studied the mobility modulation by transistor layout configuration in Si and SiGe channel pMOSFETs, and found that hole mobility in <100>/(100) channel SiGe is the highest in short and narrow channel pMOSFETs.

D-2: Advanced Design and Measurement (Area 7)
(14:45-15:45)
Chairs: H. Yamada (Tohoku Univ.)
K. Akiyama (Mitsubishi Electric Corp.)

14:45 D-2-1
Time-Resolved Measurements on Sum Frequency Generation Strongly Enhanced in (113)B GaAs/AlAs Coupled Multilayer Cavity
F. Tanaka, T. Takimoto, K. Morita, T. Kitada and T. Isu, Univ. of Tokushima (Japan)
In this study, strong SFG from the (113)B coupled multilayer cavity was confirmed to originate from the interference between the enhanced internal light electric fields of the cavity modes by time-resolved measurements.

15:00 D-2-2
Development of half-cladding semiconductor photonic device structure for surface transmission of light waves
N. Yamamoto[1], D. Murakami[2], H. Fujioka[2], K. Akahane[1], T. Kawanishi, H. Sotobayashi[3] and H. Takai[2], [1]NICT, [2]Tokyo Denki Univ. and [3]Aoyama Gakuin Univ. (Japan)
We propose a half-cladding semiconductor laser (HaCL) structure to achieve a surface transmission of light-waves in the novel photonic device. A light emission from the fabricated HaCL structure is successfully demonstrated under the current injection.

E-2: Flash Memory Ⅰ (Area 4)
(14:45-16:05)
Chairs: T. Endoh (Tohoku University)
E. Yang (eMemory Technology Inc.)

14:45 E-2-1
Improvement of Data Retention in NAND Flash Memory for beyond 3x nm using HTO Liner and IPD Thickness Optimization
J. S. Leem, J. Seo, B. K. Kim, K. S. Kim, H. H. Chang, K. O. Ahn, S. K. Lee and S. J. Hong, Hynix Semiconductor Inc. (Korea)
In this paper, we present our results on how to improve reliability with optimizing mechanical stress in active and interpoly dielectrics thickness, and confirmed the results through various simulations and test methods on 41nm NAND technology.

F-2: Novel Structures (Area 9)
(14:45-16:00)
Chairs: T. Matsui (Univ. of Tokyo)
K. Wakabayashi (NIMS)

14:45 F-2-1
Piezoelectric control of coupled vibration in elastically coupled nanomechanical oscillators
H. Okamoto[1], C. Y. Chang[1,2], K. Onomitsu[1], E. Y. Chang[2] and H. Yamaguchi[1], [1]NTT Basic Res. Labs. and [2]National Chiao Tung Univ. (Japan)
We have demonstrated all-piezoelectric operation of coupled nanomechanical oscillators at room temperature. We will be able to use the piezoelectric control of coupled vibration for applications of coupled nanomechanical oscillators, such as highly sensitive sensors.

15:00 F-2-2
Ge nanowires for nanoscale nonvolatile memory applications
S. Maikap[1], S. Majumdar[1,2], W. Banerjee[1], S. Mondal[1], S. Manna[2] and S. K. Ray[2], [1]Chang Gung Univ. and [2]Indian Institute of Technology, Kharagpur (Taiwan)
The Ge nanowires are prepared by VLS method. A broad peak in photoluminescence spectrum is due to germanium-oxygen vacancies. Good flash and resistive memory devices are obtained using Ge nanowire MOS structure for the first time.

Wednesday, September 22

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G-1: RF Circuits and systems (1) (Area 5)

13:50 G-1-3
RF Signal Generator Based on Time-to-Analog Converter Using Multi-Ring Oscillators in 90nm CMOS
K. Nakano, S. Amakawa, N. Ishihara and K. Masu, Tokyo Tech (Japan)
In this paper, a scalable wideband RF signal generator that uses a time-to-analog conversion technique using multi-ring oscillators is proposed and confirmed by fabricating a chip using 90nm CMOS.

4F 244

H-1: New Functional Materials (Area 8)

13:45 H-1-3
Luminescence Characteristics and Annealing Effect of Tb-doped AlBNO Films for Inorganic Electroluminescence Devices
K. Masumoto[1], A. Semba[1], C. Kimura[1], T. Taniguchi[2], K. Watanabe[2] and H. Aoki[1], [1]Osaka Univ. and [2]National Inst. for Materials Sci. (Japan)
Inorganic electroluminescence devices have attracted attention owing to their application in low-power-consumption displays. However, the operating voltage is very high. To lower the operating voltage, we have investigated Tb-doped AlBNO films as the luminescence layer.

14:00 H-1-4
Influence of Nitrogen Doping on the LaAlO Film Properties
M. Honjo, N. Komatsu, C. Kimura and H. Aoki, Osaka Univ. (Japan)
We have investigated the influence on the electrical and optical properties of the LaAlON (N: 0-4%) films of nitrogen doping as a way of improving the water resistance.

4F 245

I-1: III-V High-Speed and High-Frequency Transistors (Area 6)

13:45 I-1-3
Source/Drain Engineering for $In_{0.7}Ga_{0.3}As$ N-MOSFETs: Raised Source/Drain with *In Situ* Doping for Series Resistance Reduction
X. Gong[1], H.C. Chin[1], S.M. Koh[1], L. Wang[1], Ivana[1], Z. Zhu[1], B. Wang[2], C.K. Chia[2] and Y.C. Yeo[1], [1]National Univ. of Singapore and [2]Inst. of Materials Res. and Engineering, Agency for Sci. Tech. and Res. (Singapore)
We report the first demonstration of $In_{0.7}Ga_{0.3}As$ N-MOSFETs with in situ doped raised source/drain (S/D) regions. By using the new S/D architecture, a ~30% reduction in series resistance Rs can be obtained, leading to enhancement in I_{Dsat} of the $In_{0.7}Ga_{0.3}As$ N-MOSFETs.

14:00 I-1-4
A sub 350°C GaSb pMOSFET with ALD high-k dielectric
A. Nainani, T. Irisawa, Y. Sun, F. Crnogorac and K. Saraswat, Stanford Univ. (USA)
Bandgap & offsets for ALD Al_2O_3 on GaSb are calculated using SRPES. Interface characteristics are investigated using C/G-V. p+/n diode with ION/IOFF > 5E4 is developed. Finally, output characteristics on self-aligned GaSb-pMOSFET are presented.

4F 246

J-1: Carbon Nanotube Devices (Area 13)

13:45 J-1-3
Study on Device Parameters of Carbon Nanotube FETs to Realize Steep Subthreshold Slope of less than 60 mV/decade
B. P. Algul[1], T. Kodera[2], S. Oda[2] and K. Uchida[1], [1]Tokyo Tech and [2]QNERC (Japan)
In carbon nanotube FETs (CNFETs) device parameters to observe subthreshold slope (SS) of less than 60 mV/dec have been studied. It is demonstrated, for the first time, that band-to-band tunneling (BTBT) current can be greatly enhanced by reducing the thickness of inter-layer oxide (t_{int}) between substrate and CNT.

14:00 J-1-4
Metal-Catalyst-Free Growth of Carbon Nanotubes for CMOS Integration
T. Uchino[1], G. N. Ayre[1], D. C. Smith[1], J. L. Hutchison[2], C. H. de Groot[1] and P. Ashburn[1], [1]Univ. of Southampton and [2]Univ.of Oxford (UK)
Metal-catalyst-free growth of carbon nanotube (CNT) on SiO_2 using a thin Ge film is reported for the first time. This growth process is used to produce back gate CNTFETs with Pd source/drain contacts.

2F 222

K-1: Modeling of Power LDMOSFET (Area 14)

2F 223

L-1: Biosensors (Area 11)

13:45 L-1-3
Fast DNA sequencing with nanopore-embedded graphene electrodes
Y. He[1], R. H. Scheicher[2], A. Grigoriev[2], R. Ahuja[2,3], S. Long[1], Z. Ji[1], Z. Yu[1] and M. Liu[1], [1]Laboratory of nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, [2]Condensed Matter Theory Group, Department of Physics and Astronomy, Uppsala University and [3]Applied Materials Physics, Department of Materials and Engineering, Royal Institute of Technology (China)
We set up model and perform simulation of DNA sequencing with nanopore-embedded graphene nanoelectrodes. Simulation results show that compared to sequencing with gold nanoelectrodes, much improved discrimination of different nucleotides and single-base resolution are achieved. The achieved results can provide a design guide for future realization of nanopore-based electrical DNA sequencing.

14:00 L-1-4
Poly Crystalline Silicon Nanowire Field-Effect Transistor for Real-Time Detection of Influenza Virus DNA
C. Y. Hsiao[1], W. T. Lai[1], M. P. Lu[2] and Y. S. Yang[1,2], [1]National Chiao Tung Univ. and [2]National Nano Device Labs. (Taiwan)
Real-time detection of avian influenza H5 virus DNA using complementary captured DNA probe modified poly crystalline nanowire field-effect transistor was demonstrated. The result indicated that a simple, quick, and high sensitive biosensor can be developed.

Coffee Break (2F Forum)

G-2: RF Circuits and Systems (2) (Area 5)
(14:45-16:05)
Chairs: H. Takao (Kagawa Univ.)
M. Ikebe (Hokkaido Univ.)

14:45 G-2-1
A 5.4-9.2 GHz 19.5 dB CMOS UWB Receiver Frontend Low Noise Amplifier for Confocal Imaging System
A. Azhari, S. Kubota, A. Toya, N. Sasaki and T. Kikkawa, Hiroshima Univ. (Japan)
A 5.4-9.2 GHz CMOS LNA for UWB wireless communication with 19.5 dB power gain and 3.5 dB noise figure is presented. Wireless communication of Gaussian monocycle pulse by horn antennas and LNA is also investigated.

15:05 G-2-2
Confocal Imaging System Using 28.2 Gsample/s UWB Sampling Circuit
A. Toya, N. Sasaki, S. Kubota and T. Kikkawa, Hiroshima Univ. (Japan)
A confocal imaging technique was presented for detecting a target. To realize the technique in CMOS, a high-sampling rate sampling circuit is required. Here, we adopted the 28.2 GSample/s sampling circuit with an improved multiplexer.

H-2: Growth of Grapheme for Electronics Applications (Area 8)
(14:45-16:00)
Chairs: H. Hibino (NTT Basic Res. Labs.)
H. Munekata (Tokyo Tech)

14:45 H-2-1 (Invited)
Towards Industrial Applications of Graphene Electrodes
B. H. Hong, Sungkyunkwan Univ. (Korea)
We introduce ultra-large scale (~30 inch) synthesis, roll-to-roll transfer, and chemical doping of graphene films showing excellent electrical and physical properties suitable for practical applications.

15:15 H-2-2
Uniformity of Graphene CVD Growth Depending on the Thickness and Domain Structure of Epitaxial Metal Films
S. Yoshii, K. Nozawa, K. Toyoda and N. Matsukawa, Panasonic Corp. (Japan)
We investigated the graphene growth on epitaxial Ni, Ru and Co films. Locally enhanced segregation at grain boundary was found to be one of the major sources of non-uniformity. Uniform graphene growth was achieved with a single domain thin Ru film, in which grain boundaries were eliminated and segregation was suppressed.

I-2: GaN HEMTs (Area 8)
(14:45-16:00)
Chairs: Y. Ohno (Univ. of Tokushima)
S. Kuroda (Sumitomo Electric Device Innovations, Inc.)

14:45 I-2-1 (Invited)
Integration Technologies for GaN Power Transistors
T. Ueda, T. Tanaka and D. Ueda, Panasonic Corp. (Japan)
Newly developed technologies for mono-lithic integration of GaN power switching transistors are reviewed. The topics include the world first GaN-based inverter IC, a novel chip layout eliminating undesired surface flashover to achieve high breakdown voltages with low on-state resistances.

15:15 I-2-2
High-Gain and High-Bandwidth AlGaN/GaN HEMT Comparator
A. M. H. Kwan, K. Y. Wong, X. Liu and K. J. Chen, Hong Kong Univ. of Sci. and Tech. (Hong Kong)
The dynamic response of AlGaN/GaN HEMT voltage comparator was characterized. This comparator with active load demonstrates superior performance of high gain (>31dB) and wide bandwidth (>4MHz), and small propagation delay time (<20ns) over a wide range of temperatures up to 250 deg C.

J-2: Carbon Nanotube Properties and Transport (Area 13)
(14:45-16:00)
Chairs: S. Sato (AIST)
S. Akita (Osaka Prefecture Univ.)

14:45 J-2-1
Single Wall Carbon Nanotube Growth from Boron- and Nitrogen-Containing Feedstocks
S. Suzuki and H. Hibino, NTT Corp. (Japan)
BN-doped SWCNTs were successfully grown by thermal CVD method. Blueshifts of Raman spectra were clearly observed, which is an indication of considerable carrier doping. Our results indicate the possibility of both bandgap tuning and carrier doping of SWNTs.

15:00 J-2-2
Transient thermal response of an individual carbon nanotube
Y. Ohshima, T. Arie and S. Akita, Osaka Prefecture Univ. (Japan)
We have investigated the transient thermal response of an individual MWNT under the Joule heating. The suspended MWNT showed the response time within 100 ns corresponding to the transient properties of the electrical input power.

K-2: Power Module Technology (Area 14)
(14:45-15:45)
Chairs: T. Shinohe (Toshiba Corp.)
S. Matsumoto (Kyushu Inst. of Tech.)

14:45 K-2-1 (Invited)
High Performance Silicon Carbide Power Modules for Extreme Environment Applications
A. B. Lostetter, J. Hornberger, B. McPherson, R. Shaw, B. Reese and M. Schupbach, Arkansas Power Electronics International, Inc. (USA)
In this presentation, APEI, Inc. will discuss the status of development of our high performance SiC power modules for extreme environment applications.

15:15 K-2-2 (Invited)
Review of Power Converter Temperature and Loss Simulation using Compact Device Models
P. A. Mawby and A. T. Bryant, Univ. of Warwick (UK)
This paper describes the simulation technique developed for the determining the losses in high power converters. |The state of the art models are based on fundamental understanding of the power semiconductor devices that underpin this rapidly evolving technology.

L-2: Silicon Based Biomedical Devices (Area 11)
(14:45-16:00)
Chairs: Y. S. Yang (National Chiao Tung Univ.)
J. Ohta (NAIST)

14:45 L-2-1 (Invited)
Advanced Silicon Integration Technologies for Lab-on-Chip and Implantable Device Applications
C. V. Hoof[1,2] and M. O. D. Beeck[1], [1]IMEC and [2]Katholieke Univ. Leuven (Belgium)
This paper will present silicon-based enablers of eHealth. Ultra-low-power circuits will enable wearable wireless health assistants, advanced silicon integration and packaging will enable miniaturized implantable systems, and silicon-based sensors and microsystems will enable Lab-on-Chip (LoC) solutions for personal diagnostics.

15:15 L-2-2
Electronic immunochromatography embedding RFID sensor
Y. Yazawa, C. Gouda, A. Shiratori, T. Oonishi, K. Watanabe and K. Uchida, Hitachi, Ltd. (Japan)
A novel sensitive and quantitative POCT device—incorporating a chemiluminescent reaction and RFID sensor chips into an immunochromatographical test strip—with easy operability was developed and demonstrated.

Wednesday, September 22

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A-2: Electric Characterization of Organic Semiconductors (Area 10)

15:30 A-2-3
Grain boundary effect on charge transport in pentacene thin films
M. Weis[1], K. Gmucova[1], V. Nadazdy[1], D. Hasko[2], D. Taguchi[3], T. Manaka[3] and M. Iwamoto[3], [1]Slovak Academy of Sciences, [2]International Laser Centre and [3]Tokyo Tech. (Slovakia)
We illustrates with the organic field-effect transistors decrease of the effective mobility and presence of traps with decrease of the grain size. Accumulation of the defects on the grain boundary is also discussed.

1F 212

B-2: Ge MOS Technology 2 (Area 1)

15:25 B-2-3
Suppression of ALD-Induced Degradation of Ge MOS Interface Properties by Low Power Plasma Nitridation of GeO_2
R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka and S. Takagi, Univ. of Tokyo (Japan)
A low power plasma nitridation process to an ultra thin GeO2 IL was proposed to eliminate the degradation induced by ALD Al2O3 deposition, without losing the superior MOS interface properties of GeO2/Ge.

15:45 B-2-4
GeO Desorption Mechanism from GeO_2/Ge Stack Determined by ^{73}Ge Labeling Technique in Thermal Desorption Spectroscopy (TDS) Analysis
S. K. Wang[1], K. Kita[1,2], T. Nishimura[1,2], K. Nagashio[1,2] and A. Toriumi[1,2], [1]Univ. of Tokyo and [2]JST-CREST (Japan)
Desorption mechanism of GeO from GeO_2/Ge has been studied. We conclude that the GeO desorption initiates from the GeO_2 surface by using ^{73} Ge labeling technique. Two kinds of GeO desorption (uniform and non-uniform) has been demonstrated.

1F 213

C-2: Transport Physics (Area 3)

15:25 C-2-3
Experimental Investigation and Modeling for Surface Roughness Limited Mobility in Strained pMOSFETs
W. P. N. Chen, J. J. Y. Kuo, B. K. Y. Lu and P. Su, National Chiao Tung Univ. (Taiwan)
This work provides an experimental assessment of surface roughness scattering limited mobility under process-induced uniaxial strain. By accurate split C-V mobility extraction method, the surface roughness scattering limited mobility of advanced strained short channel devices has been extracted at cryogenic temperature to suppress phonon scattering mechanism.

15:45 C-2-4
Impact of the Channel Direction Dependent Low Field Hole Mobility on Si(100)
R. Kuroda, A. Teramoto, S. Sugawa and T. Ohmi, Tohoku Univ. (Japan)
The channel direction dependency of low field hole mobility characteristics due to the direction dependency of heavy hole effective mass is experimentally observed for pMOS fabricated on the atomically flat silicon (100) orientation surface.

2F 221

D-2: Advanced Design and Measurement (Area 7)

15:15 D-2-3
Design Rules and Characterisation of Electrically Pumped VECSELS
D. T. D. childs, J. Orchard, L. C. Lin, B. J. Stevens, D. Williams and R. A. Hogg, Univ. of Sheffield (UK)
We present details of the design rules and trade offs in the realisation of CW room temperature operating VECSELs. We focus on measurements of thermal effects specific to electrically pumped devices.

15:30 D-2-4
Programmable optically reconfigurable gate array using a silver-halide holographic memory including six configuration contexts
S. Kubota and M. Watanabe, Shizuoka Univ. (Japan)
This paper presents a practical demonstration of a programmable optically reconfigurable gate array (PORGA) using a silver-halide holographic memory including six configuration contexts. Aspects of the PORGA architecture performance were analyzed experimentally.

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E-2: Flash Memory Ⅰ (Area 4)

15:25 E-2-3
The Evaluation Method and Characteristics of IPD layer in TLC (Triple Level Cell) NAND Flash
B. D. Jo, Y. Jeong, J. Y. Park, P. H. Kim, S. J. Park, M. K. Cho, K. O. Ahn and Y. Koh, Hynix Semiconductor Inc. (Korea)
As NAND flash market demand for larger capacity at low cost increases, the feature-size scaling and multi-level per bit have been developed. Hence, Triple Level Cell (3 bits per cell) is being intensively developed now. In this paper, we present newly adopted evaluation method of IPD layer and its characteristics in terms of charge trap, program saturation Vth and charge loss according to PV levels in TLC NAND flash.

15:45 E-2-4
A Low Power and Improving Read Disturb Characteristics by Using Multi-CSL Architecture in MLC NAND Flash Memory
M. Kang[1,2], K. T. Park[2], Y. Song[2], S. Lee[2], Y. Lim[2], K. D. Suh[3] and H. Shin[1], [1]Seoul National Univ., [2]Samsung Electronics Co., Ltd. and [3]Sungkyunkwan Univ. (Korea)
In this paper, a new NAND string and its read operation scheme using multi-common source line (CSL) architecture to suppress power consumption and improve the read disturb characteristics were proposed in 40 nm NAND technology.

4F 242

F-2: Novel Structures (Area 9)

15:15 F-2-3
Observation of Resistive Switching in ZnO Single Crystal Whiskers
R. Mohan and S.J. Kim[1], Jeju Nat. Univ. (Korea)
The resistive memory switching in ZnO single crystal whiskers has been investigated. Anomalous resistance fluctuations between intermediate resistance states and RON state have been observed by using the current bias method.

15:30 F-2-4
Formation of thin-film-like Ge quantum dots array in thermally oxidizing SiGe pillar technique for energy harvest/conversion applications
C. C. Wang, K. H. Chen, C. Y. Chien and P. W. Li, National Central Univ. (Taiwan)
We propose a simple method, thermally oxidizing vertical SiGe pillar matrix, for generating dense and size-tunable Ge QD array in a self-organized manner. The knowledge gained from this 3D QD array system is readily transferable for fabricating QD photovoltaic and TE devices.

15:45 F-2-5
KFM Observation of Single-Electron Filling in Isolated and Clustered Dopants
M. Anwar[1], D. Moraru[1], M. Ligowski[1,2], T. Mizuno[1], R. Jablonski[2], Y. Ono[3] and M. Tabe[1], [1]Shizuoka Univ., [2]Warsaw Univ. of Tech. and [3]NTT Basic Res. Labs. (Japan)
We utilized LT-KFM to characterize charging effects in thin P-doped SOI-FETs. We observe single-electron filling, with changing VBG, in isolated and in clusters of dopants. This observation will provide support for design of electronic devices based on single-electron charging of individual dopants.

Special Plenary Session: A Half Century of Esaki Diode and Lasers (Tokyo Dome Hotel)

Special Plenary Session (17:00-18:30)
Chair: Y. Arakawa, Univ. of Tokyo, Japan

17:00 PL-2-1
50 Years of the Laser
K. Shimoda, Univ. of Tokyo, Japan

17:45 PL-2-2
In Half a Century of Research Career, What did I Explore?
L. Esaki, Yokohama College of Pharmacy / The Science and Technology Promotion Foundation of Ibaraki, Japan

18:30-20:00 Reception (Tokyo Dome Hotel)

Wednesday, September 22

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G-2: RF Circuits and Systems (2) (Area 5)

15:25 G-2-3
Wide-Frequency-Range Low-Noise Injection-locked Ring VCO for UWB Applications in 90 nm CMOS
S. Y. Lee, S. Amakawa, N. Ishihara and K. Masu, Tokyo Tech (Japan)
A scalable, wide-frequency-range (2.62-10.5GHz) and low-noise injection-locked VCO is proposed. In this work, by using an injection locking technique, a 1-MHz-offset phase noise of − 119dBc/Hz at 10GHz was achieved with comparable power consumption.

15:45 G-2-4
A 26GHz Transceiver Chipset for Short Range Radar using Post-Passivation Interconnection
S. Ujita, Y. Kawai, K. Kaibara, N. Negoro, T. Fukuda, H. Sakai, T. Ueda and T. Tanaka, Panasonic Corp. (Japan)
26GHz spread-spectrum transceiver chipset for short-range radar fabricated using post-passivation interconnection is presented. Frequency triplers lower the local oscillation frequency, which suppress the carrier leakage. Balun in Rx-IC increases the dynamic range.

4F 244

H-2: Growth of Grapheme for Electronics Applications (Area 8)

15:30 H-2-3
Synthesis of High Quality Graphene Using Diamond-Like Carbon (DLC) as Solid Carbon Source
B. Liu[1], G. Han[1], M. C. Yang[2], Q. Zhou[1], S. M. Koh[1] and Y. C. Yeo[1], [1]National University of Singapore and [2]Data Storage Institute (Singapore)
We report the first demonstration of synthesis of high quality graphene using Diamond-Like Carbon (DLC) as solid carbon source. DLC thickness, nickel thickness, SiO2 capping layer, and annealing temperature are demonstrated to affect graphene quality.

15:45 H-2-4
TEM characterization of epitaxial graphene formed on Si(111), Si(110), Si(100)
H. Handa[1], R. Takahashi[1], S. Abe[1], K. Imaizumi[1], M. H. Jung[1], S. Ito[2], H. Fukidome[1] and M. Suemitsu[1,3], [1]Tohoku Univ. and [2]CREST-JST (Japan)
Graphene forms on 3C-SiC thin films grown on Si substrates by annealing the SiC films in UHV. In this paper, we have conducted cross-sectional TEM measurements on graphene, focusing on the Si surface orientational dependence.

4F 245

I-2: GaN HEMTs (Area 8)

15:30 I-2-3
Suppression of gate leakage and enhancement of breakdown voltage using Al_2O_3 nano particles as gate dielectric for AlGaN/GaN MOS-HEMTs
J. Freedsman, T. Kubo, A. Watanabe, S. L. Selvaraj and T. Egawa, Nagoya Inst. of Tech. (Japan)
We have fabricated AlO nano particles based MOS-HEMT. The MOS-HEMT exhibit good pinch off features with reduced gate leakage and improved breakdown voltage when compared to conventional HEMT. The observed Id-max and gm-max for MIS-HEMT are 425 mA/mm and 121 mS/mm respectively.

15:45 I-2-4
In situ Silane Surface Passivation for Gate-First Undoped AlGaN/GaN HEMTs with Minimum Current Collapse and High-Permittivity Dielectric
X. Liu[1], H. C. Chin[1], E. K. F. Low[1], W. Liu[2], L. S. Tan[1] and Y. C. Yeo[1], [1]National University of Singapore and [2]Inst. of Materials Res. and Engineering, Agency for Sci. Tech. and Res. (Singapore)
An in situ surface passivation technology comprising vacuum anneal and silane treatment was integrated in the fabrication of undoped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs). Excellent DC characteristics with minimum current collapse at room temperature were obtained. DC characteristics at high temperatures were also investigated.

4F 246

J-2: Carbon Nanotube Properties and Transport (Area 13)

15:15 J-2-3
Doubly-suspended carbon nanotube resonator for ultrasensitive mass measurement
K. Oda[1], T. Arie[1,2] and S. Akita[1,2], [1]Osaka Prefecture Univ. and [2]CREST-JST (Japan)
We investigated the oscillation of the doubly-suspended CNT resonator in air and in vacuum by measuring the drain current. The resonant frequency increased with increasing the absolute value of the gate voltage.

15:30 J-2-4
Electronic transport of single-wall carbon nanotubes with superconducting contacts
M. Shimizu[1,2], H. Akimoto[1] and K. Ishibashi[1], [1]RIKEN and [2]Tokyo Univ. of Science (Japan)
We will report our on-going study of the electronic transport properties of the single wall carbon nanotube quantum dot with Al contacts in the high transparency regime and in the intermediate transparency regime (Kondo regime).

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K-2: Power Module Technology (Area 14)

2F 223

L-2: Silicon Based Biomedical Devices (Area 11)

15:30 L-2-3
Highly Accurate Optical Stimulation of Neuron using Si Neural Probe with Optical Waveguide
R. Kobayashi, S. Lee, S. Kanno, Y. Yukita, K. Lee, T. Fukushima, T. Ishizuka, H. Mushiake, H. Yao, M. Koyanagi and T. Tanaka, Tohoku Univ. (Japan)
A novel Si neural probe with micromachined optical waveguide for optical stimulation of neurons is proposed. We fabricated a carefully-designed Si neural probe and evaluated optical characteristics such as a propagation pattern and output patterns.

15:45 L-2-4
Fabrication and in vivo Evaluation of High Performance Stimulus Electrodes Employed in a CMOS Chip for Retinal Prosthesis
T. Noda[1], S. Tomimatsu[1], K. Sasagawa[1], T. Tokuda[1], Y. Terasawa[2], K. Nishida[3], T. Fujikado[3] and J. Ohta[1], [1]NAIST, [2]NIDEK Co., Ltd. and [3]Osaka Univ. (Japan)
Iridium oxide electrodes with high charge delivery capacity (CDC), employed in CMOS chips for retinal prosthesis, were fabricated. Relationship of fabrication process parameter with CDC was evaluated through electrochemical method. In vivo evaluation was performed using fabricated electrodes, and it confirmed that retinal stimulation was possible.

Special Plenary Session: A Half Century of Esaki Diode and Lasers (Tokyo Dome Hotel)

Special Plenary Session (17:00-18:30)
Chair: Y. Arakawa, Univ. of Tokyo, Japan

17:00 PL-2-1
50 Years of the Laser
K. Shimoda, Univ. of Tokyo, Japan

17:45 PL-2-2
In Half a Century of Research Career, What did I Explore?
L. Esaki, Yokohama College of Pharmacy / The Science and Technology Promotion Foundation of Ibaraki, Japan

18:30-20:00 Reception (Tokyo Dome Hotel)