Session information

Oral Presentation

05: Photonics: Devices / Integration / Related Technology

[A-2] New materials and platforms for photonics

Tue. Sep 27, 2022 2:00 PM - 3:45 PM 101 (1F)

Session Chair: Xuejun Xu (NTT Corp.), Ueli Koch (ETH Zurich)

2:00 PM - 2:30 PM

[A-2-01] Integrated active lithium niobate photonic devices

Zhiwei Fang[2], Haisu Zhang[2], Jintian Lin[1], ○Ya Cheng[1,2]
(1. Shanghai Inst. of Optics and Fine Mechanics (China), 2. East China Normal Univ. (China))

2:30 PM - 2:45 PM

[A-2-02] Improving the Production of β-Ga_2O_3 Solar-Blind Metal-Oxide-Semiconductor Field-Effect Phototransistor Based on Top-Gate Structure

○Zhe Li[1], Qian Feng[1], Jincheng Zhang[1], Chunfu Zhang[1], Yue Hao[1] (1. Xidian Univ. (China))

2:45 PM - 3:00 PM

[A-2-03] Current injection and luminescence properties of wurtzite InP nanowires with crystal phase transition

○Yuki Azuma[1], Shun Kimura[1], Hironori Gamo[1], Junichi Motohisa[1], Katsuhiro Tomioka[1] (1. Hokkaido University (Japan))

We characterized current injection and electroluminescence (EL) properties of wurtzite (WZ) InP nanowire (NW) light-emitting diodes (LEDs) with axial junction. The EL spectra showed two peaks originated from zinc-blende (ZB) and WZ phase. Also, the EL spectra exhibited two different behaviors although the LED junction structure was same. One showed single EL peak, originated from only bandgap of ZB InP. The another showed two EL peaks that originated from ZB and WZ phase. The difference of the EL behavior was resulted from the difference in contact position and depletion layer spreading.

3:00 PM - 3:15 PM

[A-2-04] Analysis of III-V MOS optical modulator with transparent doped graphene gate electrode

○Tipat - Piyapatarakul[1], Hanzhi Tang[1], Kasidit Toprasertpong[1], Shinichi Takagi[1], Mitsuru Takenaka[1] (1. Univ. of Tokyo (Japan))

We numerically study the modulation properties of InGaAsP metal-oxide-semiconductor (MOS) optical modulator with graphene gate electrode operating at a 1.55 um wavelength. Using p-type doped graphene as a transparent gate electrode, we can fully utilize the electron-induced refractive index change in an n-type InGaAsP waveguide, enabling the phase modulation efficiency of 0.79 Vcm and 0.22 dB optical loss for pi phase shift when the gate oxide thickness is 100 nm. The high electron mobility in InGaAsP also enables the modulation bandwidth of greater than 100 GHz.

3:15 PM - 3:30 PM

[A-2-05] Controllability of Luminescence Wavelength from GeSn Wires Fabricated by Laser Zone Melting on Quartz Substrates

○Takayoshi Shimura[1], Ryoga Yamaguchi[1], Naoto Tabuchi[1], Masato Kondo[1], Mizuki Kuniyoshi[2], Takuji Hosoi[3], Takuma Kobayashi[1], Heiji Watanabe[1]
(1. Osaka Univ. (Japan), 2. ULVAC-Osaka Univ. Joint Res. Lab. for Future Tech. (Japan), 3. Kwansei Gakuin Univ. (Japan))

We examined the effects of laser scan speed and power on the Sn fraction and crystallinity of GeSn wires fabricated by laser zone melting on quartz substrates. The Sn fraction increased from 1 to 3.5% with the increase in the scan speed from 5 to 100 um/s, corresponding to luminescence wavelength from 1770 to 2070 nm. This result can be understood as the scan speed dependence of the non-equilibrium degree during crystal growth. The increase in laser power reduced the Sn fraction and caused blue shift of luminescence wavelength. We discuss these phenomena based on the growth kinetics of zone melting.

3:30 PM - 3:45 PM

[A-2-06] Optical Properties of Innovative $GeSe_{1-x}Te_x$ Phase-Change Material Thin Films for On-Chip Active Components, Non-Linear and Neuromorphic Applications

○Anthony Albanese[1], Martina Tomelleri[1], Jean-Baptiste Dory[1], Christophe Licitra[1], Benoît Charbonnier[1], Jean-Baptiste Jager[2], Aurélien Coillet[3], Benoît Cluzel[3], Pierre Noé[1]
(1. Univ. Grenoble-Alpes, CEA-LETI (France), 2. Univ. Grenoble-Alpes, CEA-IRIG (France), 3. Univ. Bourgogne, ICB, UMR 6303 CNRS (France))

In this work, the linear and nonlinear optical properties of innovative GeSe(1−x)Te(x) thin films in amorphous state as well as after crystallization are studied. These alloys obtained by industrial magnetron co-sputtering of GeSe and GeTe targets belong to the GeSe-GeTe pseudo-binary line lying between the covalent GeSe compound and the “metavalently” bonded GeTe phase-change material. They are considered as very promising candidates for high temperature non-volatile resistive memory and photonic applications. In fact, they exhibit fast and reversible phase transformations between amorphous and crystalline states with unprecedented large contrast of electronic and optical properties, a very high thermal stability of the amorphous compared to other PCMs and a high transparency in the NIR-MIR range in both states. By modifying the Te content of the thin films, one can tailor their linear and non-linear optical properties for a wide range of innovative optical and photonic applications.

Session information

Oral Presentation

11: Advanced Materials: Synthesis / Crystal Growth / Characterization

[B-2] Wide Bandgap Materials

Tue. Sep 27, 2022 2:00 PM - 3:45 PM 102 (1F)

Session Chair: Shingo Ogawa (Toray Res. Center, Inc.), Takuya Hoshi (NTT Device Technology Lab.)

2:00 PM - 2:30 PM

[B-2-01] Metrology to Support Processing and Development of 4H-SiC CMOS and Power Devices at Fraunhofer IISB from Research to Multi Project Wafer Services

○Mathias Rommel[1], Tobias Erlbacher[1] (1. Fraunhofer Inst. for Integrated Systems and Device Tech. IISB (Germany))

2:30 PM - 3:00 PM

[B-2-02] Morphology and Properties of Diamond Deposited on Grooved 4H-SiC Substrate

○Kuan Yew Cheong[1], Xiufei Hu[2], Ming Li[2], Yingnan Wang[2], Yan Peng[2], Gongbin Tang[2], Mingsheng Xu[2], Xiangang Xu[2], Jisheng Han[2], Xiwei Wang[2], Bin Li[2], Yiqiu Yang[2] (1. Universiti Sains Malaysia (Malaysia), 2. Shandong Univ. (China))

3:00 PM - 3:15 PM

[B-2-03] Characterization of Ultra High-Concentration Nitrogen-doped CVD Diamond

○Mayu Ueda[1], Kyosuke Hayasaka[1], Kyotaro Kanehisa[1], Yasuhiro Takahashi[1], Chiyuki Wakabayashi[1], Taisuke Kageura[2], Hiroshi Kawarada[1,3]
(1. Waseda Univ. (Japan), 2. National Inst. of Advanced Indus. Sci. and Tech. (Japan), 3. Kagami Memorial Res. Inst. for Materials Sci. and Tech. (Japan))

The highest nitrogen-doped CVD diamond ([N] = 8×10^(20) [cm-3]) was prepared by adding the same amount of CO2 as CH4. These thin films were evaluated by X-ray diffractometer (XRD) - including a reciprocal space mapping (RSM) measurement, Raman spectroscopy, and cross-sectional TEM images. From the physical properties, it was found that under optimum gas mixture (CH4: 2.0 [%], CO2: 2.0 [%], N2: 8.0 [%], H2: 88.0 [%]), high quality crystal was obtained de-spite the highest nitrogen content.

3:15 PM - 3:30 PM

[B-2-04] Importance of dissolving source precursor of $Ga(C_5H_7O_2)_3$ with HCl in mist CVD for α-Ga_2O_3 growth

○Rie Yamada[1], Atsushi Sekiguchi[1], Takeyoshi Onuma[1], Tohru Honda[1], Tomohiro Yamaguchi[1] (1. Univ. of Kogakuin (Japan))

We dissolved the source precursor of Ga(C5H7O2)3 with either hydrochloric acid (HCl) or nitric acid (HNO3) in the mist chemical vapor deposition (mist CVD) growth of α-Ga2O3 films on α-Al2O3 substrates. Enough film thickness was obtained when HCl was used as a source solvent, while less growth occurred when HNO3 was used. With the increase of HCl concentration, it was observed that the film thickness as well as grain size tended to increase. These results indicate that chloride ion plays an important role in the mist CVD growth of α-Ga2O3.

3:30 PM - 3:45 PM

[B-2-05] First-Principles Study for Self-limiting Growth of GaN Layers on AlN(0001) Surface

○Haruka Sokudo[1], Toru Akiyama[1], Tomonori Ito[1] (1. Univ. of Mie (Japan))

We theoretically investigate the thickness dependence of surface stability and adsorption behavior in n layer GaN grown on AlN(0001) substrate to clarify the self-limiting growth on AlN(0001) surface during MOVPE. Our first-principles calculations demonstrate that stability of GaN layers on AlN(0001) substrate is similar to that of GaN(0001) surface irrespective of GaN film thickness. Furthermore, the adsorption behavior of Ga adatom on n layer GaN on AlN(0001) surfaces are independent of film thickness. These results suggest that self-limiting growth is hardly affected by surface structures and ad-sorption behavior. method [8].

Session information

Oral Presentation

11: Advanced Materials: Synthesis / Crystal Growth / Characterization

[B-3] Group IV Materials I

Tue. Sep 27, 2022 4:15 PM - 6:00 PM 102 (1F)

Session Chair: Taizoh Sadoh (Kyushu Univ.), Akira Heya (Univ. of Hyogo)

4:15 PM - 4:45 PM

[B-3-01] Heteroepitaxy of Group IV Materials for Future Device Application

○Yuji Yamamoto[1], Wei-Chen Wen[1], Bernd Tillack[1,2]
(1. IHP - Leibniz Inst. for High Performance Microelectronics (Germany), 2. Technische Universität Berlin (Germany))

4:45 PM - 5:00 PM

[B-3-02] Vertical Alignment Control of Self-Ordered Multilayered Ge Nanodots on SiGe

○Wei-Chen Wen[1], Bernd Tillack[1,2], Yuji Yamamoto[1]
(1. IHP - Leibniz Inst. for High Performance Microelectronics (Germany), 2. Technische Universität Berlin (Germany))

Mechanism of self-ordering of Ge nanodots in SiGe was investigated by fabricating multilayer Ge nano-dots with SiGe spacers on Si0.4Ge0.6 virtual substrate. By depositing the SiGe at 550 °C or raising Ge content, the SiGe surface is smooth, resulting in vertical-ly-aligned Ge nanodots to reduce strain energy. By depositing at 500 °C and lowering Ge content, check-erboard-like surface forms and the following Ge nan-odots grow at staggered position to reduce surface energy.

5:00 PM - 5:15 PM

[B-3-03] Impact of N-type Impurities on Solid-phase Crystallization of Amorphous Ge

○Koki Nozawa[1], Takeshi Nishida[1], Takashi Suemasu[1], Kaoru Toko[1] (1. Univ. of Tsukuba (Japan))

Among n-type impurities, P doping in amorphous Ge significantly promoted the lateral growth during solid-phase crystallization, resulting in large grains. The electron mobility was the highest among n-type polycrystalline Ge directly grown on insulators at low temperatures.

5:15 PM - 5:30 PM

[B-3-04] GeSn nanodots crystal nuclei for solid phase crystallization of poly-SiGeSn

○Yusei Shirai[1], Hirokazu Tatsuoka[1], Yosuke Shimura[1,2,3]
(1. Univ. of Shizuoka (Japan), 2. RIE Shizuoka Univ. (Japan), 3. imec (Belgium))

Solid phase crystallization of polycrystalline Si1-x-yGexSny using Ge1-xSnx nanodots (Ge1-xSnx-ND) as crystal nuclei was examined. The effects of the substrate temperature and the initial Ge/Sn composition on the dot size, coverage, and substitutional Sn composition in the Ge1-xSnx-ND were investigated. Lowering deposition temperature increased the substitutional Sn composition in Ge1-xSnx-ND. Crystallization of Si deposited on the Ge1-xSnx-ND was confirmed at the deposition tempera-ture of 150 °C. The Si and Sn composition in the poly-Si1-x-yGexSny layer was 36.3% and 4.2% after an-nealing at 225 °C.

5:30 PM - 5:45 PM

[B-3-05] Molecular beam epitaxy of $Si_{1-x}Sn_x$ layers with 10%-Sn content on $Si_{1-y}Ge_y$ buffers

○Kazuaki Fujimoto[1] (1. Nagoya Univ. (Japan))

5:45 PM - 6:00 PM

[B-3-06] Study on doping by ion implantation to $Si_{1-x}Sn_x$ epitaxial layers

○Tatsuki Oiwa[1], Shigehisa Shibayama[1], Mitsuo Sakashita[1], Masashi Kurosawa[1], Osamu Nakatsuka[1,2]
(1. Nagoya Univ. (Japan), 2. IMaSS, Nagoya Univ. (Japan))

A phosphorus doping study was conducted in Si1−xSnx (x = 0.017–0.079) epitaxial layers grown on Si(001) by RF sputtering. First, we found high thermal stability of the Si1−xSnx layer even at 600 °C regardless of the ultra-low Sn solubility in Si. Thanks to this fact, we have successfully realized n-type Si1−xSnx layers with wide-ranging electron concentrations (6.4×1017–1.0×1020 cm–3) without the Sn precipitation by the ion-implantation and the activation annealing at 600 °C. Additionally, we found that pseudomorphic grown layers possess comparable electron mobility with that of Si bulk.

Session information

Oral Presentation

06: Photovoltaic / Energy Harvesting / Battery-related Technology

[C-1] Energy Harvesting Devices

Tue. Sep 27, 2022 11:30 AM - 12:15 PM 103 (1F)

Session Chair: Yasuyoshi Kurokawa (Nagoya Univ.), Shunsuke Yamada (Tohoku Univ.)

11:30 AM - 11:45 AM

[C-1-01] Group IV Semiconductor Alloy Thin Films for Environmentally Friendly

○Shintaro Maeda[1], Tomoki Ozawa[1], Takashi Suemasu[1], Kaoru Toko[1] (1. Univ. of Tsukuba (Japan))

We investigated a Ge-based ternary alloy thin film, Ge1-x-ySixSny, for synthesis, the control of carrier concentration, and thermoelectric properties, using an advanced solid-phase crystallization. The addition of small amounts of Si and Sn in Ge lowered the thermal conductivity while maintaining high power factors, resulting in higher dimensionless figure of merit than most of the environmentally friendly thin-film thermoelectrics.

11:45 AM - 12:00 PM

[C-1-02] Voltage and Power Enhancement of Hygroelectric Cell via Polyethylene Glycol Addition to Electrolyte Solution

○Yusuke Komazaki[1], Taiki Nobeshima[1], Hirotada Hirama[1], Yuichi Watanabe[1], Kouji Suemori[1], Sei Uemura[1]
(1. National Inst. of Advanced Indus. Sci. and Tech. (AIST) (Japan))

Hygroelectric cell (HEC) is an energy harvester that generates electricity by the energy of humidity change in the air, based on a concentration cell with a deliquescent solution. The performance of HEC is limited by self-discharge derived from water permeation through a cation-exchange membrane. In this work, we report on the voltage and power enhancement of HEC via the self-discharge suppression effect by adding polyethylene glycol (PEG) to the electrolyte solution of HEC. At maximum, the addition of 10 wt% PEG4000 improved the output voltage under the humidity changes between 30-90%RH to 86 mV from 25 mV and the addition of 10 wt% PEG1000 improved the output power to 7.6 µW from 4.4 µW.

12:00 PM - 12:15 PM

[C-1-03] Performance enhancement of droplet-based electricity generator using a CYTOP intermediate layer

○Haitao - Wang[1], Yasuyoshi - Kurokawa[1], Kazuhiro - Gotoh[1], Shinya - Kato[2], Shigeru - Yamada[3], Takashi - Itoh[3], Noritaka - Usami[1] (1. Nagoya Univ. (Japan), 2. Nagoya Inst. of Tech. (Japan), 3. Gifu Univ. (Japan))

Effective strategies for improving the performance of a droplet-based electricity generator (DEG) remain a challenge. Herein, we propose to bury a high negative charge density layer to act as an excellent triboelectric charge storage layer by directly enhancing the surface charge density. Consequently, we successfully fabricated a high-performance DEG with 1.4-fold higher per-for-mance than the original one, which could promote its practical application in energy harvesting.

Session information

Oral Presentation

06: Photovoltaic / Energy Harvesting / Battery-related Technology

[C-2] Inorganic Semiconductor Materials & Applications

Tue. Sep 27, 2022 2:00 PM - 3:45 PM 103 (1F)

Session Chair: Kazuhiro Gotoh (Nagoya Univ.), Shogo Ishizuka (AIST)

2:00 PM - 2:15 PM

[C-2-01] Preparation and thermoelectric characterization of boron-doped silicon nanocrystals/silicon oxide multilayers

○Keisuke Shibata[1], Shinya Kato[2], Masashi Kurosawa[1], Kazuhiro Gotoh[1], Satoru Miyamoto[1], Noritaka Usami[1], Yasuyoshi Kurokawa[1]
(1. Nagoya Univ. (Japan), 2. Nagoya Inst. Tech. (Japan))

Boron-doped silicon nanocrystals (Si-NCs)/silicon oxide (SiOy) multilayers were prepared by plasma enhanced chemical vapor deposition (PECVD) and post-annealing. The diameter of Si-NCs was changed by varying the thickness of Si-rich amorphous silicon oxide (a-SiOx) layer from ta-SiOx=3 to 50 nm. The electrical conductivity (σ) showed an increased tendency with in-creasing ta-SiOx from 3 to 13 nm. Further increase of ta-SiOx resulted in the saturation of σ at about 5.7 kS·m-1. Thermal conductivity was in the range of 1.4-1.5 W·m-1·K-1 and almost independent of the thickness of the Si-rich layer (ta-SiOx), which is much lower than that of bulk Si. A maximum power factor of 0.33 mW·m-1·K-2 was obtained at ta-SiOx=13 nm.

2:15 PM - 2:30 PM

[C-2-02] Observation of Reaction Dynamics of GASnI3 Formation from Vacuum-deposited GAI and SnI2 Bi-layer Thin Films by In-situ Infrared MAIRS

○Kazuki Shimada[1], Shingo Maruyama[1], Tetsuhiko Miyadera[2], Kenichi Kaminaga[1], Yuji Matsumoto[1]
(1. Tohoku Univ. (Japan), 2. AIST (Japan))

The reaction process of vacuum-deposited guani-dinium iodide (GAI) and SnI2 bi-layer thin films to form organic-inorganic hybrid material GASnI3 was investi-gated by using our originally developed in situ infrared (IR) multiple-angle incidence-resolved spectroscopy (MAIRS) – vacuum deposition system. The isothermal reaction process was analyzed quantitatively based on isotropic spectra which were constructed from IR MAIRS spectra. The time dependence of the formation ratio was found to strongly depend on the reaction temperature.

2:30 PM - 2:45 PM

[C-2-03] Study on The Coated Solar Cells using Chemically Synthesized SnSe Nanosheets

○Hayato Sato[1], Yuto Nunomura[1], Kohki Mukai[1] (1. Yokohama National Univ. (Japan))

Solar cells that use chemically synthesized SnSe nanosheets as the light absorption layer were investigated. SnSe nanosheets are expected as a material for tandem solar cells that can be produced by the coating method. A power conversion efficiency (PCE) of 1.07% was obtained using a light absorption layer in which SnSe nanosheets and PEDOT: PSS were mixed at a volume ratio of 1: 75. The PCE is the highest ever for a similar solar cell obtained using chemically synthesized SnSe nanosheets.

2:45 PM - 3:00 PM

[C-2-04] Effect of Substrate Temperature and Annealing Temperature on the Structural, Optical, and Electrical Properties of RF Sputtered Tungsten Oxide Thin Films

Samiya Mahjabin[1], Md. Mahfuzul Haque[1], M. S. Jamal[2], M. S. Bashar [2], Munira Sultana[2], Vidhya Selvanathana[1], K. Sobayel[1], Kamaruzzaman Sopian[1], ○Md. Akhtaruzzaman[1]
(1. Solar Energy Research Institute (SERI), Universiti Kebangsaan Malaysia (UKM) (@ The Natgional University of Malaysia) (Malaysia), 2. Bangladesh Council of Scientific and Industrial Research, Dhaka-1215, Bangladesh (Bangladesh))

3:00 PM - 3:15 PM

[C-2-05] Effects of Additional WO_3 on Heterojunction with Intrinsic Thin Layer Solar Cell

○Doowon Lee[1], Hee-Dong Kim[1] (1. Sejong Univ. (Korea))

3:15 PM - 3:45 PM

[C-2-06] Perovskite/silicon tandem solar cells: paths towards enhanced performance and stability

○Stefaan De Wolf[1] (1. KAUST (Saudi Arabia))

Session information

Oral Presentation

06: Photovoltaic / Energy Harvesting / Battery-related Technology

[C-3] Perovskite Solar Cells

Tue. Sep 27, 2022 4:15 PM - 6:00 PM 103 (1F)

Session Chair: Naoyuki Shibayama (Toin Univ. of Yokohama), Md. Shahiduzzaman (Kanazawa Univ.)

4:15 PM - 4:45 PM

[C-3-01 (Invited)] From ink development to module commercialization, approach, challenges, and opportunities.

○Samy Almosni[1] (1. Saule Technologies (Poland))

4:45 PM - 5:00 PM

[C-3-02] Enhanced Performance and Stability of Perovskite Solar Cells Fabricated By Blade-Coating Process

○Bi Shane - Cheng[1], Yuan Wen Hsiao[2], Chuan Feng Shih[3], Hsuan Ta Wu[4]
(1. Univ. of National Cheng-Kung Advanced Material Lab. (Taiwan), 2. Univ. of National Cheng-Kung Advanced Material Lab. (Taiwan), 3. Univ. of National Cheng-Kung Advanced Material Lab. (Taiwan), 4. Univ. Minghsin of Science and Technology (Taiwan))

This study aims to explore the completion of perovskite solar cell technology with a large-area blade coating process. In this study, the structural transformation will be carried out, and the dual active layer will be added to the solar cell structure design and combined with the 2D/3D heterojunction. Using two-dimensional perovskite to reduce the surface defects of three-dimensional perovskite, it finally has excellent performance on solar cells, and the highest efficiency of 15.96% is achieved by the blade coating process in the high humidity atmospheric environment. The device with high stability, after 35 days still keeps the high performance above 15%.

5:00 PM - 5:15 PM

[C-3-03] First-principles Theoretical Study on Photo-induced Composition Separation of Mixed-halide Perovskites $CsPb(I_xBr_{1-x})_3$ for Solar-cell Application

○Ami Tomita[1], Takashi Nakayama[1] (1. Chiba Univ. (Japan))

Mixed-halide perovskites CsPb(IxBr1-x)3 are promising materials for solar-cell usage because their band gaps can be easily controlled by their halogen compositions. However, they often separate into I-rich and Br-rich phases under photo irradiation, which leads to the instability of optical properties and thus is one of issues for their application. In this work, by the first-principles calculations, we show that the photo-induced carriers promote such composition separation of mixed-halide CsPb(IxBr1-x)3, and discuss how to prevent such separation based on the result.

5:15 PM - 5:30 PM

[C-3-04] Impedance analysis of light soaking and reverse bias behavior in perovskite solar cell

○Takeshi Tayagaki[1], Atsushi Kogo[1], Masahiro Yoshita[1] (1. AIST (Japan))

5:30 PM - 5:45 PM

[C-3-05 (Late News)] Highly Efficient Perovskite Solar Cells with Surface Passivation Surpassing 5,000 Hours of Operational Stability

○Ganbaatar Tumen-Ulzii[1], Toshinori Matsushima[2], Chihaya Adachi[2], Samuel D. Stranks[1]
(1. Univ. of Cambridge (UK), 2. Kyushu Univ. (Japan))

5:45 PM - 6:00 PM

[C-3-06 (Late News)] High Stable Lead-Free Bismuth based Perovskite Photovoltaics Fabricated by Vacuum Deposition

○Md Shahiduzzaman[1], Masahiro Nakano[1], Makoto Karakawa[1], Jean Michel Nunzi[1], Tetsuya Taima[1] (1. Kanazawa University (Japan))

Session information

Oral Presentation

07: Organic / Molecular / Bio-electronics

[D-1] Micro/Nano technologies for biosensing and interfaces

Tue. Sep 27, 2022 11:30 AM - 12:30 PM 104 (1F)

Session Chair: Takashi Tokuda (Tokyo Tech), Cheng-Hsien Liu (National Tsing Hua Univ.)

11:30 AM - 11:45 AM

[D-1-01] Comparison of the H_2S gas response characteristics of semiconductor gas sensors (HFGFET-, TFT-, and resistor-type) fabricated on the same wafer.

○Gyuweon Jung[1], Wonjun Shin[1], Hunhee Shin[1], Seongbin Hong[1], Yujeong Jeong[1], Kangwook Choi[1], Jinwoo Park[1], Donghee Kim[1], Chayoung Lee[1], Jaehyeon Kim[1], Woo Young Choi[1], Jong-Ho Lee[1] (1. Seoul Nat. Univ. (Korea))

So far, various types of semiconductor gas sensors have been proposed. However, there are few compara-tive studies of various sensor types. Here we compare the H2S gas-sensing properties (response and SNR) of HFGFET-, TFT-, and resistor-type gas sensors. FET-type (HFGFET- and TFT-type) gas sensors have different responses depending on the operating region. FET-type gas sensors have the largest response and SNR when operating in the subthreshold region and at VGS = Vth, respectively. In contrast, the resistor-type sensor showed a similar response and SNR regardless of the biasing condition.

11:45 AM - 12:00 PM

[D-1-02] Distributed CMOS chip for retinal prosthesis with high-rate stimulation

○Yuki - Nakanishi[1], Kiyotaka - Sasagawa[1], Ronnakorn - Siwadamrongpong[1], Kenzo - Shodo[2], Yasuo - Terasawa[2], Hironari - Takehara[1], Makito - Haruta[1], Hiroyuki - Tashiro[1,3], Jun - Ohta[1]
(1. Nara Inst. of Sci. and Tech. (Japan), 2. Nidek Co. LTD (Japan), 3. Kyushu Univ. (Japan))

In this study, we propose a CMOS chip for retinal prosthesis for high-rate stimulation. With an optimized control circuit, the current values of stimulation electrodes were set by only 36 clocks per electrode. We demonstrated operation at a frequency of 2.3 MHz on the prototype chip and a setup time of 17 μs for each electrode.

12:00 PM - 12:15 PM

[D-1-03] Design and Evaluation of Light and Dark Adaptation Functions for High QoL Artificial Vision Chip

○Kohei Nakamura[1], Yaogan Liang[1], Bang Du[1], Shengwei Wang[1], Yuta Aruga[1], Bunta Inoue[1], Hisashi Kino[1], Takafumi Fukushima[1], Koji Kiyoyama[2], Tetsu Tanaka[1] (1. Tohoku Univ. (Japan), 2. Nagasaki Inst. of Applied Sci. (Japan))

To cope with the increasing number of visually impaired people due to the aging of the population, research on artificial vision, which reconstructs vision using engineering methods, is being actively conducted. To realize the artificial vision with high QOL, it is important to implement the Light and Dark Adaptation (LDA) function, one of the human retinal functions. Although several methods to implement the LDA function have been proposed using electronic circuits, some issues remain regarding function accuracy and circuit area. This study developed an integrated circuit for artificial vision that realizes a small-area appropriate LDA function with high accuracy by introducing a feedback function that changes the sensitivity control signal in steps.

12:15 PM - 12:30 PM

[D-1-04] Controlling Fluorescence Quenching Efficiency of Graphene Oxide to Lipid Bilayers using SiO_2 Layer Fabricated by Atomic Layer Deposition

Jocelyn Min Yuan Lau[1], Kensaku Kanomata[2], Fumihiko Hirose[2], ○Ryugo Tero[1]
(1. Toyohashi Univ. Tech. (Japan), 2. Yamagata Univ. (Japan))

The SiO2 layer fabricated by the atomic layer dep-osition (ALD) method was applied to control the effi-ciency of the fluorescence quenching of graphene oxide (GO) to supported lipid bilayers (SLBs). Lipid bilayers are the fundamental structure of cell membranes. Lateral and vertical distribution of lipids and proteins in lipid bilayers are essential information to under-stand the membrane reactions on the molecular level. GO is a chemical derivative of graphene and shows a unique fluorescence quenching property. We aim to control the efficiency of GO quenching to SLB.

Session information

Oral Presentation

07: Organic / Molecular / Bio-electronics

[D-2] Biosensor, chips and microfluidic devices for cell functions

Tue. Sep 27, 2022 2:00 PM - 3:45 PM 104 (1F)

Session Chair: Ryugo Tero (Toyohashi Univ. of Tech.), Huang-Ming Chen (NYCU)

2:00 PM - 2:30 PM

[D-2-01 (Invited)] Electrochemical imaging system and its application for vascular model and stem cell differentiation

○Hitoshi Shiku[1] (1. Tohoku Univ. (Japan))

2:30 PM - 2:45 PM

[D-2-02] High-Sensitivity Extended Gate Field-Effect Transistor-Type Dopamine Sensor Based on Resistance-Coupling Effect

○Tae-Hwan Hyun[1], Won-Ju Cho[1] (1. Kwangwoon Univ. (Korea))

In this study, we propose an extended gate field-effect transistor (EGFET) based high-sensitivity dopamine (DA) sensor using resistive coupling effect to effectively amplify electrical signals. The constructed dopamine sensor has a structure in which an individual transducer unit and a sensing unit are electrically connected. The SnO2 sensing membrane of EG had a low dopamine sensitivity of 10.14 mV/log [DA], but the resistance coupling effect greatly amplified the sensitivity of dopamine up to 8.67 times and 87.95 mV/log [DA]. In addition, it was con-firmed that the resistance-binding effect can linearly amplify dopamine sensitivity. Therefore, the proposed EGFET-based sensor is expected to be an effective method for fast and accurate detection of dopamine by utilizing the resistive coupling effect.

2:45 PM - 3:00 PM

[D-2-03] Fabrication of UCNP (Upconversion Nanoparticle) Disk Device for Non-Invasive Optical Stimulation Therapy of Organ Diseases

○Shimon - Suzuki[1], Hisashi - Kino[2], Takafumi - Fukushima[1], Tetsu - Tanaka[1,2]
(1. Department of Mechanical Systems Engineering, Graduate School of Engineering, Tohoku University (Japan), 2. Department of Biomedical Engineering, Graduate School of Biomedical Engineering, Tohoku University (Japan))

Recently, a method of optical stimulation with an optical fiber by introducing a light-sensitive protein into the vagus nerve leading to the pancreas has been investigated as a treatment for diabetes mellitus. However, the optical fiber-based method has the problem of stimulating organs other than the target organ. Therefore, in this study, we proposed a non-invasive UCNP disk device using upconversion nanoparticles (UCNPs); UCNPs were mixed with a photosensitive resin SU-8 and formed into a disc shape to develop the UCNP disk device. This disc device can be introduced into the whole organ through the pancreatic duct, etc., and non-invasive optical stimulation of specific organs is possible by wirelessly emitting UCNPs. In this study, the UCNP disk device was evaluated by shape evaluation, luminescence test, and In-vitro experiment.

3:00 PM - 3:15 PM

[D-2-04] Tumor-on-a chip in 3D microfluidic device for immunotherapy study

○Yu-Chen - Chen[1], Kang-Yun Lee[2], Wei-Lun Sun[2], Wan-Chen Huang[3], Yu-Shiuan Wang[3], Wei-Chiao Chang[4], Cheng-Hsien Liu[1]
(1. National Tsing Hua Univ. (Taiwan), 2. Shuang Ho Hospital (Taiwan), 3. Academia Sinica (Taiwan), 4. Taipei Medical Univ. (Taiwan))

3:15 PM - 3:30 PM

[D-2-05] A mirodevice towards gene transfer to a cell using non-thermal atmospheric pressure plasma

Seiya Kato[1], Yuki Tsutsui[1], ○Shinya Kumagai[1] (1. Meijo Univ. (Japan))

Gene transfer is one of the key technologies in life science. Gene transfer using non-thermal atmospheric pressure plasma is expected to achieve safe and high-efficiency gene transfer among various methods. In this study, a microdevice was developed towards gene transfer to a cell using plasma.

3:30 PM - 3:45 PM

[D-2-06] A 3D-MICROFLUIDIC DRUG TESTING PLATFORM INFLUENCED BY RETICULATE VENATION OF DICOTS

○Madhushree Poddar[1], Yu-de Chu[2], Chau-Ting Yeh[2], Cheng-Hsien Liu[1]

(1. National Tsing Hua University (Taiwan), 2. Chang Gung Memorial Hospital (Taiwan))

Three-dimensional (3D) tissue models replicating liver architectures and functions are increasingly being needed for regenerative medicine. We present here a simple yet unique polydimethylsiloxane (PDMS) microfluidic chip for an easy setup of a 3D co-culture mimicking liver tumor microenvironment for drug testing. We aim to provide stable culture and open a pathway for various biological applications like drug testing. This chip contains two co-culture systems counterfeiting tumor microenvironment, including individual control groups in a gelatin methacryloyl (GelMA) hydrogel-based matrix applicable for drug testing.

Session information

Oral Presentation

07: Organic / Molecular / Bio-electronics

[D-3] Advanced technologies for bio- and chemical sensing

Tue. Sep 27, 2022 4:15 PM - 6:00 PM 104 (1F)

Session Chair: Nicolas Clement (Univ. of Tokyo), Toshihiro Shimada (Hokkaido Univ.)

4:15 PM - 4:45 PM

[D-3-01 (Invited)] 3D nanoelectrode arrays for high resolution neuronal recording at the single cell level.

○Guilhem Larrieu[1,2], Luca Bettamin[1], Ines Muguet[1], Fabrice Mathieu[1], Tatsuya Osaki [2], Joel Hernandez [2], Charline Blatche[1], Maelle Gilotin[1], Laurent Mazenq[1], Frank Bardie[1], Elsa Suberbielle [3], Yoshiho Ikeuchi[2], Daniel Dunia [3]
(1. LAAS-CNRS (France), 2. IIS, Univ. of Tokyo (Japan), 3. Infinity (France))

4:45 PM - 5:00 PM

[D-3-02] Spatiotemporal Thermal Management of Homogeneous Oxide Sensor Array for Discrimination of Biomarkers in Mixed Molecules

○Shintaro Nagata[1], Tsunaki Takahashi[1,2], Haruka Honda[1], Motoki Date[1], Yohsuke Shiiki[3], Wataru Tanaka[1], Takuro Hosomi[1,2], Kazuki Nagashima[1,2], Hiroki Ishikuro[3], Takeshi Yanagida[1,4]
(1. Department of Applied Chemistry, Graduate School of Eng., The Univ. of Tokyo (Japan), 2. JST, PRESTO (Japan), 3. Department of Electronics and Electrical Eng., Keio Univ. (Japan), 4. Inst. for Materials Chemistry and Eng., Kyushu Univ. (Japan))

We propose a chemical sensor system for discrimination of trace-level biomarkers in mixed molecules based on spatiotemporal thermal management of homogeneous oxide sensor array. Self-Joule-heating modulates chemical reactivity of individual SnO_2 channels, enabling a virtual heterogeneous chemical sensor array operation. Mixed molecules were separately transported to the sensor array via time-series desorption temperature control of silica adsorbents, which densify trace-level molecules in a sample gas. Furthermore, we demonstrate the discrimination of model samples which mimic urine of tumor patients using the proposed sensor system.

5:00 PM - 5:15 PM

[D-3-03] A Neuromorphic Olfactory System Using Temporal Encoded Spiking Neural Networks

○Jiseong Im[1,2], Donghee Kim[1,2], Woo Young Choi[1,2], Jong-Ho Lee[1,2]
(1. Seoul National Univ. (Korea), 2. Inter-Univ. Semiconductor Res. Center (ISRC) (Korea))

An efficient neuromorphic system for fast and relia-ble gas detection is proposed. FET-type gas sensors with an In_2O_3 sensing layer are fabricated and measured. Temporal encoded spiking neural network (SNN) predicts the type and concentration of the target gas using the gas responses of the sensors. Only 10 sensors are used and the network successfully detects the type and concentration of H_2S and NO_2 gases with low error (~3%) and fast infer-ence time (~7 s).

5:15 PM - 5:30 PM

[D-3-04] Na^+ sensing and electrochemical noise measured with nano FinFET

○Simon - Grall[1], Yumi Gosselin[1], Inès Muguet[2], Laurent Jalabert[1], Soo Hyeon Kim[1], Guilhem Larrieu[2], Nicolas Clement[1]
(1. Univ. of Tokyo/LIMMS-CNRS (Japan), 2. LAAS-CNRS (France))

Ion-sensitive field effect transistor (ISFET) are commonly used as pH sensors, but the interactions of these devices with other ions remain poorly understood. Recently, a selective-layer-free approach has been introduced based on the non-Coulombic cation adsorption on the surface of a silicon nanotransistor. We show in this work that this approach can be extended to other devices architecture as illustrated with a micrometer-thick nano FinFET covered by Al_2O_3 oxide. Sensitivity to Na^+ ion is demonstrated over a wide concentration range (6 orders of magnitude), with signal to noise ratio consistently over 150.

5:30 PM - 5:45 PM

[D-3-05] H_2S Sensing Characteristics of the Amplifier Circuit Consisting of *p*FET-type and Resistor-type Gas Sensors

○Yujeong Jeong[1], Seongbin Hong[1], Gyuweon Jung[1], Wonjun Shin[1], Woo Young Choi[1], Jong-Ho Lee[1]
(1. Seoul National Univ. (Korea))

We investigate the H2S sensing characteristics of the amplifier circuit consisting of the pFET- and resistor-type gas sensor. The pFET- and resistor-type gas sensors are fabricated on the same substrate. When exposed to H2S gas, the drain current of the pFET-type gas sensor decreases while the current of the resistor-type gas sensor increases. The Vout of the amplifier circuit changes more sensitively to gas molecules than that of other amplifier circuits since the pFET-type sensor has complementary sensing characteristics to the resistor-type sensor.

5:45 PM - 6:00 PM

[D-3-06] Detection of Lysophosphatidylcholine, a Sepsis Biomarker, from Complex Solution and Plasma, in Few Minutes, using Silanized Porous Silicon Surfaces and Desorption Ionization on Silicon Mass Spectrometry.

○Antonin Lavigne[1], Benoit Gilquin[2], Vincent Jousseaume[2], Marc Veillerot[2], Thomas Géhin[3], Céline Chevalier[3], Cécile Jamois[3], Yann Chevolot[3], Magali Phaner-Goutorbe[1], Christelle Yeromonahos[1]
(1. Univ. Lyon, Ecole Centrale de Lyon (France), 2. Univ. Grenoble Alpes, CEA Leti (France), 3. Univ. Lyon, CNRS (France))

In the present study, we propose a tool for Lyso-PC trapping, from plasma, based on porous silanized silicon surfaces and compatible with Desorption Ionization on Silicon Mass Spectrometry (DIOS-MS) detection. Results show that by tuning the chemical nature of the silane monolayer, the Lyso-PC MS detection signal can be im-proved enough to overcome the use of an organic matrix and to allow direct detection in plasma samples, without any pre-treatment steps.

Session information

Oral Presentation

10: Thin Film Electronics: Oxide / Non-single Crystalline / Novel Process

[E-1] Emerging Thin Film Devices and Technologies

Tue. Sep 27, 2022 11:30 AM - 12:45 PM 105 (1F)

Session Chair: Jun Koyama (Semiconductor Energy Lab.), Juan Paolo Bermundo (NAIST)

11:30 AM - 11:45 AM

[E-1-01] Reliability Study of Stacked high-k Metal-Insulator-Metal Capacitors

Wei-Hua Chen[1], ○Gui-Sheng Chao[1], Chrong-Jung Lin[1], Ya-Chin King[1] (1. Univ. of Hsinchu (Taiwan))

11:45 AM - 12:00 PM

[E-1-02] Room-temperature processable highly amorphous transparent B-doped In_2O_3 for use as a flexible conductive film

○Shun Mori[1], Ayumu Nodera[1], Kotaro Watanabe[1], Kaito Murano[1], Shinya Aikawa[1] (1. Kogakuin Univ. (Japan))

Recently, completely amorphous transparent conductive
oxides are strongly much attention for realization of next-generation flexible devices. In this study, we fabricated
highly amorphous B-doped In2O3 (IBO) with comparable
electrical properties of a commercial ITO, even at room temperature deposition. We also demonstrated a bending test to compare mechanical flexibility with ITO. The result showed that the IBO forms large domains with polygonal shape. We believe that the domain shape is important to improve mechanical flexibility of brittle oxide thin-films.

12:00 PM - 12:15 PM

[E-1-03] Optical Properties of C-axis Oriented Polycrystalline GaN Thin Layer on Si (001) substrate grown by RF-MBE

○Shyun Koshiba[1], Takeshi Kuraoka[1], Kazuhiro Morishita[1], Hidefumi Akiyama[2], Naoshi Takahashi[3], Hayato Miyagawa[1], Yasuhiro Tanaka[1] (1. Kagawa University (Japan), 2. Univ. of Tokyo (Japan), 3. Kagawa University (Japan))

Optical properties of c-axis oriented polycrystalline GaN on the Si (001) substrates formed by plasma assisted molecular beam epitaxy were studied. Light emission near the band edge of polycrystalline GaN was observed by PL measurement at room temperature. From the red shift of the peak and the size of the peak width, the effects of lattice strain with the Si substrate and grain boundaries, on fluctuation in the GaN bandwidth were clarified. As a result of Voigt function fitting of the PL spectrum at 77K, it was clarified that there are three energy levels related to the GaN near band edge and crystalline defects.

Results of room temperature PL measurement of samples with GaN layers of different thickness and sam-ples with an AlN barrier layer in between GaN and Si substrate, thickness of the surface depletion layer of the c-axis oriented polycrystalline GaN is smaller than 20 nm, while the thickness of the depletion layer from the GaN / Si interface is between 20 nm and 100 nm.

12:15 PM - 12:30 PM

[E-1-04 (Late News)] HfO_2-based ferroelectric-gated variable-area capacitors

○Takaaki Miyasako[1], Shingo Yoneda[1], Tadasu Hosokura[1], Masahiko Kimura[1], Eisuke Tokumitsu[2]
(1. Murata Manufacturing Co., Ltd. (Japan), 2. Japan Advanced Institute of Science and Technology (JAIST) (Japan))

12:30 PM - 12:45 PM

[E-1-05] pH Sensing Enhancement for ALD High-k Membrane By Stack Structures and Post annealing In LAPS

○Jiun Han Yen[1], Yu Cheng Yang[2], Nai Chuan Chen[1,2], Chia Ming Yang[1,2,3,4]
(1. Inst. of Electro-Optical Engineering, Chang Gung Univ. (Taiwan), 2. Department of Electronic Engineering, Chang Gung Univ. (Taiwan), 3. Department of Nephrology, Chang Gung Memorial Hospital (Taiwan), 4. Department of Materials Engineering, Ming-Chi Univ. Tech. (Taiwan))

The atomic deposition system (ALD) is one of the best methods to deposit high-k oxide thin films and the stacked structure, which can greatly improve the stability of the device performance. Therefore, a high-quality pH sensing membrane constructed by the stack structure with Al2O3 and HfO2 nm-scale films in-situ layer-by-layer process by ALD system is proposed in this study. The total thickness of this stack structure is 24 nm, which is composed with Al2O3 and HfO2 layer with thickness of 6 and 6 nm for 2 cycles in sequence. In this fabricated sensing membrane on Si-based light-addressable potentiometric sensor (LAPS), an N2 RTA treatment at 400°C was used to improve the hydrogen ion sensitivity, linearity, hysteresis and drift to be 54.9 mV/pH, 99.9%, 4.16 mV and -0.35 mV/h, respectively. This superior pH sensing performance can be recommended to apply in the field-effect sensors.

Keywords — Al2O3, HfO2, high-k, LAPS, photo current, RTA, stacked structure

Session information

Oral Presentation

10: Thin Film Electronics: Oxide / Non-single Crystalline / Novel Process

[E-2] Advanced Group IV Thin Film Devices and Technologies

Tue. Sep 27, 2022 2:00 PM - 4:00 PM 105 (1F)

Session Chair: Shin-ichiro Kuroki (Hiroshima Univ.), Ryo Matsumura (NIMS)

2:00 PM - 2:30 PM

[E-2-01 (Invited)] In-situ observations of crystal growth behaviors of silicon during solidification

○Kozo Fujiwara[1] (1. Tohoku Univ. (Japan))

2:30 PM - 2:45 PM

[E-2-02] Characteristics of FD-SOI-MOSFETs using low-temperature sputtering SiO_2 gate insulator with high pressure water annealing

○Wenchang Yeh[1], Masato Ohya[1], Yusaku Magari[1] (1. Shimane University (Japan))

N channel MOSFET were fabricated on intrinsic 60nm-Si SOI substrate using low-temperature sputter-ing SiO2 gate insulator (GI) combined with high pres-sure water annealing (HWA), in order to reveal poten-tial of low-temperature sputtering SiO2 as GI. In order to prevent unwanted contamination of carbon at chan-nel interface from photoresist, resistless process was used. The maximum process temperature after GI formation was 580°C. Resultant characteristics are field effect mobility μ of 676 cm2/Vs, subthreshold swing ss of 122 mV/dec, Vth of 0.9 V, and Ion/Ioff of 6×108.

2:45 PM - 3:00 PM

[E-2-03] A Novel Scheme for Fabrication of T-Gate Polysilicon Thin Film Transistors with Lightly Doped Drain

○Cheng-Kuei Lee[1], Po-Hsun Yu[1], Chang-Mao Wu[1], Pei-Wen Li[1], Horng-Chih Lin[1] (1. National Yang Ming Chiao Tung Univ. (Taiwan))

We report a novel approach for fabricating T-gate polysilicon thin film transistors (T-gate TFTs) with lightly doped drain (LDD) structures using a single process step of S/D implantation. The fabrication is thus greatly simplified as compared to conventional LDD formation scheme. Moreover, the T-gate device exhibits not only suppressed off-state leakage but also much higher current drive than that of conventional poly-Si TFT without LDD.

3:00 PM - 3:15 PM

[E-2-04] Implantation-Free Vertically Stacked GAA Poly-Si Nanosheet FETs with Raised Source/Drain

○Po-Yi Kuo[1], Po-Yang Huang[1], Yu-Cheng Chou[1], Cing-Long Huang[1], Yu-Ming Chiu[1]
(1. Department of Electronic Engineering, Feng Chia University (Taiwan))

The implantation-free vertically stacked gate-all-around (GAA) poly-Si nanosheet (NS) FETs (VS GAA Poly-Si NSTs) with raised S/D have been successfully fabricated and demonstrated. The proposed VS GAA Poly-Si NSTs with 2 NS channels exhibit improved electrical characteristics and low gate operation voltages compared with conventional SPC planar poly-Si TFTs.

3:15 PM - 3:30 PM

[E-2-05] First Demonstration of Rectifying Schottky Contact on Polycrystalline P-Type Ge Using ZrN Electrode

○Kenta Moto[1,2], Kaoru Toko[3], Tomonari Takayama[1], Toshifumi Imajo[3], Keisuke Yamamoto[1]
(1. Kyushu Univ. (Japan), 2. JSPS Research Fellow (Japan), 3. Univ. of Tsukuba (Japan))

3:30 PM - 3:45 PM

[E-2-06] Realization of Highly-Strained n-type Ge-on-Insulator by CW Laser Annealing

○Rahmat Hadi Saputro[1,2], Ryo Matsumura[1], Naoki Fukata[1,2] (1. NIMS (Japan), 2. Univ. of Tsukuba (Japan))

In order to enhance the quasi-direct band emission on Ge-based materials, we investigated the implementation of both tensile strain and n-type doping on the Ge-on-insulator (GeOI) structure. Our microsecond CW laser annealing technique was utilized to crystallize the Sb-doped Ge, and we successfully realized the highly tensile-strained n-type Ge-on-Insulator.

3:45 PM - 4:00 PM

[E-2-07 (Late News)] Real-Time and Atomic-Scale Observation of Local Solid-Phase Epitaxial Growth in Thin Silicon Film

○Manabu Tezura[1], Takanori Asano[1], Riichiro Takaishi[1], Mitsuhiro Tomita[1], Masumi Saitoh[1], Hiroki Tanaka[1] (1. KIOXIA Corp. (Japan))

Session information

Oral Presentation

10: Thin Film Electronics: Oxide / Non-single Crystalline / Novel Process

[E-3] Oxide Semiconductor TFT

Tue. Sep 27, 2022 4:15 PM - 6:00 PM 105 (1F)

Session Chair: Tsutomu Tezuka (KIOXIA Corp.), Cuan Liu (Sun Yat-sen Univ.)

4:15 PM - 4:45 PM

[E-3-01 (Invited)] Electrical Characteristic and Stability of Indium-Oxide Based Nanosheet Transistor with Different Metal Dopants

○Po-Tsun Liu[1], Zhen-Hao Li[1], Tsung-Che Chiang[1], Hsin-Hua Lee[1], Chun-Hao Tu[1] (1. NYCU (Taiwan))

4:45 PM - 5:00 PM

[E-3-02] Contiguous Plasma-Enhanced ALD for High-Performance Zinc Oxide TFTs

○Ben Daniel Rowlinson[1], Jiale Zeng[1], Vasilieos Mourgelas[1], Christian Patzig[2], Lutz Berthold[2], Joshua Daniel Akrofi[1], Martin Ebert[1], Harold Chong[1] (1. Univ. of Southampton (UK), 2. Fraunhofer Inst. IMWS (Germany))

Metal-oxide thin-film transistors are a promising technology for enabling future advances in display drivers
and heterogeneous integration. Plasma-enhanced atomic
layer deposition (PEALD) tools with multiple precursors
allow contiguous deposition of high-quality metal-oxide
semiconductors and insulators, which are deposited in sequence without breaking vacuum. We demonstrate low
hysteresis ZnO TFTs with mobility above 16 cm^2/(Vs),
subthreshold swing of 115 mV/dec, and on/off current
ratio of 2.5×10^9. Combining outstanding performance
across all parameters is rare in low-temperature ZnO TFTs
making our devices competitive with the state of the art and
highly attractive for future voltage driver circuits and heterogeneous integration.

5:00 PM - 5:15 PM

[E-3-03] High Performance Ta-Doped β-Ga_2O_3 MISFET with h-BN Dielectric and Its Carrier Scattering Mechanisms

○Xiao-Xi Li[1], Yu Sun[2], Yu-Chun Li[1], Rui Zhang[2], Chang-Tai Xia[3], Ying-Guo Yang[1], Hong-Liang Lu[1]
(1. Fudan Univ. (China), 2. Zhejiang Univ. (China), 3. Shanghai Inst. of Opt./Fine Mech., CAS (China))

5:15 PM - 5:30 PM

[E-3-04] Structural Relaxation of Rare-Metal-Free Oxide Semiconductors for Control of Bias Stress-Induced Instability in Solution-Processed Transistors

○Yu-Jin Hwang[1], Do-Kyung Kim[1], Sang-Hwa Jeon[1], Ziyuan Wang[1], Sin-Hyung Lee[1,2], In-Man Kang[1,2], Jaewan Jang[1,2], Jin-Hyuk Bae[1,2] (1. Eng of Electronic and electrical, Univ. of Kyungpook (Korea), 2. Eng of Electronics, Univ. of Kyungpook (Korea))

Here, we investigate the effects of structural relaxa-tion (SR) on bias stability in solution-processed Ra-re-metal-free Zinc-Tin-Oxide (ZTO) thin-film transistors (TFTs). To demonstrate the effects of SR, the annealing time of ZTO semiconductor was controlled. As the an-nealing time increased, the negative bias stress stability deteriorated due to the SR effect, especially increase of oxygen vacancy in ZTO. In contrast, the localized states near conduction band in ZTO decreased owing to the re-duction of the free volume and the stabilization of the local atomic condition by additional thermal energy as the annealing time increased. As a result, positive bias stress stability was improved by SR. This study might contribute to the optimization of semiconductor activa-tion for minimizing the negative and positive bi-as-induced instability of newly emerged rare-metal-free oxide semiconductor TFTs.

5:30 PM - 5:45 PM

[E-3-05] Atomic Layer Deposited Ultra-Thin Indium Zinc Oxide Channel Thin Film Transistor

Yan-Kui Liang[1], ○Wei-Li Lee[1], Jing-Wei Lin[1], Sih-Rong Wu[1], Tsung-Ying Yang[1], Li-Chi Peng[1], Tsung-Te Chou[2], Chi-Chung Kei[2], Edward-Yi Chang[1], Chun-Hsiung Lin[1]
(1. National Yang Ming Chiao Tung University (Taiwan), 2. Taiwan Instrument Research Institute, National Applied Research Laboratories (Taiwan))

5:45 PM - 6:00 PM

[E-3-06] Utilizing Dual-stacked IGZO channel structure to Achieve Optical Memories Application

○Kuan-Ju Zhou[1], Ting-Chang Chang[1], Simon M. Sze[2], Ya-Ting Chien[1], Po-Yu Yen[1]

(1. National Sun Yat-Sen University, Kaohsiung 80424, Taiwan. (Taiwan), 2. National Yang Ming Chiao Tung Hsinchu, 300, Taiwan. (Taiwan))

Through bandgap engineering, a dual-stacked IGZO channel layer device (IGZO with higher Zinc con-tent/IGZO) was fabricated. The more Zn content in IGZO, the larger the energy band gap, which can be used as a buried channel design. Buried channel designs can be used for lower subthreshold swing and higher mobility. In addition, using the characteristics of Zn in-terstitial and Zn vacancy hole traps of the more Zn con-tents IGZO channel layer can cause the threshold voltage shift. Therefore, this device structure can be effectively used for optoelectronic memory storage during the oper-ation of dual-gate IGZO TFTs.

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-1] Ferroelectric Memory Materials

Tue. Sep 27, 2022 11:30 AM - 12:30 PM 201 (2F)

Session Chair: Halid Mulaosmanovic (GlobalFoundries), Norikatsu Takaura (Hitachi, Ltd.)

11:30 AM - 11:45 AM

[F-1-01] Fabrication of Thin Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Film by Millisecond Flash Lamp Annealing

Yasuo Nara[1], Yuto Ota[1], ○Hideaki Tanimura[2], Hikaru Kawarazaki[2], Shin'ichi Kato[2]
(1. Univ. of Hyogo (Japan), 2. SCREEN Semiconductor Solutions Co., Ltd. (Japan))

A ferroelectric Hf0.5Zr0.5O2 (HZO) thin film was formed by a short-time heat treatment using flash lamp annealing. For 10nm thick HZO, remnant polarization of about 30 uC/cm2 was obtained with higher endurance than RTA treatment. Further improvement of endurance was confirmed for thinner (5nm) HZO film.

11:45 AM - 12:00 PM

[F-1-02] Formation of ferroelectric ZrO_2 film in ultra-thin region by sputtering method

○Shigehisa Shibayama[1], Jotaro Nagano[1], Mitsuo Sakashita[1], Osamu Nakatsuka[1,2]
(1. Nagoya Univ. (Japan), 2. IMaSS, Nagoya Univ. (Japan))

We examined the formation of ultra-thin ferroelectric ZrO2 films on the TiN bottom electrode using a sputtering method in conjunction with post oxidation treatment. We found that high-temperature sputtering and post plasma oxidation at room temperature successfully forms ferroelectric ZrO2 films. Furthermore, we demonstrated the formation of ferroelectric ZrO2 in the ultra-thin region down to 6 nm. Finally, we discussed the possibility of further improvement of the ZrO2 ferroelectricity.

12:00 PM - 12:15 PM

[F-1-03] Conflicting Effect of Oxygen Vacancy in the Bulk and at the Interface on Endurance of $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Thin Film

○Danyang Chen[1], Tianning Cui[1], Shuman Zhong[1], Liying Wu[1], Jingquan Liu[1], Mengwei Si[1], Xiuyan Li[1]
(1. Shanghai Jiao Tong Univ. (China))

This paper discusses two sides to oxygen vacancy (Vo) in endurance of Hf0.5Zr0.5O2 ferroelectric films: 1) Vo in the bulk improves the endurance with a strong wake-up effect due to enhancing the formation of tetragonal phase, and 2) Vo at the interface degrades the endurance with easier breakdown. Cutting off the kinetic linkage between two kinds of Vo is a key to the endurance enhancement.

12:15 PM - 12:30 PM

[F-1-04] Demonstration of Ultra-thin Sub-10 nm Indium Oxide (In_2O_3) Field-Effect-Transistors (FETs) by Sputtering Deposition with Annealing-Free Toward BEOL Memory Applications

Zhao-Feng LOU[1], Chun-Yu Liao[1], Kuo-Yu Hsiang[1,2], Chen-Ying Lin[1], Jia-Yang Lee[1], Pin-Huan Chen[3], Wei-Chang Ray[1], Zhi-Xian Li[1], Han-Chen Tseng[1], Fu-Sheng Chang[1], Chun-Chieh Wang[1], Jeng-Han Tsai[3], Ming-Han Liao[4], ○Min-Hung Lee[1]
(1. Inst. and Undergraduate Program of Electro-Optical Engineering, National Taiwan Normal Univ. (Taiwan), 2. Department of Electronics Engineering, National Yang Ming Chiao Tung Univ. (Taiwan), 3. Department of Electrical Engineering, National Taiwan Normal Univ. (Taiwan), 4. Department of Mechanical Engineering, National Taiwan Univ. (Taiwan))

Sub-10 nm In2O3 Field-Effect-Transistors (FETs) by sputtering deposition with annealing-free is demonstrated for high on/off ratio 106 and low operation voltage 4V. The ultra-thin 4 nm and 10 nm of In2O3 are validated by HR-TEM and EDS, as well as the mobility extracted as 1 cm2/V.s and 4 cm2/V.s, respectively. The FeMFET of the proposed In2O3 FET with ferroelectric HfZrO2 capacitor shows hysteretic Threshold voltage shift for memory capability and is feasible for back end of line (BEOL) application.

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-2] PCM, MRAM, and RRAM

Tue. Sep 27, 2022 2:00 PM - 3:30 PM 201 (2F)

Session Chair: Atsushi Himeno (Panasonic Corporation), Laurent Grenouillet (CEA-Leti)

2:00 PM - 2:15 PM

[F-2-01] Study of Write Error Rate in MRAM with Fixed Voltage Input

○Lihua An[1], Yue Xin[1], Zhengping Yuan[1], Yumeng Yang[1], Zhifeng Zhu[1] (1. ShanghaiTech Univ. (China))

The write error rate (WER) is studied in the bit cell driven by a fixed voltage. A new simulation framework is developed to enable the co-simulation of magnetic tunnel junction (MTJ) and transistor. In contrast to the commonly known result, the WER has a significant dependence on the device properties such as the resistance and the area of MTJ. For the devices studied here, the WER decreases from 31% to 3% as the resistance is increased from 1kΩ to 6kΩ, and the WER increases from 31% to 67% when the area is increased from 50nm×50nm to 100nm×100nm. In addition, our results show that the device with a higher resistance-area product can be more attractive when one has a strict requirement on the WER.

2:15 PM - 2:30 PM

[F-2-02] Improved State Stability of PCMO-based RRAM by Asymmetric Programming Voltage for Convolutional Kernels

○Eunryeong Hong[1], Seonuk Jeon[2], Heebum Kang[1], Hyun Wook Kim[1], Nayeon Kim[1], Kibong Moon[3], Jiyong Woo[1]
(1. Kyungpook National University, School of Electronic and Electrical Engineering (Korea), 2. Kyungpook National University, School of Electronics Engineering (Korea), 3. Pohang University of Science and Technoloy, Department of Materials Science and Engineering (Korea))

2:30 PM - 2:45 PM

[F-2-03] Effect of SiN Sidewall and Reference-Layer-Thickness Dependence of MR Ratio for High Performance STT-MRAM

○Yoshiteru Amemiya[1], Junichi Tsuchimoto[1,2], Hiroyuki Hosoya[2], Hiroki Nakanishi[1], Chihiro Watanabe[1], Akinobu Teramoto[1]
(1. Hiroshima Univ. (Japan), 2. CANON ANELVA Corp. (Japan))

For high performance spin transfer torque magnetic random access memory (STT-MRAM), an ion beam etch-ing (IBE) is improved and a thickness of reference layer is controlled. In the improved process, a fabrication pro-cess of SiN sidewall is included. Magnetoresistance (MR) ratio of the fabricated device with the IBE angle of 20° becomes larger than that of 60° because of edge current suppression by the SiN sidewall and etching damage sup-pression by decreasing IBE angle. The thickness depend-ence of the reference layer is investigated, when the refer-ence layer is FeB and the thickness is 0.7, 0.9 or 1.05 nm. The MR ratio increases with increase of the reference layer thickness. The MR ratio of ~180% can be achieved, when the FeB thickness is 1.05 nm.

2:45 PM - 3:00 PM

[F-2-04] $Hf_{1-x}Zr_xO_2$ RRAM Prepared via Co-Sputtering with High Uniformity, Fast Switching Time of 10 ns, and Low Switching Energy of 20 pJ

○Quanzhou Zhu[1], Jun Lan[1], Bing Zhou[1], Muhammad Zaheer[1], Jinxuan Liang[1], Peng Chen[1], Feichi Zhou[1], Longyang Lin[1], Guobiao Zhang[1], Mei Shen[1], Xuewei Feng[2], Zhen Chen[3], Zhixiong Li[3], Yida Li[1]
(1. Southern University of Science and Technology (China), 2. Shanghai Jiao Tong University (China), 3. Shenzhen Longsys Electronics Co., Ltd (China))

In this work, the performance enhancement of HfxZr1-xO2 (HZO) using co-sputtering is reported. The HZO RRAMs shows reduced operating voltages (by 30%) as compared to control HfO2 and ZrO2 RRAMs respectively, attributed to the increase of oxygen vacancies as a result of the Zr alloying. Consequently, DC endurance greater than 350 cycles, retention time exceeding 104 s, fast switching time down to 10 ns, and switching energy of 20 pJ were achieved. Furthermore, characterization of multiple HZO RRAMs shows excellent uniformity (coefficient of variation less than 0.8), thus paving a potential path-way for further development of HZO RRAM for use in future storage and computing applications.

3:00 PM - 3:15 PM

[F-2-05] Investigation of Structure Evolution and Oxygen-ion Migration in LaCoOx-Based Resistance Random Access Memory

○Yen Jung Chen[1], Hung-Yang Lo[1], Jan-Chi Yang[2], Wen-Wei Wu[1]
(1. National Yang Ming Chiao Tung University (Taiwan), 2. National Cheng Kung University (Taiwan))

Resistive switching occurs in a wide range of materials among the transition metal oxides (TMO) . In this work, we utilize epitaxial ternary metal oxides layer, LaCoOx (LCO), which grows on Nb-doped SrTiO3 (Nb-STO) substrate as RRAM device. We deposited Au/Ti metal as the top electrode, and measured the SET and RESET process with more than 900 cycles. In order to reveal the resistive switching behaviors, we use the TEM and STEM to observe the structure evolution and oxygen-ion migration in LaCoOx.
From the TEM results and corresponding Fast-Fourier-Transform Diffraction pattern (FFT-DP), the functionalities of LaCoOx films can be manipulated by distinct voltage. It is clearly demonstrated that the structure changes from monocrystalline to polycrystalline. This study not only revealed the oxygen-ion migration of LaCoOx but also proved it to be the promising candidate for RRAM application.

3:15 PM - 3:30 PM

[F-2-06] Breaking the Thermal Stability Limit of Phase-Change Materials for Embedded Memory thanks to Innovative N-doped $GeSe_{1-x}Te_x$ Alloys

○Martina Tomelleri[1,2], Anthony Albanese[1], Chiara Sabbione[1], Niccolo Castellani[1], Christophe Licitra[1], Valentina M. Giordano [3], Daniel Benoit[2], Francoise Hippert[4], Pierre Noe[1]
(1. Inst. CEA-LETI, F-38000, Grenoble (France), 2. Indus. STMicroelectronics, F-38926 Crolles (France), 3. ILM, UMR 5306 Univ. Lyon 1-CNRS, F-69622 Villeurbanne Cedex (France), 4. Univ. Grenoble Alpes, CNRS, Grenoble INP, LMGP, F-38000 Grenoble (France))

Recently, we revealed the unprecedented high thermal stability offered by the novel chalcogenide phase-change GeSe1-xTex alloys. The latter is of paramount interest for non-volatile PCM memory requiring high-temperature data retention. Herein, we investigate for the first time the effect of N incorporation in Ge-Se-Te thin films. We show that the thermal and programming performances in device can be potentially boosted thanks to the addition of ~10 at.% of nitrogen, making N-doped GeSe1-xTex an extremely promising material for embedded PCM memories.

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-3] Ferroelectric Devices

Tue. Sep 27, 2022 4:15 PM - 6:00 PM 201 (2F)

Session Chair: Laurent Grenouillet (CEA-Leti), Hiroshi Naganuma (Tohoku Univ.)

4:15 PM - 4:45 PM

[F-3-01 (Invited)] HfO2–based FeRAM, from material perspective to circuit application

○Jean Coignus[1], Terry Francois[1], Julie Laguerre[1], Simon Martin[1], Catherine Carabasse[1], Nicolas Vaxelaire[1], Adam Makosiej[2], Bastien Giraud [2], Francois Andrieu [1], Laurent Grenouillet[1] (1. CEA-Leti (France), 2. CEA-LIST (France))

4:45 PM - 5:00 PM

[F-3-02] Physical Origin of Ferroelectric-like Behaviors in MIM with Amorphous Dielectric

○Huan Liu[1], Jing Li[2], Chengji Jin[1], Jiajia Chen[1], Ze Feng[3], Yan Liu[2], Hong Dong[3], Xiao Yu[1], Genquan Han[2]
(1. Zhejiang Lab (China), 2. Xidian University (China), 3. Nankai University (China))

The physical origin of the ferroelectric-like character-istics in metal-insulator-metal (MIM) structures with amorphous (a-) dielectric enabled by oxygen ions (O2-) and vacancies (Vo2+) migration are systematically inves-tigated by modulating the metal-insulator interface and dielectric thickness. It is found that O2- and Vo2+ origi-nate from the interface between metal nitride and a-ZrO2 film, drifting through the path in a-ZrO2 film un-der the applied electric field to form the long-range movement induced polarization. Furthermore, the po-larization has a thickness-dependent saturation due to ions pinning.

5:00 PM - 5:15 PM

[F-3-03] Universal Phase Transition on the Polarization Switching Cycling of Antiferroelectric/Ferroelectric $Hf_xZr_{1-x}O_2$ towards high endurance performance

○Danyang Chen[1], Shuman Zhong[1], Tianning Cui[1], Liying Wu[1], Jingquan Liu[1], Mengwei Si[1], Xiuyan Li[1]
(1. Shanghai Jiao Tong Univ. (China))

In this paper, we clarify a universal route of tetragonal-orthorhombic-monoclinic (T-O-M) phase transition on the polarization switching cycling of antiferroelectric/ferroelectric HfxZr1-xO2 (AFE/FE-HZO) system and develop a phase engineering method toward high endur-ance of AFE/FE memory devices. In addition, a 1012 endurance on 6 nm AFE HZO under 4.5 MV/cm and 1 MHz is achieved to demonstrate the potential of this strategy.

5:15 PM - 5:30 PM

[F-3-04] Electrical Assessment of Scaled HfO_2-Based BEOL-Integrated FTJs Leading to Multi-Level Capability Demonstration

○Justine Barbot[1], Jean Coignus[1], François Triozon[1], Catherine Carabasse[1], Olivier Glorieux[1], François Aussenac[1], François Andrieu[1], Laurent Grenouillet[1] (1. CEA-Leti, Univ. Grenoble Alpes, F-38000 Grenoble, France (France))

CMOS compatible TiN/HfO2:Si/Al2O3/TiN Ferroelectric Tunnel Junctions (FTJs) integrated in a 130nm Back-End of Line (BEOL) process are reported. FTJ device operation de-pendence on cycling conditions is assessed. Switching kinetic of FTJ is then studied and yields to the successful programming of four read-disturb-free conductance levels. These results confirm the potential of bilayer FTJs for scalability and future neuromorphic applications.

5:30 PM - 5:45 PM

[F-3-05] Nanosecond Laser Annealing Based Wake-up of Ferroelectric $HfZrO_2$ Capacitors for BEOL Compatible and High Throughput FeRAM

○Jia-Yang - Lee[1,2], Kuo-Yu Hsiang[1,3], Chun-Yu Liao[1], Zhao-Feng Lou[1], Chen-Ying Lin[1], Song-Lin Tang[1], Fu-Sheng Chang[1], Zhi-Xian Li[1], Wei-Chang Ray[1], Han-Chen Tseng[1], Chun-Chieh Wang[1], Ming-Han Liao[4], Chee-Wee Liu[2], Min-Hung Lee[1]
(1. Inst. and Undergraduate Program of Electro-Optical Eng. , National Taiwan Normal Univ. (Taiwan), 2. Graduate School of Advance Tech. , National Taiwan Univ. (Taiwan), 3. Inst. of Electronics, National Yang Ming Chiao Tung Univ. (Taiwan), 4. Department of mechanical engineering, National Taiwan Univ. (Taiwan))

Novel wake-up procedure is proposed by nanosecond laser annealing (NLA), and the outstanding delta 2Pr and low temperature process (lower than 400oC for underneath layer) are demonstrated. The general wake-up by E-field cycling makes mass production difficult due to individual device step by step. The proposed method is feasible for BEOL compatible and high throughput FeRAM.

5:45 PM - 6:00 PM

[F-3-06 (Late News)] Read-disturb & Data-retention Error-robust and Fast Training Methods of FeFET LM-GA CiM for Hyperdimensional Computing

Eitaro Kobayashi[1], ○Chihiro Matsui[1], Naoko Misawa[1], Ken Takeuchi[1] (1. Univ. of Tokyo (Japan))

Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[G-1] Cryo-CMOS

Tue. Sep 27, 2022 11:30 AM - 12:45 PM 301 (3F)

Session Chair: Sakura Takeda (NAIST), Anabela Veloso (imec)

11:30 AM - 11:45 AM

[G-1-01] Substrate Impurity Concentration Dependence of Sub-threshold Swing of Si n-Channel MOSFETs at Cryogenic Tempeartures down to 4 K

○Min-Soo Kang[1], Kei Sumita[1], Hiroshi Oka[2], Takahiro Mori[2], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1]
(1. Univ. of Tokyo (Japan), 2. National Inst. of Advanced Indus. Sci. and Tech. (AIST) (Japan))

The sub-threshold swing (SS) of Si n-MOSFETs is experimentally and systematically evaluated in a temperature range of 4 K to 300 K with varying the substrate impurity concentration (Nsub) from ~1016 cm-3 to ~1018 cm-3, to obtain a physical understanding of SS at cryogenic temperatures. It is clarified that the temperature and ID dependencies of SS in n-MOSFETs are well described by both mobile tail states and localized interface states, irrespective of Nsub, and that the densities of these states increase with increasing Nsub. A physical origin of the tail states is studied by examining the impact of substrate bias (Vsub) on the tail state width to separate the effects of substrate impurity concentrations and electric field. It is found, as a result, that the band tail states can be explained by the Lifshitz model.

11:45 AM - 12:00 PM

[G-1-02] Electron mobility of Si nMOSFETs in a nonlinear model of surface roughness scattering at cryogenic temperature

○Kei Sumita[1], Min-Soo Kang[1], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1] (1. Univ. of Tokyo (Japan))

Surface roughness (SR) scattering in MOSFETs is of great interest because it is a dominant scattering mechanism of electrons in nanosheet channels and at cryogenic temperature. Recently, the accurate nonlinear model of SR scattering has been reported. However, the validity of this nonlinear model at cryogenic temperature has been not examined yet. In this study, we report that when the mobility of the Δ4 valley is underestimated, the calculated mobility agrees very well with the experimental values, suggesting a new physical model that the Δ4 valley electrons are occupied at 4.2 K in tail states with low mobility.

12:00 PM - 12:15 PM

[G-1-03] Anomalous Threshold Voltage Increase due to the Depletion of Extension Edges in Cryogenic MOSFETs

○Takumi Inaba[1], Hidehiro Asai[1], Junichi Hattori[1], Koichi Fukuda[1], Hiroshi Oka[1], Takahiro Mori[1]
(1. National Inst. of Advanced Indus. Sci. and Tech. (Japan))

Anomalous threshold voltage increase was observed from short-channel bulk p-MOSFETs operating in the linear-mode. Because the increase was suppressed in the saturation-mode, a threshold voltage mismatch between
the linear- and saturation-mode increased as if drain-induced barrier lowering increased. On the basis of cryogenic TCAD simulation, the increase was attributed to the depletion of extension edges at cryogenic temperature.

12:15 PM - 12:30 PM

[G-1-04] Accurate Evaluation of Interface Trap Density at InAs MOS Interfaces by Using C-V characteristics at Low Temperatures

○Ryohei Yoshizu[1], Kei Sumita[1], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1] (1. Univ. of Tokyo (Japan))

A method of accurately evaluating the interface trap density (Dit) by using the high-frequency C-V curves at InAs MOS interfaces is experimentally examined. Low-temperature measurements are performed to suppress the response of interface states. We study the impacts of the accuracy of the oxide capacitance, the distribution function, and the C-V hysteresis due to slow traps on Dit evaluated by the high-frequency C-V (Terman) method. It is found that temperatures lower than 40 K and the C-V measurements in limited voltage ranges are indispensable in the accurate evaluation of Dit.

12:30 PM - 12:45 PM

[G-1-05 (Late News)] Temperature Dependence of MOSFET Series Resistance from 300 K to 4 K

○Kiyoshi Takeuchi[1], Tomoko Mizutani[1], Takuya Saraya[1], Hiroshi Oka[2], Takahiro Mori[2], Masaharu Kobayashi[1], Toshiro Hiramoto[1] (1. Univ. of Tokyo (Japan), 2. AIST (Japan))

Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[G-2] Modeling, Simulation and Characterization

Tue. Sep 27, 2022 2:00 PM - 4:00 PM 301 (3F)

Session Chair: Satofumi Souma (Kobe Univ.), Seongjae Cho (Gachon Univ.)

2:00 PM - 2:30 PM

[G-2-01 (Invited)] Opportunity of Deep Learning Applicable to TCAD

○Sanghoon Myung[1], Byungseon Choi[1], Wonik Jang[1], Jinwoo Kim[1], In Huh[1], Jae Myung Choe[1], Young-Gu Kim[1], Dae Sin Kim[1]
(1. Samsung Electronics (Korea))

2:30 PM - 2:45 PM

[G-2-02] An Atomistic Study of Thermal Conductance in Novel GeC Channel Materials

○Shao Chen Lee[1], Yu Ting Chen[1], Cheng Rui Liu[1], Sheng Min Wang[1], Ying Tsan Tang[1] (1. National Central University (Taiwan))

Silicon carbide (4H-SiC) has been considered as one of the future candidates for power electronics components, ena-bling smaller size, faster switching speed, higher reliability, and higher efficiency than silicon-based MOSFETs. To date, however, the thermal performance of Si-Ge-C-based power MOSFETs is unclear. This work explains the thermal prop-erties of Si1-xGexC by simulating the thermal conductivity through molecular dynamics (MD) and proposes a novel low leakage, high thermal conductivity and high power 4H-GeC MOSFET device.

2:45 PM - 3:00 PM

[G-2-03] Large Radiation Damages to Si MOS Devices Induced by Intermediate Energy Region X-ray Irradiation

○Naohiro Matsukawa[1], Koichiro Inoue[1], Takao Sueyama[1] (1. KIOXIA Corp. (Japan))

It is found that medium energy X-ray irradiation causes greater, more than one order of magnitude, damages than high energy X-ray irradiation in Si MOSFETs. This phenomenon could be attributed to larger X-ray absorption by photoelectric effect in medium energy region, and smaller X-ray absorption caused by the Compton effect in high energy region. X-ray energy dependent radiation damages, therefore, should be seriously considered to evaluate exact radiation hardness of the Si MOS devices.

3:00 PM - 3:15 PM

[G-2-04] Resistance Modeling of Short-range Connections: Impact of Current Spreading

○Davide Tierno[1], Victor Vega-Gonzalez[1], Simone Esposto[1], Ivan Ciofi[1] (1. imec (Belgium))

We investigated the impact of current spreading (CS) on the resistance of short-range connections by performing simulations in Synopsys Sentaurus, based on a calibrated resistivity model. As a case study, we considered Vertical-Horizontal-Vertical (VHV) middle-of-line (MOL) connections, recently introduced to boost the routing of 4-Track (4T) standard cells (SDC). We analyzed the impact of via and line geometry on VHV link resistance (RLink). We found that low aspect ratios (AR) lines are needed to minimize the average SDC resistance (RSDC). We performed extensive resistance simulations of various short-range connections and concluded that large AR lines are indeed detrimental when RLink is dominated by the vias. Finally, we show that ignoring CS can lead to significant miscalculations of Rlink in such scenarios.

3:15 PM - 3:30 PM

[G-2-05] Drain Current Variability Assessment in 2-levels Stacked Nanowire Gate All Around Field Effect Transistors

○Donghyun Kim[1,2], Sylvain Barraud[3], Jae Woo Lee[2], Gerard Ghibaudo[1], Christoforos Theodorou[1]
(1. Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, Grenoble INP, CNRS, IMEP-LAHC (France), 2. Electronics and info. engineering, Korea Univ. (Korea), 3. Univ. Grenoble Alpes, CEA, LETI (France))

3:30 PM - 3:45 PM

[G-2-06] *Ab initio* investigation of Ga doping in $Si_{1-x}Ge_x$: effect of biaxial strain and interaction of dopants with point-defects

○Gianluca Rengo[1,2,3], Geoffrey Pourtois[2,4], Clement Porret[2], Roger Loo[2], André Vantomme[1]
(1. QSP, KU Leuven (Belgium), 2. imec (Belgium), 3. Research Foundation - Flanders (FWO) (Belgium), 4. Plasmant, University of Antwerp (Belgium))

Ga doping in Si1-xGex is studied through density functional theory calculations. The preferential Ga local atomic environment is investigated revealing that Ge nearest neighbors are energetically favored over Si atoms. In Si0.5Ge0.5 the interaction of the Ga dopant with (i) another substitutional Ga atom, and (ii) a vacancy defect is simulated. The binding energy is found to be positive for the Ga-V complex formation.

3:45 PM - 4:00 PM

[G-2-07 (Late News)] Temperature Effects on Static Characteristics of Complementary Field-Effect Transistors with Si and Ge Nanosheets

○Junichi Hattori[1], Koichi Fukuda[1], Tsutomu Ikegami[1], Wen Hsin Chang[1] (1. AIST (Japan))

Session information

Oral Presentation

Focus Session 1 (Area1&2&9)

[G-3] Quantum Computing 1

Tue. Sep 27, 2022 4:15 PM - 5:45 PM 301 (3F)

Session Chair: Jun Yoneda, Masahiko Ishida (NEC Corp.)

4:15 PM - 4:45 PM

[G-3-01 (Invited)] Quantum Computation - Spins Inside

○Lieven Vandersypen[1] (1. Delft Univ. of Tech. (Netherlands))

4:45 PM - 5:00 PM

[G-3-02] Introduction of deep impurity levels of S and Zn and high temperature single-electron transport in Si tunnel FETs

○Yoshisuke Ban[1], Kimihiko Kato[2], Shota Iizuka[2], Shigenori Murakami[2], Koji Ishibashi[1], Satoshi Moriyama[3], Takahiro Mori[2], Keiji Ono[1] (1. RIKEN (Japan), 2. AIST (Japan), 3. Tokyo Denki Univ. (Japan))

We introduced deep impurity levels with strong electron confinement into Si devices for high temperature operation of Si qubit and observed single-electron transport through the deep levels. First, Group II-VI impurities, S and Zn, were introduced into the Si substrate by ion implantation as deep impurities, and post-implantation annealing condition was found from the depth profiles of S and Zn measured by SIMS. Next, the formation of deep levels in Si was confirmed by DLTS analyses. Then, we performed the process integration into Si devices under the S and Zn I/I condition found in the above experiments. To realize single-electron transport through deep impurity levels, we employed a single-electron transistor with a tunnel FET structure. Finally, as a result of the evaluation of S and Zn implanted Si TFETs, large charging energy values were observed at 10 K and 300 K. These values are 10 - 20 times higher than room temperature, suggesting high temperature stability as a Si qubit.

5:00 PM - 5:15 PM

[G-3-03] Device Structure and Fabrication Process for MOS Type Silicon Spin Qubit Realizing Process-Variation-Robust two-Qubit SWAP Gate

○Hidehiro Asai[1], Shota Iizuka[1], Tohru Mogami[1], Junichi Hattori[1], Koichi Fukuda[1], Tsutomu Ikegami[1], Kimihiko Kato[1], Hiroshi Oka[1], Takahiro Mori[1] (1. National Institute of Advanced Industrial Science and Technology (AIST) (Japan))

In this study, we propose a device structure, gate fabrication process, and back-bias-assisted operation for Si spin qubits, to realize high robustness of two-qubit SWAP gate operation against process variations. For the first time, we present a novel qubit design for 6σ yield SWAP gate operation with 99% fidelity assuming device size fluctuation of the IRDS target for 2022. These technologies provide a solution to complete a universal quantum gate set realizing universal quantum computers with silicon.

5:15 PM - 5:30 PM

[G-3-04] Long-term Characteristic Stabilization of a Semiconductor Double Quantum Dot Based on a Multi-dimensional Gradient Descent Technique

○Chutian WEN[1], Hiroki Takahashi[1], Sayyid Irsyadul Ibad[1], Shimpei Nishiyama[1,2], Kimihiko Kato[2], Yongxun Liu[2], Shigenori Murakami[2], Takahiro Mori[2], Raisei Mizokuchi[1], Jun Yoneda[1], Tetsuo Kodera[1]
(1. Tokyo Inst. of Tech. (Japan), 2. National Inst. of Advanced Indus. Sci. and Tech. (Japan))

5:30 PM - 5:45 PM

[G-3-05] Electrically-addressable engineering in self-assembled Ge double quantum-dots for CMOS integratable quantum electronic devices

○Yu Ju Chiu[1], I Hsiang Wang[1], Pei Wen Li[1] (1. National Yang Ming Chiao Tung Univ. (Taiwan))

We reported a CMOS approach for fabricating germanium double quantum dots with inter-QD coupling barrier of Si3N4 or Si-fin. Individual QDs and their inter-QD coupling barrier are electrically addressable by individual, well-isolated electrodes through self-organized dielectric layers using spacer and self-assemble technologies. Based on a pre-patterned Si-fin that is designed to serve as coupling barrier, poly-Si source/drain reservoirs self-align with the Si-fin barrier via Si3N4 spacer layers.

Session information

Oral Presentation

08: Low Dimensional Devices and Materials

[H-1] Characterization I: Low Dimensional Devices and Materials

Tue. Sep 27, 2022 11:30 AM - 12:30 PM 302 (3F)

Session Chair: Takayuki Arie (Osaka Metropolitan Univ.), Reina Kaji (Hokkaido Univ.)

11:30 AM - 11:45 AM

[H-1-01] Generation of Hollow Beam from GaAs/InGaAs/GaAs Core-multishell Nanowire Cavity

○Taiga Kunimoto[1,2], Shinjiro Hara[1,2], Junichi Motohisa[1,2]
(1. Graduate School of Info. Sci. and Tech., Hokkaido Univ. (Japan), 2. Res. Center for Integrated Quantum Electronics (RCIQE) (Japan))

We characterized the beam profiles and polarization states in low-temperature photoluminescence (PL) from a GaAs/InGaAs/GaAs core-multishell nanowire (NW) under CW and pulsed excitations. In the beam profile observation under pulsed excitation, we observed a doughnut-shaped intensity distribution. The beam was also shown to exhibit an axisymmetric distribution in the polarization. These observations indicate that vector beams are generated from the NW. Observed polarization do not correspond to low-order modes of vector beams, suggesting the presence of complicated polarized states reflecting the cavity modes in NWs.

11:45 AM - 12:00 PM

[H-1-02] Atomistic Modeling of Electronic Structure of Disordered InP Quantum Dots

○Jin Hyong Lim[1], Nobuya Mori[1] (1. Osaka Univ. (Japan))

The electronic structures of disordered InP quantum dots (QDs) are investigated using an empirical tight-binding (TB) method. The bandgaps of InP QDs with different shapes and sizes are computed, and the effect of surface roughness on the bandgap is investigated. The relationship between the bandgap changes and the modulus squared of the wavefunction is also discussed.

12:00 PM - 12:15 PM

[H-1-03] Time-resolved measurements of electron-nuclear spin dynamics via anomalous Hanle effect in a single semiconductor quantum dot

○Reina Kaji[1], Sota Yamamoto[1], Satoru Adachi[1] (1. Hokkaido Univ. (Japan))

Formation of a large in-plane nuclear field Bn under transverse magnetic fields, known as the anomalous Hanle effect, was studied comprehensively in a single quantum dot. From the time-resolved measurements, the buildup time of the in-plane Bn was revealed. Further, the impact of the sign inversion of longitudinal Bn exhibited discrepancies between experiments and calculations, which led us to reconsider the previously proposed model. The newly developed model successfully explained the experimental data, and it suggests that the anomalous Hanle effect is an indication of a large distribution of principal axis of nuclear quadrupole interaction.

12:15 PM - 12:30 PM

[H-1-04] Piezoelectricity of the hBN/1L-MoS_2 heterostructure membrane

Calvin Chiba[1], Shota Sugawara[1], Emi Kitayoshi[1], Kenji Watanabe[2], Takashi Taniguchi[2], Kentarou Sawano[1], Hiroyuki Fujita[1], ○Yusuke Hoshi[1] (1. Tokyo City Univ. (Japan), 2. NIMS (Japan))

We investigate the piezoelectricity of the hBN/1L-MoS2 van der Waals heterostructure membrane on the microtrench cavity. It is demonstrated that the 1L-MoS2 can be pulled together with the multilayered hBN by the back-gate bias tuning due to the Coulomb interaction. Furthermore, we show the response of the piezoelectric voltage generated between graphite source-drain electrodes under the cyclical DC back-gate voltage.

Session information

Oral Presentation

09: Novel Functional / Quantum / Spintronic Devices and Materials

[H-2] Novel Function Devices

Tue. Sep 27, 2022 2:00 PM - 3:45 PM 302 (3F)

Session Chair: Kensuke Ota (KIOXIA Corp.), Yoshifumi Nishi (Toshiba Corp.)

2:00 PM - 2:30 PM

[H-2-01 (Invited)] In-Materio Reservoir Computing Devices of Random Network Nanoparticles for Autonomous robotics

○Hirofumi Tanaka[1] (1. Kyushu Institute of Technology (Japan))

2:30 PM - 2:45 PM

[H-2-02] An Ultra-low-voltage Synaptic Behavior of WO_3/Pd based 2-terminal Protonic Memristive Device

○Satya Prakash Pati[1], Satoshi Hamasuna[1], Takeaki Yajima[1] (1. Kyushu University (Japan))

Memristive devices are basic building blocks for de-signing memory and logic circuits. Conventional resis-tive switching by ion transport in solid state devices suf-fers from poor reproducibility and high-power con-sumption. Herein, we demonstrate a simple two terminal protonic solid-state device which rely on electrochemical change of conductance state. This alternative synaptic device comprising of a WO3 conducting channel and a Pd reservoir. Electric field control of protonation and deprotonation results in conductance change in WO3 over several orders of magnitude. Moreover, protons being smallest ion and their barrier free motion in this device structure offers low energy switching of con-ductance state for ultra-low power consumption neuro-morphic computing.

2:45 PM - 3:00 PM

[H-2-03] Amorphous GaO_x Crossbar Array Memristors for Artificial Synaptic Devices

○Naoki Masaoka[1], Yusuke Hayashi[1], Tetsuya Tohei[1], Akira Sakai[1] (1. Osaka Univ. (Japan))

3:00 PM - 3:15 PM

[H-2-04] The impact of floating gate insertion regarding channel percolation of ferroelectric FET

○Sangho Lee[1], Giuk Kim[1], Taehyong Eom[1], Sanghun Jeon[1] (1. Korea Advanced Institute of Science and Technology (KAIST) (Korea))

As the scaling of ferroelectric FET (FeFET) progresses, channel percolation caused by random distribution of the ferroelectric film's crystal phase has been recognized as a primary issue. We investigated a structural approach to minimize device-to-device variance and performance degradation due to spatial variations of crystal phase, which worsens with the scaling of FeFETs, using technol-ogy computer-aided design (TCAD) simulations. By in-serting a floating gate below the ferroelectric film, the influence of ferroelectric polarization on the lower chan-nel can be averaged, thus reducing device variation sig-nificantly. At the same time, it results in a larger MW of FeFETs and a significant improvement in accuracy of in-memory computing applications. We believe that a floating gate insertion will be a key structural strategy for enhancing FeFET reliability.

3:15 PM - 3:30 PM

[H-2-05] Electron temperature in semiconductor double barrier thermionic cooling heterostructures

○Xiangyu Zhu[1], Marc Bescond[1,2], Gerald Bastard[3], Naomi Nagai[1], Kazuhiko Hirakawa[1,2,4]
(1. IIS, Univ. of Tokyo (Japan), 2. LIMMS-CNRS, Univ. of Tokyo (Japan), 3. ENS PSL (France), 4. INQIE, Univ. of Tokyo (Japan))

We investigate electron transport in asymmetric double-barrier (Al, Ga)As/GaAs thermionic cooling heterostructures. To establish quantitative understanding, we develop an intuitive analytical model for sequential electron transport and energy balance in the two-dimensional quantum well (QW). The electron temperature in the QW is calculated and compared with the results obtained from voltage-dependent photoluminescence measurements.

3:30 PM - 3:45 PM

[H-2-06] Low Temperature Operation of 2DHG Diamond FETs with Superconducting Diamond Sources and Drains aiming at JoFET or SCFET operation

○Chiyuki Wakabayashi[1], Yasuhiro Takahashi[1], Taisuke Kageura[2], Yoshihiko Takano[3], Minoru Tachiki[3], Shuuichi Ooi[3], Shunichi Arisawa[3], Hiroshi Kawarada[1,4]
(1. Waseda Univ. (Japan), 2. National Inst. of Advanced Indus. Sci. and Tech. (Japan), 3. MANA National Inst. for Materials Science (Japan), 4. The Kagami Memorial Res. Inst. for Materials Sci. and Tech. (Japan))

We fabricated Diamond FETs with two-dimensional hole gas (2DHG) diamond channels and superconducting boron-doped diamond sources and drains aiming at JoFET or SCFET operation. The channel was miniaturized down to 200 nm. As a result, FETs were operated in cryogenic environments down to 1.6 K.

Session information

Oral Presentation

08: Low Dimensional Devices and Materials

[H-3] Characterization II: Low Dimensional Devices and Materials

Tue. Sep 27, 2022 4:15 PM - 6:00 PM 302 (3F)

Session Chair: Toshifumi Irisawa (AIST), Fumitaro Ishikawa (Hokkaido Univ.)

4:15 PM - 4:30 PM

[H-3-01] Revealing the role of oxygen on defect formation of MoS_2 by combining thermal desorption spectroscopy and atomic layer deposition

○Shuhong Li[1], Tomonori Nishimura[1], Mina Maruyama[2], Susumu Okada[2], Kosuke Nagashio[1]
(1. Univ. of Tokyo (Japan), 2. Univ. of Tsukuba (Japan))

The stability of MoS2 is critical for device application, while no capable method is reported to trace the atomic scale defects for MoS2 on insulating SiO2/Si substrate. Herein, the defect formation of MoS2 was quantitatively investigated from the viewpoint of sulfur desorption by thermal desorption spectroscopy and also traced through defect selective oxide deposition by ALD. With annealing MoS2 even at ultra-high vacuum, the adsorbed oxygen molecule assists the sulfur atom to dissociate from MoS2 and thus defects are formed, suggesting that removal of adsorbed oxygen is key to avoiding degradation of MoS2

4:30 PM - 4:45 PM

[H-3-02] Experimental Study on Suspended Trapezoid Graphene for Thermal Rectification

○Fayong Liu[1], Jiayu Guo[1], Yoshiki Ozono[1], Shinichi Ogawa[2], Yukinori Morita[2], Manoharan Muruganathan[1], Hiroshi Mizuta[1]
(1. Japan Advanced Institute of Science and Technology (Japan), 2. National Institute of Advanced Industrial Science and Technology (Japan))

We report on successful fabrication of a series of sus-pended trapezoid graphene devices and observation of the thermal rectification phenomenon at low temperatures. The trapezoid graphene channel is patterned by electron beam lithography (EBL) followed by reactive ion etching (RIE). From the experimental results, we find that heat transport is strongly related to the heat injection length from the hot region to the graphene channel.

4:45 PM - 5:00 PM

[H-3-03] Thickness-Dependent Magnetic Domain Structures in CoFe/MgO Nanolayer Patterns on GaAs (001) Substrates

○Li Zi[1], Wei Dai[1], Masashi Akabori[2], Shinjiro Hara[1] (1. Hokkaido Univ. (Japan), 2. Japan Advanced Inst. of Sci. and Tech. (Japan))

We characterize the magnetic domains in CoFe/MgO nanolayer patterns deposited on GaAs (001) substrate for a different nanolayer thickness by magnetic force microscopy without an external magnetic field at room temperature. The results show that thickness of the nanolayer patterns and crystallographic orientation of the substrate are still key factors for controlling magnetic domain structures. In addition, the MgO film also plays an important role in adjusting domain structures.

5:00 PM - 5:15 PM

[H-3-04] Light-emitting layered architectures tunable with chiral light and magnetic field

Haider Golam[1], Vaibhav Varade[2], Shankar Khanal[2], Arthur Slobodeniuk[2], Tomas Novotny[2], Martin Zacek[2], Martin Kalbac[1], ○Jana Kalbacova Vejpravova[2]
(1. J. Heyrovsky Institute of Physical Chemistry, CAS (Czech Republic), 2. Charles University, Faculty of Mathematics and Physics (Czech Republic))

Van der Waals (vdW) materials have revealed a great
potential for constructing ultrathin opto-spintronic and
valleytronic devices. Here we summarize our recent experimental and theoretical results on hybrid layered architectures based on transition metal dichalcogenides,
hexagonal boron nitride, and layered magnets, including
their rational design, fabrication, and performance under
chiral light and magnetic field down to helium temperatures.

5:15 PM - 5:30 PM

[H-3-05 (Late News)] Electronic and Magnetic Properties of $CoSb_3$, Cr-doped $CoSb_3$, and Related Compound Thin Films

○Kazuaki Kobayashi[1], Hirokazu Takaki[2], Masato Shimono[1], Hiroyuki Ishii[2], Nobuhiko Kobayashi[2], Kenji Hirose[3], Takao Mori[1]
(1. Nat. Inst. Mater. Sci. (Japan), 2. Univ. of Tsukuba (Japan), 3. NEC Corp. (Japan))

5:30 PM - 6:00 PM

[H-3-06 (Invited)] Post-growth Tailoring of Nanowires’ Bandgap: Towards Tunable Single Photon Sources and Quantum Rings

○Marta De Luca[1] (1. Sapienza Univ. of Rome (Italy))

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-1] Advanced Technologies for GaN Devices

Tue. Sep 27, 2022 11:30 AM - 12:30 PM 303 (3F)

Session Chair: Shinsuke Harada (AIST), Hiroshi Kawarada (Waseda Univ.)

11:30 AM - 11:45 AM

[J-1-01] Shockley–Read–Hall Lifetime in p-type Distributed-Polarization Doped AlGaN Estimated from Current–Voltage Characteristics of p-n^{+} Diode

○Takeru Kumabe[1], Hirotaka Watanabe[2], Yoshio Honda[2], Hiroshi Amano[2,3,4]
(1. Dept. of Electronics Nagoya Univ. (Japan), 2. IMaSS Nagoya Univ. (Japan), 3. VBL Nagoya Univ. (Japan), 4. ARC Nagoya Univ. (Japan))

11:45 AM - 12:00 PM

[J-1-02] Characterization of Magnesium Channeled Implantation Layers in GaN(0001)

○Atsushi Suyama[1,2], Hitoshi Kawanowa[2], Hideaki Minagawa[2], Junko Maekawa[2], Shinji Nagamachi[2], Masahiko Aoki[2], Akio Ohta[1], Katsunori Makihara[1], Seiichi Miyazaki[1] (1. Nagoya Univ. (Japan), 2. Ion Technology Center Co., Ltd. (Japan))

Effect of channeled implantation of 20keV Mg+ ions to GaN(0001) has been studied systematically in the ion dose range of 1.0 ~ 10 × 1014 cm-2. P-type conduction in the layer implanted with 1.0 × 1014 ions/cm2 and N2-annealed at 1300ºC is confirmed by Hall effect and photoluminescence (PL) measurements although the generation of N vacancies and several types of defects are verified by PL and Scanning-TEM (STEM) observations. Rutherford backscattering spectroscopy (RBS) spectra obtained from the implanted layers after the activation anneal show crystalline quality with χmin values of 3.5 ~ 4.5% except highly-defective surfaces. These results indicate that channeled implantation leads to a promising doping technique for GaN devices.

12:00 PM - 12:15 PM

[J-1-03] Effect of Atomic Layer Etching using Nitrogen Plasma on Hall Accumulation at MIS Interface of GaN Polarization-Junction Substrate

○Takuya Hoshii[1], Shonosuke Kimura[1], Kuniyuki Kakushima[1], Hitoshi Wakabayashi[1], Kazuo Tsutsui[1] (1. Tokyo Tech (Japan))

Atomic layer etching (ALE) is a promising process for fabricating recessed-gate GaN devices with superior MIS interfaces. In this study, nitrogen-plasma ALE was applied for the p-channel GaN MISFETs, and the resulting drive current improvement was verified. This improvement indicates a contribution of hole accumulation at the MIS interface. Also, XPS for the MIS interfaces revealed that ALE using nitrogen plasma could reduce the Ga oxides, which would be attributed to the suppression of nitrogen desorption from GaN surfaces during etching and resulting in superior MIS properties. Therefore, nitrogen-plasma ALE could be a novel technique to improve the performance of p-channel GaN MISFETs.

12:15 PM - 12:30 PM

[J-1-04] Tight-Binding Analysis of the Effect of Strain on the Band Structure of GaN

○Wataru Miyazaki[1], Hajime Tanaka[1], Nobuya Mori[1] (1. Osaka Univ. (Japan))

The effects of strain on the band structure of GaN are investigated by using an empirical tight-binding method. The impacts on its bandgap, carrier effective mass, and group velocity are discussed. The strain suitable for achieving high breakdown voltage is proposed.

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-2] GaN-based High-speed Devices

Tue. Sep 27, 2022 2:00 PM - 3:30 PM 303 (3F)

Session Chair: Taketomo Sato (Hokkaido Univ.), Naotaka Iwata (Toyota Technological Inst.)

2:00 PM - 2:30 PM

[J-2-01 (Invited)] Advanced GaN HEMTs for high-efficiency and high-frequency power amplifiers

○Yusuke Kumazaki[1], Shiro Ozaki[1], Yuichi Minoura[1], Atsushi Yamada[1], Naoya Okamoto[1], Naoki Hara[1], Yasuhiro Nakasha[1], Junji Kotani[1], Masaru Sato[1], Toshihiro Ohki[1] (1. Fujitsu Ltd. (Japan))

2:30 PM - 2:45 PM

[J-2-02] Steep Slope GaN MOS-HEMTs with Ferroelectric Semiconductor Heterostructure

○Jeong Yong Yang[1], Min Jae Yeom[1], Seok Chan Yoon[1], Yeong Je Jeong[1], Chan Ho Lee[1], Sang Hee Kim[1], Seung Yoon Oh[1], GeonWook Yoo[1] (1. Univ. Soongsil (Korea))

We demonstrate a steep subthreshold slope (SS) (12 mV/dec) AlGaN/GaN MOS-HEMT by integrating an α-In2Se3 ferroelectric semiconductor as a gate layer. The ferroelectric polarization and semiconductor characteristics of two-dimensional α-In2Se3 is a promising candidate ferroelectric material for modulating the 2DEG channel. The self-aligned α-In2Se3 etching process optimizes device's performance by concentrating its ferroelectric polarization in vertical directions. Furthermore, the reduction of carrier distribution after the etching process enables an achieving the high on/off ratio in a short channel structure. The device with superior characteristics can be a utilizing for GaN-based fast logic and reconfigurable device applications.

2:45 PM - 3:00 PM

[J-2-03] GaN channel thickness dependence in AlGaN / GaN HEMT structures with back barriers

○Yoshikaze Ito[1], Seita Tamai[1], Takuya Hoshi[2], Yasuyuki Miyamoto[1]
(1. Tokyo Institute of Technology (Japan), 2. NTT Device Technology Laboratories, NTT Corporation (Japan))

AlGaN/GaN HEMTs with 65 nm channel and 38 nm channel with back barrier layers were fabricated. The isolation process caused damage related to the thickness of the channel layer, possibly due to the surface oxidation, resulting in deteriorated characteristics such as sheet resistance and transconductance. Although the suppression of the short-channel effect by the back-barrier layer was confirmed, no significant property change due to the channel layer thickness was observed in the range of fab-ricated gate length.

3:00 PM - 3:15 PM

[J-2-04] Self-terminating Photo-electrochemical (PEC) Etching for Recessed-gate Fabrication on AlGaN/GaN HEMTs

○Takuya Togashi[1], Kosaku Ito[1], Taketomo Sato[1] (1. Hokkaido Univ. (Japan))

The controllability of photo-electrochemical (PEC) etching was investigated for the fabrication of recessed-gate AlGaN/GaN HEMTs. The self-termination depth of the PEC etching was strongly dependent on the light power intensity, showing that the photovoltaic effect of the electrolyte/AlGaN system is the driving force for PEC etching.

3:15 PM - 3:30 PM

[J-2-05] Depletion width in AlGaN/GaN heterostructures under Ohmic-metals

○Kazuya Uryu[1,2], Toshi-kazu Suzuki[1] (1. Japan Advanced Inst. of Sci. and Tech. (Japan), 2. Advantest Lab. Ltd. (Japan))

For AlGaN/GaN heterostructures with Ohmic-metals, we determined the depletion width under the Ohmic-metals, by using multi-probe-Hall measurements in combination with high-frequency characterization of floating contacts.

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-3] High-speed Devices

Tue. Sep 27, 2022 4:15 PM - 5:45 PM 303 (3F)

Session Chair: Akira Satou (Tohoku Univ.), Colombo Bolognesi (ETH Zurich)

4:15 PM - 4:45 PM

[J-3-01 (Invited)] Terahertz InP/GaAsSb Double Heterojunction Bipolar Transistors

○Akshay Mahadev Arabhavi[1], Sara Hamzeloui[1], Filippo Ciabattini[1], Olivier Ostinelli[1], Colombo R Bolognesi[1]
(1. ETH-Zurich (Switzerland))

4:45 PM - 5:00 PM

[J-3-02] Surface-oxide-controlled InGaAs/InAlAs Inverted-type MOS-HEMTs for Sub-THz High-power Amplifiers

○Shiro Ozaki[1], Yusuke Kumazaki[1], Naoya Okamoto[1], Yasuhiro Nakasha[1], Naoki Hara[1], Toshihiro Ohki[1] (1. Fujitsu Limited (Japan))

Herein, we successfully improved the maximum oscillation frequency and maximum stable gain (MSG) across a wide bias range using surface-oxide-controlled (SOC) InGaAs/InAlAs inverted-type metal-oxide-semiconductor HEMTs (inverted MOS-HEMTs) due to a reduction in the gate leakage current and drain conductance. H2O vapor treatment selectively decreased the narrow band gap oxide (InOx) at the surface of the In-based epitaxial layer. Consequently, SOC inverted MOS-HEMTs show a high MSG of over 12 dB across a wide bias range at 100 GHz.

5:00 PM - 5:15 PM

[J-3-03] Single-asymmetric-gated graphene field-effect transistor for terahertz applications

○Chao Tang[1], Koichi Tamura[1], Akira Satou[1], Victor Ryzhii[1], Taiichi Otsuji[1] (1. Tohoku Univ. (Japan))

A novel device structure of the single-asymmetric-gated graphene field-effect transistor (GFET) has been proposed and theoretically investigated using both the equivalent lumped circuit and the distributed waveguide models. In this structure, the ballistic electrons (BE) are injected from the source electrode, traveling through the ungated intrinsic region (i-region), then interact with electrons in the gated n-doped region (n-region) via the Coulomb drag effect, which generates the dragged quasi-equilibrated electrons (DQE), and quasi-equilibrated electrons (QE) reversely injected from the drain electrode when the drain is biased to arise a negative potential slope between the gate and drain. The aforementioned process leads to the current-voltage properties of the negative differential conductivity. One can regulate the frequency, where a negative impedance emerges, by designing the parameter of GFET in the terahertz (THz) range.

5:15 PM - 5:30 PM

[J-3-04] Successful operation of large-area resonant tunneling diodes without heat destruction by introducing a heat-dissipation InP conduction layer

○Hiroki Tanaka[1], Hidenari Fujikata[1], Feifan Han[1], Akira Ishikawa[1], Safumi Suzuki[1], Masahiro Asada[1]
(1. Tokyo Institute of Technology (Japan))

This study proposed a new resonant-tunneling-diode (RTD) structure with improving heat dissipation. In the proposed structure, the low-thermal conductive n+-InGaAs layer, which disturbed heat dissipation to the substrate, was replaced by a high-thermal conductive n+-InP layer. We measured the current-voltage characteristics of various RTD mesa areas, and investigated the number of RTD mesa without heat destruction under the IV measurement. We found that operations without heat destruction were obtained up to twice the larger area or consumed power from the previous structure.

5:30 PM - 5:45 PM

[J-3-05] Superlattice resonant tunneling diode epitaxial structure for THz applications

○Michele Cito[1], Brett A. Harrison[2], Toshikazu Mukai[3], Richard A. Hogg[1]
(1. University of Glasgow (UK), 2. University of Sheffield (UK), 3. RohmCo. Ltd (Japan))

A novel superlattice (SL) design is proposed to improve the crystal quality in AlAs/InGaAs/InP resonant tunnelling diode (RTD) epitaxial structure. The ternary InGaAs well is substituted with binary InAs and GaAs layers in a periodic structure growth by MBE. The SL structure is compared with a standard equivalent ternary structure grown by MBE and one grown by MOVPE. Characterization by photoluminescence (PL) highlighted improvements in crystal uniformity

Session information

Oral Presentation

03: Interconnect / 3D Integrations / MEMS

[K-1] 3D Integration and Advanced Packaging I

Tue. Sep 27, 2022 11:30 AM - 12:30 PM 304 (3F)

Session Chair: Takeyasu Saito (Osaka Metropolitan Univ.), Jenn-Ming Song (National Chung Hsing Univ.)

11:30 AM - 11:45 AM

[K-1-01] Simulation and Experimental Study of Stretchable 3D Corrugated Interconnections for Chiplet-Embedded Flexible Hybrid Electronics Using Wafer-Level Packaging

○CHANG LIU[1], Yuki Susumago[1], Tadaaki Hoshi[1], Hisashi Kino[2], Tetsu Tanaka[1,2], Takafumi Fukushima[1,2]
(1. Graduate School of Eng., Tohoku Univ. (Japan), 2. Graduate School of Biomed. Eng., Tohoku Univ. (Japan))

The bendability and stretchability of inter-chip wires are one of the important issues for FHE (Flexible Hybrid Electronics). Being bent with a small bending radius (R smaller than 1 mm) or in-plane stretched with critical deformation (strain larger than 1%) leads to high stress concentration in the wires, causing electric disconnection and structural failure such as delamination with high possibility. This work deals with vertically corrugated interconnections compatible to advanced FOWLP (fan-out wafer-level packaging)-based FHE we have developed so far. The out-of-plane geometric structure is simulated to reduce mechanical stress and the validity of the optimized 3D design is experimentally evaluated to verify the simulational analyses.

11:45 AM - 12:00 PM

[K-1-02] Warpage and Stress Study of Wafer-to-Wafer Bonding Fabrication Process

○Wei FENG[1], Haruo Shimamoto[1], Tsuyoshi Kawagoe[2], Ichirou Honma[2], Masato Yamasaki[2], Fumitake Okutsu[2], Takatoshi Masuda[2], Katsuya Kikuchi[1] (1. National Inst. of Advanced Indus. Sci. and Tech. (AIST) (Japan), 2. UltraMemory Inc. (Japan))

Wafer warpage causes alignment issues and the degradation of the device’s performance. The increase of metal layers in the stack direction in the development of devices will worsen the warpage problem. We successfully study the warpage issue in Wafer-to-Wafer (W2W) bonding process with experiments and full wafer simulation. After the W2W bonding process, the wafer warpage increases to 3 times the single wafer warpage value. The simulation model is validated by the good agreement with the measured data. The wafer-level stress is revealed in the W2W bonding process. With the validated model, the wafer warpage of the 4-stack wafer bonding is estimated to be 7 times the single wafer warpage value. This study provides useful information on wafer warpage and stress in the W2W bonding process and reveals the severe warpage issue with increasing the stacked metal layers.

12:00 PM - 12:15 PM

[K-1-03] Fabrication of the 3D-stacked retinal prosthesis chip to realize high-performance retinal prosthesis

○Aoba Onishi[1], Ryotaro Bamba[1], Bungo Tanaka[1], Ryouhei Kishimoto[2], Hisashi Kino[1], Takafumi Fukushima[1,2], Tetsu Tanaka[1,2]
(1. Dep. of Biomed. Eng., Graduate School of Biomed. Eng., Tohoku Univ. (Japan), 2. Dep. of Mech. Sys. Eng., Graduate School of Eng., Tohoku Univ. (Japan))

Retinitis pigmentosa and age-related macular degeneration

cause blindness due to the deterioration of photoreceptor cells. The retinal prosthesis has been developed to obtain the vision lost by these diseases. We have been developing a 3D-stacked retinal prosthesis chip to enhance the performance of the retinal prosthesis. This retinal prosthesis has a 3D-stacked structure, improving area efficiency and realizing high resolution, functionality, and sensitivity. This study fabricated a 3D-stacked retinal prosthesis chip and evaluated the electrical characteristics.

12:15 PM - 12:30 PM

[K-1-04] Demonstration of 90,000 Superconductive Bump Connections for Massive Quantum Computing

○Yuuki Araga[1], Hiroshi Nakagawa[1], Masaru Hashino[1], Katsuya Kikuchi[1]
(1. National Inst. of Advanced Indus. Sci. and Tech. (AIST) (Japan))

We developed fabrication and bonding technology of superconductive bump for massive quantum computing. A bonded test vehicle demonstrates supercurrent through 90,000 series daisychain. Proposed bump consists of lead-indium alloy. The bumps land onto gold pad on the opposite chip and alloy with the gold pad for supercurent. The primary advantage of the proposed bump is the minimized damage to the pad chip, which is opposite of the bump. The plasma cleaning process can be omitted for the pad chip and less thermal damage by 100 degrees Celsius of bonding temperature which is lower than typical bonding process.

Session information

Oral Presentation

12: Advanced Circuits / Systems Interacting with Innovative Devices and Materials

[K-2] Advanced Sensor Systems

Tue. Sep 27, 2022 2:00 PM - 3:15 PM 304 (3F)

Session Chair: Koh Johguchi (Shinshu Univ.), Jerald Yoo (National Univ. of Singapore)

2:00 PM - 2:15 PM

[K-2-01] High-Resolution Sensor Interface IC with Switched-Capacitor Frequency Locked Loop Circuit for Battery-less RF Backscatter Sensing

○Hiroki Sato[1], Hiroyuki Ishiwata[2], Shinji Murata[2], Noboru Ishihara[3], Hiroyuki Ito[3]
(1. Nisshinbo Micro Devices Inc. (Japan), 2. ALPS ALPINE Corp., Ltd. (Japan), 3. Tokyo Inst. of Tech. (Japan))

A sensor interface IC that enables battery-less wireless sensing is proposed. The circuit consists of a sensor interface circuit with an instrumentation amplifier and a frequency locked loop FLL for highly sensitive and stable operation, an RF backscatter circuit that enables wireless sensing without power consumption, and an energy harvester circuit that enables battery less operation was integrated by the 0.13-μm CMOS process technology. As a result of inputting a 920MHz RF signal to the IC, we succeeded in realizing wireless sensing by intermittent operation without batteries. The sensor information could be obtained by the frequency variation of the RF backscatter signal, and the sensitivity to the sensor voltage was 12kHz/mV. The IC operated with an RF signal power input of more than -5dBm. The IC dissipate less than 150μA.
The IC is expected to be applied to such as internal body monitoring for medical use and monitoring of blind environments such as in luggage and structures.

2:15 PM - 2:30 PM

[K-2-02] A 22nm CMOS 1.25V 29pW 0.000013 mm^2 Supply Voltage Detector Using Stacked 3 Thick-Gate-Oxide PMOSs and Dynamic Leakage Suppression Buffer

○Yuma Hayashi[1], Kiichi Niitsu[1] (1. Nagoya Univ. (Japan))

This paper presents low-standby-power supply volt-age detector with small footprint in 22nm CMOS for energy-autonomous IoT applications. By using stacked 3 thick-gate-oxide PMOSs and dynamic leakage suppres-sion buffer, standby power can be reduced. Test chip has been designed and developed in 22nm bulk CMOS technology. Measured results showed successful func-tionality with 29 pW power under 1.2 V supply voltage.

2:30 PM - 2:45 PM

[K-2-03] A High-Precision Wearable Perspiration Monitor with 0.18 μm BCD Process and PDMS Micro Air-Flow Path

○Ayumu Yamamoto[1], Yuta Kaga[1], Tomohiro Aso[1], Shin-Ichiro Kuroki[2], Hideya Momose[3], Koh Johguchi[1]
(1. Shinshu Univ. (Japan), 2. Hiroshima Univ. (Japan), 3. Skinos Co.,Ltd. (Japan))

To realize daily perspiration monitoring, this paper presents a compact perspiration monitoring circuit with a micro blower driver by a 0.18 μm BCD process. A micro air-flow path is manufactured with PDMS material. All system is placed on a custom flexible board, and it also produces sustainable high precision perspiration monitoring.

2:45 PM - 3:00 PM

[K-2-04] An Indirect Measuring Method for the Flow-Through Current using Multi-Output MOSFET

○Tomochika Harada[1], Keito Yamaguchi[1], Shinya Suzuki[1], Kota Oikawa[1] (1. Yamagata Univ. (Japan))

In this paper, we propose the indirect measuring method for the flow-through current using multi-output MOSFETs, a MOSFET-type sensor that is expected to reduce the cost, size, and size of sensors. We design and fabricate multi-output CMOS inverter to detect the flow-through current indirectly using 0.18μm CMOS technology. As a result, we realize that it is possible to detect the through-current indirectly by reading the voltage from the output terminal located on both sides of the channel in MOSFET.

3:00 PM - 3:15 PM

[K-2-05 (Late News)] A Z-gate Layout MOSFET Design and Verification of Radiation Hardness against γ-ray Total Ionizing Dose Effect

○Kaito Kuroki[1], Arisa Kimura[1], Kenji Hirakawa[2], Masayuki Iwase[2], Munehiro Ogasawara[2], Takashi Yoda[2], Noboru Ishihara[1,2], Hiroyuki Ito[1,2]
(1. Nano Sensing Unit, Inst. of Innovative Res. , Tokyo Inst. of Tech. (Japan), 2. Lab. for Future Interdisciplinary Res. of Sci. and Tech. , Tokyo Inst. of Tech. (Japan))

2022 International Conference on
Solid State Devices and Materials
ssdm 2022 September 26-29, 2022

Session information

Oral Presentation

Focus Session 3 (Area3&5&12)

[K-3] Design, Process, and Technology for High-performance Chiplet I

Tue. Sep 27, 2022 4:15 PM - 5:45 PM 304 (3F)

Session Chair: Takeyasu Saito (Osaka Metropolitan Univ.), Satoshi Iwamoto (Univ. of Tokyo)

4:15 PM - 4:45 PM

[K-3-01 (Invited)] Wafer Bonding Advances and 3D Applications

○Hiroshi Yamamoto[1] (1. EV Group Japan (Japan))

4:45 PM - 5:15 PM

[K-3-02 (Invited)] Heterogenous Integration on Flexible Substrates

○Lars Zimmermann[1] (1. IHP (Germany))

5:15 PM - 5:45 PM

[K-3-03 (Invited)] Advanced Encapsulants for Compound Semiconductor Package

○Kuo-Chan Chiou[1] (1. Industrial Technology Research Institute (Taiwan))