Session information

Oral Presentation

05: Photonics: Devices / Integration / Related Technology

[A-5] UV Sources and Detectors

Wed. Sep 28, 2022 10:45 AM - 12:15 PM 101 (1F)

Session Chair: Kouichi Akahane (NICT), Hideki Ono (OKI)

10:45 AM - 11:00 AM

[A-5-01] Ultra-Low Voltage Fin-Shaped AlGaN/GaN Ultraviolet Photodetector with Enhanced Frequency Responses

○Yuhan Pu[1], Yung C. Liang[1] (1. National Univ. of Singapore (Singapore))

This paper presents an ultra-low voltage AlGaN/GaN ultraviolet (UV) photodetector with trench-fin-shaped structural design. Owing to the intrinsic polarization field and fin-shaped field plates, the collection of photo-carriers is effective at a bias voltage as low as 200 mV, with the 365-nm photocurrent to dark current ratio above 10^5 and the peak UV responsivity around 10^3 measured. The enhanced frequency response was also observed up to 1 kHz on 365-nm UV switching. The proposed fin-shaped UV photodetector is very suitable for future ultra-low voltage III-V integrated circuits.

11:00 AM - 11:15 AM

[A-5-02] Study on the Optical Characteristics of Light-Emitting HEMT with Different Quantum Well Locations

○Yao-Luen Shen[1], Chih-Yao Chang[1], Po-Liang Chen[1], Cheng-Chan Tai[1], Tian-Li Wu[2], Yuh-Renn Wu[3], Chih-Fang Huang[1]
(1. National Tsing-Hua Univ. (Taiwan), 2. National Yang Ming Chiao Tung Univ. (Taiwan), 3. National Taiwan Univ. (Taiwan))

11:15 AM - 11:30 AM

[A-5-03] Fabrication and optical characterization of GaN microdisk cavites undercut by laser-assisted photo-electrochemical etching

○Sho Sosumi[1], Kenshin Shimoyoshi[1], Kazuo Uchida[1], Takeyoshi Tajiri[1] (1. The University of Electro-Communications (Japan))

GaN micro-disk cavities undercut by laser-assisted
photo-electrochemical (PEC) etching are fabricated and
optically characterized. The PEC etching uses a laser
source which is tuned to be absorbed by the InGaN/GaN
superlattice under the GaN disk for selective etching of
the superlattice. Resonant modes of the fabricated cavities
are confirmed by micro-photoluminescence spectroscopy
of light emission from the embedded quantum wells. Thequality factor reaches about 3900 at blue-violet wavelengths. Such high quality factor at this wavelength range
highlights the applicability of laser-assisted PEC etching
to fabrication of air-clad GaN micro-cavities.

11:30 AM - 11:45 AM

[A-5-04] Effect of Modulation Mg Doped p-Interlayer in 230 nm Far-UVC AlGaN LightEmitting Diodes with Transparent p-Contact Layer

○Noritoshi Maeda[1], Yukio Kashima[1], Eriko Matsuura[1], Yasushi Iwaisako[2], Hideki Hirayama[1]
(1. RIKEN (Japan), 2. Nippon Tungsten (Japan))

11:45 AM - 12:00 PM

[A-5-05] Significant Improvement of Injection Efficiency in Deep-UV LD Structures by Light Mg Doping in p-Core Layer

○Yuri Itokazu[1,2], Noritoshi Maeda[1], Hiroyuki Yaguchi[2], Hideki Hirayama[1] (1. RIKEN (Japan), 2. Saitama Univ. (Japan))

Improvement of injection efficiency is essential to achieve lower threshold and shorter wavelength LDs. We have confirmed that the introduction of electron blocking layer and Mg doping layer into the core layer significantly improves the injection efficiency. In this study, we show that optimizing the Mg doping level in the core layer improves the external quantum efficiency by a factor of about 10 compared to the non-doped sam-ple. This is because the dip in the conduction band due to polarization charge at the core/cladding layer inter-face is suppressed by ionized Mg activated by the Poole-Frenkel effect.

12:00 PM - 12:15 PM

[A-5-06] Improvement of Injection Efficiency by Modulation Doping into p-Side Waveguide Layer in 290 nm Laser Diode Structures

○Noritoshi Maeda[1], Yukio Kashima[1], Eriko Matsuura[1], Yasushi Iwaisako[2], Hideki Hirayama[1]
(1. RIKEN (Japan), 2. Nippon Tungsten (Japan))

Session information

Oral Presentation

05: Photonics: Devices / Integration / Related Technology

[A-6] III-V Light Sources

Wed. Sep 28, 2022 1:30 PM - 3:45 PM 101 (1F)

Session Chair: Yuhki Itoh (Sumitomo Electric Industries, Ltd.), Nobuhiko Ozaki (Wakayama Univ.)

1:30 PM - 1:45 PM

[A-6-01] 1060nm Single-mode Bottom Emitting VCSEL Array with Intra-cavity Metal-aperture for Multi-core Fiber Co-packaged Optics Transceivers

○Liang Dong[1], Xiaodong Gu[2,1], Fumio Koyama[1] (1. Tokyo Inst. of Tech. (Japan), 2. Ambition Photonics Inc. (Japan))

We demonstrate 1060nm 16 channels bottom emitting VCSEL arrays with intra-cavity metal-aperture. The metal-aperture enables the single mode operation with large oxidation apertures and the bandwidth enhancement. Thanks to the transverse response, the 3dB small signal response reaches over 20 GHz.

1:45 PM - 2:00 PM

[A-6-02] All III-arsenide 1.6 µm-band InAs quantum dot lasers on InP(001) with a low threshold current density

○Jinkwan Kwoen[1], Natalia Morais[1], Wenbo Zhan[1], Satoshi Iwamoto[1,2], Yasuhiko Arakawa[1]
(1. NanoQuine, Univ. of Tokyo (Japan), 2. RCAST, Univ. of Tokyo (Japan))

We have grown an L-band quantum dot (QD) laser with only III-arsenide layers on InP(001) by molecular beam epitaxy. The threshold current density of the fab-ricated QD laser was 633 A/cm2, which is the lowest value for QD lasers in the 1.6 µm-wavelength region.

2:00 PM - 2:15 PM

[A-6-03] 25-Gb/s Uncooled direct-modulation Using 1270-nm InGaAlAs-Based MQWs DFB Laser

○Hsiang-Chun Yen[1], Te-Hua Liu[1], Chee-Keong Yee[1], Yun-Cheng Yang[1], Hao-Tien Cheng[1], Guei-Ting Hsu[1], Tien-Tsorng Shih[2], Chao-Hsin Wu[1] (1. Univ. of Taiwan (Taiwan), 2. Univ. Sci. Tech. Kaohsiung (Taiwan))

In this paper, We reported an uncooled operation of a directly-modulated 1270 nm, InGaAlAs multiple quantum wells (MQWs) DFB laser with a high modulation bandwidth at 45 °C (above 20 GHz). The presented device possesses a non-return-to-zero transmission speed of 25 Gb/s with an eye-opening feature at room temperature (25 °C).

2:15 PM - 2:30 PM

[A-6-04] Single-Mode High-Speed 850 nm VCSEL Operated at 50 Gb/s for Pre-emphasis NRZ-OOK after 100-m GI-SMF transmission

○Kuo-Hsiung Chu[1], Yen-Wei Yeh[1], Chia-Wei Sun[1], Hao-Chung Kuo[1] (1. National Yang Ming Chiao Tung Univ. (Taiwan))

In this study, a single mode and high speed verti-cal-cavity surface-emitting laser (VCSEL) is designed and fabricated. The device exhibits 26.5 GHz 3-dB E-O bandwidth and 50 Gb/s for pre-emphasis NRZ-OOK transmission in back-to-back and 100m GI-SMF links with eye-opening, which is extremely fast for single mode 850nm VCSELs.

2:30 PM - 2:45 PM

[A-6-05] Room-temperature operation characteristics of a spin-polarized light-emitting diode using InAs quantum dots tunnel-coupled with GaNAs

○Kohei Etou[1], Satoshi Hiura[1], Junichi Takayama[1], Agus Subagyo[1], Kazuhisa Sueoka[1], Akihiro Murayama[1]
(1. Faculty of Information Science and Technology, Hokkaido University (Japan))

We have developed a spin-polarized light-emitting diode (spin LED) using InAs quantum dots (QDs) tunnel-coupled with a GaNAs quantum well, which can amplify the electron spin polarization in QDs at room temperature due to the thermally activated spin filtering in GaNAs. Since conduction band electrons are easily trapped in deep-level defects in GaNAs during LED operation, the introduction of GaNAs can significantly increase the injection current required to obtain a sufficient QD electroluminescence (EL). We also observe the high degree of EL circular polarization ranging from 5 to 6 % under high bias conditions above 4 V. This high spin polarization is due to the selective transfer of minority spins from QDs to GaNAs spin filter via electron wavefunction coupling.

2:45 PM - 3:00 PM

[A-6-06] Optical-to-MMW/THz Carrier Frequency Down-Conversion by UTC-PD-Integrated HEMT: the Scaling Rule of Conversion Gain on UTC-PD Mesa Size

○Dai Nakajima[1], Kazuki Nishimura[1], Tomotaka Hosotani[1], Keisuke Kasai[1], Masato Yoshida[1], Tetsuya Suemitsu[2], Taichi Otsuji[1], Akira Satou[1]

(1. Research Institute of Electrical Communication, Tohoku University (Japan), 2. New Industry Creation Hatchery Center, Tohoku University (Japan))

We experimentally investigate the scaling rule of the conversion gain on unitraveling-carrier-photodiode (UTC-PD) mesa size of the UTC-PD-integrated HEMT for optical to millimeter-wave (MMW)/terahertz (THz) frequency down-conversion. We showed that the conversion gain monotonically increases as the mesa size is reduced, due to the suppression of the in-plane diffusion of photogenerated electrons in the absorption layer.

3:00 PM - 3:15 PM

[A-6-07] Consideration of the interface diffusions for narrow-period terahertz quantum cascade lasers

○Li WANG[1], Tsung-Tse Lin[1], Thomas Grange[2], Ke Wang[3], Hideki Hirayama[1]

(1. RIKEN (Japan), 2. nextnano (Germany), 3. nanjing Univ. (China))

The effects of diffused interface scattering on the transport and the optical gain is still not well shown. In this work, we have determined the interface profiles of GaAs/Al0.3Ga0.7As quantum structures using transmis-sion electron microscopy (TEM). The diffused width is extracted following sigmdial-type functions and then used as basic parameters to estimate the scattering of such a diffused interface based on NEGF method. The optical gain of the 3-level terahertz quantum cascade lasers at 300K is 32% down when such a diffused interface is con-sidered. However, the corresponding scattering is not the reason as its strength is quite small that plays a minor role on the lifetime of states, instead, the shifting of wave-function is original for this change of gain by leading to an obvious misalignment of resonant tunneling for injec-tion.

3:15 PM - 3:30 PM

[A-6-08] Development of Epitaxial Regrowth for GaAs-Based Quantum Dot PCSELs

○Adam F McKenzie[1], Aye M. Kyaw[1], Ben C. King[1], Neil D. Gerrard[1], Kenichi Nishi[2], Keizo Takemasa[2], Mitsuru Sugawara[2], Calum H. Hill[3], David T. D. Childs[3], Richard J. E. Taylor[3], Donald A. MacLaren[1], Richard A. Hogg[1]

(1. Univ. of Glasgow (UK), 2. QD Laser Inc. (Japan), 3. Vector Photonics Ltd. (UK))

We present the development of epitaxial regrowth processes to allow the realization of a PCSEL utilizing a quantum dot active region. An electron microscope-based study investigates the effect of group-III surface mobility on grating infill. An optimal process utilizing AlGaAs in-fill is used to fabricate QD devices that display room temperature ground state lasing at 1230 nm.

3:30 PM - 3:45 PM

[A-6-09] Late News

Session information

Oral Presentation

11: Advanced Materials: Synthesis / Crystal Growth / Characterization

[B-5] Advanced materials, Nanofabrication, and Thin Films I

Wed. Sep 28, 2022 10:45 AM - 12:00 PM 102 (1F)

Session Chair: Hirokazu Tatsuoka (Shizuoka Univ.), Yoriko Tominaga (Hiroshima Univ.)

10:45 AM - 11:00 AM

[B-5-01] Fabrication and optical characterization of InGaN/GaN MQW fine nanopillar arrays by low-damage HEATE process

○Takeki Aikawa[1], Akihiko Kikuchi[1,2,3]
(1. Sophia Univ. (Japan), 2. Sophia Photonics Research Center (Japan), 3. Sophia Semiconductor Research Institute (Japan))

Position-controlled high-aspect ultrafine InGaN/GaN nanopillar arrays ranging from 9 to 1000 nm in diameter and 300 nm in height have been fabri-cated via hydrogen environment anisotropic thermal etching (HEATE) method, which utilizes a SiO2 etching mask and hydrogen-assisted thermal decomposition of GaN. The blue photoluminescence emission was ob-tained at room temperature even from 9 nm diameter ultrafine nanopillars, and the optical properties of InGaN quantum wells were systematically character-ized over a wide range of two orders of magnitude.

11:00 AM - 11:15 AM

[B-5-02] Heteroepitaxial Chemical Bath Deposition of Ultra-High Density ZnO Nanorod Arrays on Au thin-films: Impacts of Au thin-film crystallinity and Periodic Template

○Sho Mekata[1], Yuki Murata[1], Kentaro Watanabe[2] (1. Shinshu Univ. (Japan), 2. IFES, ICCER, Shinshu Univ. (Japan))

11:15 AM - 11:30 AM

[B-5-03] Impact of Oxygen Annealing Temperature on Electrical Conductivity of Individual Free-standing ZnO Nanowires Studied by In-situ “differential” I-V Method

○Kota Miyajima[1], Yuki Murata[1], Kentaro Watanabe[2] (1. Shinshu Univ. (Japan), 2. IFES, ICCER, Shinshu Univ. (Japan))

11:30 AM - 11:45 AM

[B-5-04] Development of fabrication technique of a novel optical-guiding crystal scintillator plate for radiation imaging applications

○Ryuga Yajima[1,2], Kei Kamada[2,3,4], Naoko Kutsuzawa[4], Rikito Murakami[2,4], Masao Yoshino[3], Takahiko Horiai[3], Rei Sasaki[1,2], Kyoung Jin Kim[3], Akihiro Yamaji[3], Shunsuke Kurosawa[2,3,5], Yuui Yokota[2,3], Hiroki Sato[3], Satoshi Toyoda[3], Yuji Ohashi[3], Takashi Hanada[2], Vladimir V Kochurikhin[4], Seichi Yamamoto[6], Akira Yoshikawa[2,3,4]
(1. Department of Materials Sci., Graduate School of Eng., Tohoku Univ. (Japan), 2. IMR, Tohoku Uni. (Japan), 3. NICHe, Tohoku Uni. (Japan), 4. C&A corp. (Japan), 5. Inst. of Laser Eng., Osaka Univ. (Japan), 6. Waseda Univ. (Japan))

A novel optical-guiding crystal scintillator (OCS) plate was developed for radiation imaging applications. OCS plates consist of a large number of tens of microns diameter scintillator crystal fibers as a core, which are filled into a glass cladding. Due to the refractive index difference between the glass cladding and the scintillator crystal core, the OCS plate has light guiding performance similar to an optical fiber. The optical-guiding function provides high resolution and sensitivity in radiation imaging, enabling sharper images and shorter imaging times. The advantage is that industrially mass-producible manufacturing processes can be applied, and the size and structure can be easily controlled compared to previously reported optical waveguide eutectics.

11:45 AM - 12:00 PM

[B-5-05] Formation of High-Mobility InSb Films on Glass by Sputtering and Rapid-Thermal Annealing

Takashi KAJIWARA[1], Otokichi SHIMODA[2], Tatsuya OKADA[2], Charith Jayanada KOSWATHTHAGE[2], Takashi NOGUCHI[2], ○Taizoh SADOH[1]
(1. Kyushu Univ. (Japan), 2. Univ. of the Ryukyus (Japan))

Session information

Oral Presentation

11: Advanced Materials: Synthesis / Crystal Growth / Characterization

[B-6] Advanced materials, Nanofabrication, and Thin Films II

Wed. Sep 28, 2022 1:30 PM - 3:15 PM 102 (1F)

Session Chair: Yu-Lun Chueh (National Tsing-Hua Univ.), Akihiko Kikuchi (Sophia Univ.)

1:30 PM - 1:45 PM

[B-6-01] Correlation between Dipole Layer Formation and Surface Terminating Crystal Face in Perovskite Oxide Epitaxial Stacks Clarified by Lateral Force Microscopy

○Atsushi Tamura[1], Koji Kita[1,2]
(1. Dept. of Materials Engineering, Univ. of Tokyo (Japan), 2. Dept. of Advanced Materials Science, Univ. of Tokyo (Japan))

Dipole layer formation in perovskite epitaxial stacks is considered to be affected by the stacking sequence of monatomic layers of polar oxide (LaAlO3 (LAO)). It was found that the magnitude of dipoles in LAO/SRO(SrRuO3) stacks were significantly different only by inserting a few monolayers of SrAlOx (SAO) between LAO and SRO. The statistical analysis of lateral force microscopy (LFM) images on LAO clarified a difference in dominant sur-face terminating crystal faces. These results support the correlation between the interfacial dipole layer for-mation and the stacking sequence of monatomic layers of LAO.

1:45 PM - 2:00 PM

[B-6-02] Surface Morphology Analysis of $BiFeO_3$ Film on $DyScO_3$ Substrate by RF Sputtering

○Fuminobu Imaizumi[1], Kazuki Hisada, Rikuto Nakada (1. National Institute of Technology(KOSEN), Oyama College (Japan))

We investigated the formation of BiFeO3 films as a lead-free ferroelectric material on DyScO3 substrate. Experiments were performed to analyze the film formation process via the sputtering method, followed by post-annealing process. Consequently, a BiFeO3 film was formed with a single (001) orientation, and two types of bonds (FeO and Fe2O3) were observed.

2:00 PM - 2:15 PM

[B-6-03] Atomic-scale observation of biased monolayer MoSSe devices *via in situ* transmission electron microscopy

○Hsin-Ya Sung[1], Yi-Tang Tseng[1], Wen-Wei Wu[1] (1. National Yang Ming Chiao Tung University (Taiwan))

2:15 PM - 2:30 PM

[B-6-04] Synthesis of Ge-based Nanosheet Bundles from $CaSi_2$ Crystal Powders by Thermal Annealing with $MgCl_2$/Mg

○Kaito Sekino[1], Yosuke Shimura[1,2,3], Hirokazu Tatsuoka[1] (1. Shizuoka Univ. (Japan), 2. RIE Shizuoka Univ. (Japan), 3. imec (Belgium))

Ge-based nanosheet bundles were synthesized by vapor phase technique from CaGe2 crystal powders.
MgCl2/Mg sources were used as the extraction agent of Ca from CaGe2. It was also observed that GeH phases were formed. In addition, stabilities of the GeH phases and the nanosheet structures were examined, then fine structural properties of the resulted bundles were also characterized.

2:30 PM - 2:45 PM

[B-6-05] Effect of Underlayer on Reduction of Graphene Oxide by Atomic Hydrogen Annealing

○Akira Heya[1], Akinori Fujibuchi[1], Masahiro Hirata[1], Koji Sumitomo[1] (1. Univ. of Hyogo (Japan))

Effect of underlayer on reduction of graphene oxide (GO) by atomic hydrogen annealing (AHA) was investi-gated using microwell substrate with holes of um order. In AHA, atomic hydrogen is generated on a heated tungsten mesh through a catalytic cracking reaction of H2 gas. The X-ray photoelectron spectra showed that the GO film was reduced by AHA at 170 °C. The Ni underlayer affected the reduction of GO films. The intensity ratio of the D and G bands indicates that reduction is less likely to occur with suspended GO than with supported GO.

2:45 PM - 3:00 PM

[B-6-06] Formation of Ultra-thin NiGe film with Mono-crystalline Phase and Smooth Surface

○Shunsuke Nishimura[1], Noriyuki Taoka[1], Akio Ohta[1], Katsunori Makihara[1], Seiichi Miyazaki[1] (1. Univ. of Nagoya (Japan))

Ni and Ge films with various thicknesses are formed on a SiO2 layer. Ni-germanides were formed by annealing in an N2 ambient condition. Consequently, an ultra-thin Ni-germanide film with a mono-crystalline phase and a smooth surface was successfully formed. In the formation, reductive and oxidative reactions occurred in the films, which are quite important for determining a composition of the Ni-germanide.

3:00 PM - 3:15 PM

[B-6-07] Refractory NbMoTaW High Entropy Alloy film as Diffusion Barrier for Copper/Silicon Interconnections

Chuan Feng Shih[1], ○Cheng Hsien Yeh[1], Hsuan Ta Wu[2], Teng Yi Huang[1]
(1. National Cheng Kung Univ. (Taiwan), 2. Minghsin Univ. of Sci. and Tech. (Taiwan))

The NbMoTaW high entropy alloy (HEAs) films with equal proportion and excellent single-phase solid solution were fabricated by DC magnetron sputtering. A 70 nm-thick NbMoTaW film shows excellent thermal stability and maintains good electrical properties about 75 μΩ-cm after 500°C annealing. A 15 nm-thick NbMoTaW film was prepared as a diffusion barrier. It was found that the structure is complete, and no diffusion occurs after 500°C annealing. Moreover, Cu/HEAs/Si interface become obscure slightly after 700°C annealing that is superior to the Cu/Ti/Si interface, which become rough at 500°C. It indicates that the critical point of failure of the HEA diffusion barrier was improved. The results also suggest a high opportunity of NbMoTaW film to replace the conventional Ti, Ta and other binary alloys/nitrides with the advantages of low resistivity and thermal stability, being a potential candidate in Cu/Si interconnects as a diffusion barrier.

Session information

Oral Presentation

06: Photovoltaic / Energy Harvesting / Battery-related Technology

[C-4] Battery, Photocatalyst, Photodetector

Wed. Sep 28, 2022 9:00 AM - 10:15 AM 103 (1F)

Session Chair: Masaki Matsui (Hokkaido Univ.), Munekazu Motoyama (Nagoya Univ.)

9:00 AM - 9:30 AM

[C-4-01] Toward Low Cost and High Energy Beyond Li-Ion Batteries for Large-Scales

○Haegyeom Kim[1] (1. Lawrence Berkeley National Lab. (United States of America))

9:30 AM - 9:45 AM

[C-4-02] Cathode Supported Solid-State Polymer Electrolyte Enriched with Lewis Acid Sites

○Rohan Paste[1,2], Hong-Cheu Lin[1], Chih Wei Chu[2]
(1. Department of Materials Science and Eng., National Yang Ming Chiao Tung University (Taiwan), 2. Research Center for Applied Sciences, Academia Sinica, Taipei (Taiwan))

9:45 AM - 10:00 AM

[C-4-03] Accurate estimation of surface recombination velocities for $SrTiO_3$ using angle-lapped structures

○Masashi Kato[1], Yosuke Kato[1] (1. Nagoya Institute of Technology (Japan))

Surface recombination velocity is an important factor for carrier recombination which dominates energy conversion efficiency in photocatalysts. We employed angle-lapped structure of SrTiO3 to estimate surface recombination velocities. We analyzed thickness dependence of the carrier lifetime by numerical modelling. Then we obtained more accurate values for the surface recombination velocities compared with the previous study.

10:00 AM - 10:15 AM

[C-4-04] Investigation of Organic Solar Cells as Photodetectors

○Jiaxun You[1], Md. Shahiduzzaman[1], Masahiro Nakano[1], Makoto Karakawa[1], Kohichi Iiyama[1], Tetsuya Taima[1]
(1. Kanazawa Univ. (Japan))

In this work, we investigate the effect of organic photovoltaic (OPV) structures such as Schottky, planar heterojunction (PHJ) and bulk heterojunction (BHJ) as the organic photodetectors (OPD) and how it contributes to the improvement of the resultant device performance. Interestingly, the Schottky device as OPV exhibited the lowest power conversion efficiency (PCE) of 3×10-4%, subsequently almost unfeasible, whereas Schottky device as the OPD showed the higher linear dynamic range (LDR) of 53 dB, which is superior to those of PHJ and BHJ devices as the OPD (39 dB and 13 dB). OPV with BHJ structure showed higher PCE than Schottky whereas BHJ devices revealed lower LDR than Schottky devices used as OPD because of the poor rectification that get a higher dark current.

Session information

Oral Presentation

Focus Session 1 (Area1&2&9)

[C-5] Quantum Computing 3

Wed. Sep 28, 2022 10:45 AM - 12:00 PM 103 (1F)

Session Chair: Yuichiro Matsuzaki (AIST), Takashi Tsuchiya (NIMS)

10:45 AM - 11:15 AM

[C-5-01] Developments of Silicon Spin Qubits beyond High-Fidelity Gate Operations

○Jun Yoneda[1] (1. Tokyo Tech (Japan))

11:15 AM - 11:30 AM

[C-5-02] High-speed and low-variability operation of one-dimensional silicon-spin-qubit array employing buried nanomagnets

○Shota Iizuka[1], Kimihiko Kato[1], Atsushi Yagishita[1], Hidehiro Asai[1], Tetsuya Ueda[1], Hiroshi Oka[1], Junichi Hattori[1], Tsutomu Ikegami[1], Koichi Fukuda[1], Takahiro Mori[1] (1. AIST (Japan))

We investigated X-gate operation speed and variation tolerance in one-dimensionally integrated Si spin qubits employing the buried nanomagnet (BNM) technology. Our numerical simulations reveal that about 30 times faster X-gate operation is achievable thanks to a large slanting magnetic field generated by the BNM placed close to the spin qubits. Also, the proposed self-aligned fabrication process of the BNM can suppress fidelity variation caused by the fabrication process variation, supposing that the single wavelength microwaves control all qubits.

11:30 AM - 11:45 AM

[C-5-03] SPICE compact model of spin qubits using FinFET focusing on single-electron tunneling

○Elias Perez[1], Teresa T Orvañanos-Guerrero[2], Tetsufumi Tanamoto[1]
(1. Teikyo Univ. (Japan), 2. Universidad Panamericana (Mexico))

We proposed a Simulation Program with Integrated Circuit Emphasis (SPICE) compact model for the con-trol circuit of the spin qubit based on a fin field-effect transistor (FinFET). A SPICE model is constructed to simulate the single-electron process which describes the setup of a qubit using FinFETs. We investigated the pa-rameter dependence of Coulomb oscillations.

11:45 AM - 12:00 PM

[C-5-04] Mixed-mode RF reflectometry for reduction of crosstalk effects

○Masato Machida[1], Raisei Mizokuchi, Jun Yoneda, Takashi Tomura, Tetsuo Kodera (1. Tokyo Inst of Tech (Japan))

RF reflectometry is a promising technique for spin qubit readout, suitable for large-scale integrated qubit systems by combination with multiplexing techniques and gate-based readout. However, in such a system, it is suspected that the accuracy of RF readout of individual qubits can be degraded by crosstalk among dense RF readout lines. In this study, we propose a mixed-mode RF reflectometry to reduce the effect of the crosstalk and verify its effectiveness by electromagnetic field simulations. The results of the simulations show the possibility of sup-pressing the effects of crosstalk by using mixed modes.

Session information

Oral Presentation

Focus Session 1 (Area1&2&9)

[C-6] Quantum Computing 4

Wed. Sep 28, 2022 1:30 PM - 3:30 PM 103 (1F)

Session Chair: Kae Nemoto (NII), Takashi Tsuchiya (NIMS)

1:30 PM - 2:00 PM

[C-6-01] Recent Progress in Quantum Annealing Machine Using Kerr-Parametric Oscillators

○Aiko Yamaguchi[1,2] (1. NEC Corp. (Japan), 2. AIST (Japan))

2:00 PM - 2:15 PM

[C-6-02] Spectroscopic estimation of the photon number for superconducting Kerr parametric oscillators

○Keisuke Matsumoto[1], Aiko Yamaguchi[1,2], Tsuyoshi Yamamoto[1,2], Shiro Kawabata[1], Yuichiro Matsuzaki[1]
(1. AIST (Japan), 2. NEC (Japan))

Quantum annealing (QA) is a way to solve combina-tional optimization problems. Kerr nonlinear parametric oscillators (KPOs) are promising devises to implement QA. To solve the combinational optimization problems with QA using the KPOs, it is necessary to know the pho-ton number of the KPOs. Here, we propose a feasible scheme to estimate the number of photons of the KPO. We consider to couple an ancillary qubit to the KPO, and show that spectroscopic measurements on the qubit pro-vide the information of the photon number of the KPO.

2:15 PM - 2:30 PM

[C-6-03] Uniformity Improvement of Josephson Junction Resistance by Considering Al Deposition on a Resist Sidewall for Large-scale Integration of Qubits

○Tsuyoshi Takahashi[1,2], Norinao Kouma[1,2], Yoshiyasu Doi[1,2], Shintaro Sato[1,2], Shuhei Tamate[2], Yasunobu Nakamura[2,3]
(1. Fujitsu Limited (Japan), 2. RIKEN (Japan), 3. Univ. of Tokyo (Japan))

We report an improvement in the uniformity of Josephson junctions (JJs) in wafer-scale superconducting quantum bit (qubit) chips. We revealed that junction-resistance (RN) variations in Al/AlOx/Al JJs are due to unintentional Al deposition on the resist mask sidewall during shadow mask evaporation. We developed a new two-step shadow evaporation method and success-fully reduced variations in the RN of JJs in a 3-inch wafer from 6.7% to 4.5%, corresponding to 1.1% in a 16-qubit chip with dimensions of 10 mm × 10 mm. This method is promising for developing large-scale super-conducting quantum computers.

2:30 PM - 2:45 PM

[C-6-04] Reducing Microwave Dielectric Losses of Niobium Superconducting Resonators by a Tantalum Cap Layer

○Yoshiro Urade[1], Kunihiro Inomata[1], Kay Yakushiji[1], Manabu Tsujimoto[1], Takahiro Yamada[1], Wataru Mizubayashi[1]
(1. AIST (Japan))

Niobium (Nb), a common material for electrodes of state-of-the-art superconducting qubits, experiences large microwave dielectric losses due to its surface oxide. Mitigating such losses of superconducting materials is crucial for improving the quality of superconducting qubits. To this end, we propose adding a tantalum cap layer on a Nb film. Superconducting resonators based on the composite film have been characterized using microwaves, and a significant increase in the internal quality factor of the resonators has been confirmed. The proposed composite film is expected to improve the coherence time of superconducting qubits.

2:45 PM - 3:00 PM

[C-6-05] Analysis of the shortest vector problems with the quantum annealing to search the excited states

○Katsuki Ura[1,2], Takashi Imoto[1], Tetsuro Nikuni[2], Shiro Kawabata[1], Yuichiro Matsuzaki[1]
(1. AIST (Japan), 2. Tokyo Univercity of Science (Japan))

3:00 PM - 3:15 PM

[C-6-06] Rapid Control of ^{15}N Nuclear Spin within Diamond NV Centers

○Yusuke Azuma[1], Hideyuki Watanabe[2], Satoshi Kashiwaya[3], Shintaro Nomura[1]
(1. Univ. of Tsukuba (Japan), 2. AIST (Japan), 3. Nagoya Univ. (Japan))

We propose a method for fast initialization and quantum control of a 15N nuclear spin in diamond nitrogen-vacancy (NV) centers using non-selective microwave pulses. We demonstrate that the nuclear spin states can be initialized in 130 ns, which is an order of magnitude faster than the conventional methods. Our result may contribute to the development of quantum devices using electron and nuclear spins in NV centers.

3:15 PM - 3:30 PM

[C-6-07] Broadband microwave surface loop-gap resonator for quantum sensors using nitrogen-vacancy centers in diamond

○Toyofumi Ishikawa[1], Yasunori Mawatari[1], Satoshi Kashiwaya[1,2], Akio Yoshizawa[1], Hideyuki Watanabe[1]
(1. National Institute of Advanced Industrial Science and Technology (AIST) (Japan), 2. Nagoya Univ. (Japan))

Quantum sensors based on nitrogen-vacancy (NV) centers in diamond are expected to be a powerful probe for detecting magnetism and nuclear spins at the nanometer scale. Various applications with NV quantum sensors require a uniform microwave (MW) magnetic field. Here, we report on a surface loop-gap resonator that generates a uniform MW field within an area of 7 mm2. Its bandwidth is more than 100 MHz; thus, multiple resonances of spin states can be addressed. The bandwidth can be modified by adjusting the capacitance between the resonator and a microstrip line.

Session information

Oral Presentation

07: Organic / Molecular / Bio-electronics

[D-5] Transistor technologies for biological and electrochemical applications

Wed. Sep 28, 2022 10:45 AM - 12:15 PM 104 (1F)

Session Chair: Toshinori Matsushima (Kyushu Univ.), Hisashi Kino (Tohoku Univ.)

10:45 AM - 11:15 AM

[D-5-01 (Invited)] Synthesis and Characterization of new TADF (macro)molecular materials based on through-space donor-acceptor interactions

○Fabrice Mathevet[1] (1. IPCM, CNRS, Sorbonne Universite (France))

11:15 AM - 11:30 AM

[D-5-02] Signature of carrier delocalization in electrochemically doped conducting polymer DPPT-TT with electrolyte-gated transistor

○Hisaaki Tanaka[1], Ryotaro Yamatoko[1], Shun-ichiro Ito[1], Taishi Takenobu[1] (1. Nagoya Univ. (Japan))

Carrier delocalization in conducting polymers upon carrier doping has been a long-pursued issue both in terms of scientific and technological points of view. In this work, we demonstrate that a typical donor-acceptor (D-A)-type conjugated copolymer exhibits a signature of carrier delocalization within the crystalline domains up-on carrier doping. We adopt the electrolyte gating meth-od to continuously control the doping level, combined with the microscopic observation of injected charge car-riers by operando electron spin resonance (ESR) spec-troscopy. The ESR signal exhibits a clear line broadening in highly doped state characteristic of the scattering of conduction electrons by phonons (Elliott mechanism). Indeed, temperature dependence of the linewidth exhibits strong broadening at hither temperatures, consistent with the Elliott mechanism. The conduction electrons arise from the edge-on oriented crystalline domains as sug-gested from the observed anisotropy of the g values.

11:30 AM - 11:45 AM

[D-5-03] Macroscopically Aligned P(NDI2OD-T2) Floating Films for *n*-Channel Organic Field Effect Transistor

○Manish Pandey[1], Yuya Sugita[1], Jumpei Toyoda[1], Yongyoon Cho[1], Hiroaki Benten[1], Masakazu Nakamura[1]
(1. Nara Institute of Science and Technology (Japan))

11:45 AM - 12:00 PM

[D-5-04] Aging-Robust Amplifier Design Using Low Voltage Organic Semiconductor Loads

○Yuto Kaneiwa[1], Kazunori Kuribara[2], Takashi Sato[1]
(1. Kyoto Univ. (Japan), 2. National Inst. of Advanced Industrial Sci. and Tech. (Japan))

We propose a novel amplifier design for organic thin-film transistor (OTFT), which is robust against temporal characteristics degradation.
The proposed circuit consists of two pairs of OTFT-based resistor and p-type OTFT, each for bias generation and amplification stages. By using the same configurations for the two stages, the proposed circuit compensates the characteristic degradation of the OTFTs, maintaining the proper bias voltage condition for a long period of time.
Experimental results show that the proposed amplifier achieved a 20 dB gain and a cutoff frequency of 40 Hz at a drive voltage of 2.5 V.
In addition, the proposed circuit operates successfully without significant bias drift nor gain degradation after a total of 90 minutes of continuous operation and after one month of environmental degradation.

12:00 PM - 12:15 PM

[D-5-05 (Late News)] Crossbar Array Structured Milk-Ta_2O_5 Hybrid Memristors for Neuromorphic Electronics based on Natural-organic Materials

○Jin-Gi Min[1], Won-Ju Cho[1] (1. Univ. of Kwangwoon (Korea))

Session information

Oral Presentation

07: Organic / Molecular / Bio-electronics

[D-6] Functional devices and application

Wed. Sep 28, 2022 1:30 PM - 3:30 PM 104 (1F)

Session Chair: Masakazu Nakamura (NAIST), Kuniharu Takei (Osaka Metropolitan Univ.)

1:30 PM - 2:00 PM

[D-6-01 (Invited)] Recent Progress of On-Skin Electronics and Smart Textiles

○Takao Someya[1], Tomoyuki Yokota[1], Kenjiro Fukuda[2], Sunghoon Lee[1] (1. Univ. of Tokyo (Japan), 2. Riken (Japan))

2:00 PM - 2:15 PM

[D-6-02] Development of Small-Area Pixel Circuit with Light-to-Pulse Width Converter for the High-Resolution Smart Skin Display

○Yuta - Aruga[1], Bang - Du[1], Yaogan - Liang[1], Kouhei - Nakamura[1], Shengwei - Wang[1], Bunta - Inoue[1], Hisashi - Kino[2], Takafumi - Fukushima[1], Koji - Kiyoyama[3], Tetsu - Tanaka[1,2]
(1. Dept. of Mechanical Systems Eng., Graduate School of Eng., Tohoku Univ. (Japan), 2. Dept. of Biomedical Eng., Graduate School of Biomedical Eng., Tohoku Univ. (Japan), 3. Dept. of Electrical and Electronics Eng., Nagasaki Inst. of Applied Science (Japan))

Photoplethysmography (PPG), a main optical-electrical noninvasive biosignal, is utilized in several wearable devices to achieve daily healthcare and early disease diagnosis. We have proposed a smart skin display with the PPG recording circuit and integrated display LEDs showing subcutaneous vessels for the early diagnosis of vascular disease. A 12 x 12 pixels light-to-pulse width converter circuit, including PPG reading circuits, was developed and evaluated to control the light intensity of display LEDs. The proto-type circuit was designed and fabricated using standard 0.18-μm CMOS technology and was evaluated.

2:15 PM - 2:30 PM

[D-6-03] A novel gas-permeable nanomesh humidity sensor with high sensitivity

○Wenqing Wang[1], Md Osman Goni Nayeem[1], Haoyang Wang[1], Chunya Wang[1], JaeJoon Kim[1], Sunghoon Lee[1], Tomoyuki Yokota[1], Takao Someya[1] (1. University of Tokyo (Japan))

In this paper, we report a humidity sensor made by nanomesh electrodes and nanomesh sensitive materials. The porous structure makes the sensor gas-permeable and increases the surface area, leading to high sensitivity. The gas-permeability suppresses the skin inflammation and allows natural evaporation of sweat, making a same condition as bare skin. The mechanical durability of the sensor makes it suitable for on-skin monitoring.

2:30 PM - 2:45 PM

[D-6-04] A Wireless CMOS Imaging Device for Mouse Under Freely Moving Conditions

○Thanaree Treepetchkul[1], Ronnakorn Siwadamrongpong[1], Hironari Takehara[1], Makito Haruta[1], Hiroyuki Tashiro[1,2], Kiyotaka Sasagawa[1], Jun Ohta[1] (1. Nara Inst. Sci. Tech. (Japan), 2. Kyushu Univ. (Japan))

We developed a small wireless device based on a lensless CMOS imaging system that enables observing the neural activities in the mouse brain. The weight of the device was 4.6 g and the dimensions were 15 × 24 mm2 with a Bluetooth low-energy (BLE) module and a microcontroller embedded analog-to-digital (ADC) function. This device is driven by a 3-V lithium coin battery. This system has successfully transferred the image at a frame rate of 0.95 fps with a 16×30-pixel size. The result suggests that the device could be applied for in-vivo experiments in a freely moving mouse.

2:45 PM - 3:00 PM

[D-6-05] An Extended-Gate-Type Organic Field-Effect Transistor Functionalized with a Dimercapto Thiadiazole Derivative for the Detection of Mercury(II) Ions at Picomolar Level

○Shijun Shi[1], Kohei Ohshiro[1], Qi Zhou[1], Hikaru Tanaka[2], Akari Yamagami[2], Kazutake Hagiya[2], Tsuyoshi Minami[1]
(1. Inst. of Indus. Sci., Univ. of Tokyo (Japan), 2. TOYOBO Corp., Ltd. (Japan))

Mercury(II) ions in environmental water (e.g., river) causes a significant risk to human health. Herein, we report an ultrasensitive detection of mercury(II) ions by an extended-gate-type organic field-effect transistor (EG-OFET). The EG-OFET functionalized with a dimercapto thiadiazole derivative-based self-assembled monolayer (SAM) realized the sensitive and selective detection of mercury(II) ions at pM levels in an aqueous solution. Moreover, a real-sample analysis was demonstrated for river water.

3:00 PM - 3:15 PM

[D-6-06] Efficient OTFT Array Measurement for the Long-Term Reliability Evaluation using External Measurement Board

〇Yasuhiro Ogasahara[1], Kazunori Kuribara[1], Takashi Sato[2]
(1. National Inst. of Advanced Indus. Sci. and Tech. (AIST) (Japan), 2. Kyoto University (Japan))

Abstract— We propose an efficient many-element measurement system for long-term reliability evaluation of organic thin-film-transistor (OTFT). Based on the silicon transistor array measurement method, we designed a dedicated printed circuit board for measurement, and constructed the array measurement system of OTFT. The proposed measurement system can measure the OTFT array in (sweep time of source measure unit) × (number of OTFTs) period, and took 17 minutes for 17 pOTFTs (502 point/sweep, 3 Vds and 3 Vgs sweep conditions) in trial experiment.

3:15 PM - 3:30 PM

[D-6-07] Low-voltage operation of pentacene-based floating-gate memory utilizing N-doped LaB_6 metal and high-k LaB_xN_y insulator stacked structure

〇Eun-Ki Hong[1], Shun-ichiro Ohmi[1] (1. Tokyo Inst. of Tech. (Japan))

In this paper, we have investigate low-voltage opera-tion of pentacene-based floating-gate memory utilizing nitrogen-doped (N-doped) LaB6 metal and LaBxNy insu-lator stacked structure. The Ar/N2-plasma nitridation was found to be effective to suppress the leakage current between the Au source/drain and N-doped LaB6 float-ing-gate. The pentacene-based floating-gate memory was successfully developed with memory window (MW) of 0.4 V under program/erase (P/E) voltage and time of ±3 V/100 μs, and the process temperature of 200 °C maximum.

Session information

Oral Presentation

Joint Session (Area1&10)

[E-4] Oxide Semiconductors for Logic and Memory Applications

Wed. Sep 28, 2022 9:00 AM - 11:15 AM 105 (1F)

Session Chair: Mamoru Furuta (Kochi Univ. of Technology), Masaharu Kobayashi (Univ. of Tokyo)

9:00 AM - 9:30 AM

[E-4-01 (Invited)] Atomic-layer-deposited atomically thin In2O3 channel for BEOL logic and memory applications

○Peide D. Ye[1] (1. Purdue Univ. (United States of America))

9:30 AM - 10:00 AM

[E-4-02 (Invited)] Opportunity of Monolithic 3D Compute-in-Memory Technology

Yuan-Chun Luo[1], ○Shimeng Yu[1] (1. Georgia Institute of Technology (United States of America))

10:00 AM - 10:15 AM

[E-4-03] Optimum Composition Ratio of CAAC-IGZO

○Toshiki Hamada[1], Yuichi Sato[1], Motomu Kurata[1], Naoki Okuno[1], Hitoshi Kunitake[1], Shunpei Yamazaki[1]
(1. Semiconductor Energy Laboratory Co., Ltd. (Japan))

Focusing on the composition ratios of indium to gallium and zinc in field-effect transistors using a c-axis-aligned crystalline oxide semiconductor as a channel material (OSFETs), we have performed fundamental evaluation of IGZO films and evaluation of the electrical characteristics of the OSFETs. The results of the Hall effect measurement and the electrical characteristics evaluation show that an OSFET with an In-rich composition has high mobility but exhibits normally-on characteristics, while an OSFET with an Zn-rich composition exhibits favorable normally-off characteristics.

10:15 AM - 10:30 AM

[E-4-04] Nanoscale Trench-Gate Self-Aligned C-Axis Aligned Crystalline Indium-Gallium-Zinc Oxide Field-Effect Transistor using Cap Layer

○MASAHIRO WAKUDA[1], Motomu Kurata[1], Satoru Saito[1], Shunichi Ito[1], Ryo Arasawa[1], Shinya Sasagawa[1], Kentaro Sugaya[1], Yoshikazu Hiura[1], Hidekazu Miyairi[1], Yuji Egi[1], Ryota Hodo[1], Hitoshi Kunitake[1], Shunpei Yamazaki[1]
(1. Semiconductor Energy Laboratory Co., Ltd. (Japan))

Highly accurate nanoscale fabrication technology is required to enable nanoscale field-effect transistors (FETs) using crystalline oxide semiconductors to have good switching characteristics. As a structure satisfying the requirements, a trench-gate self-aligned FET using c-axis aligned crystalline indium-gallium-zinc oxide (IGZO) is provided with a film (cap layer) that protects a top and side surfaces of an S/D electrode and a side sur-face of an IGZO layer under the S/D electrode.

Short Break （10:30 AM - 10:45 AM）

10:45 AM - 11:00 AM

[E-4-05] 3D monolithic CAAC-IGZO/Si hybrid CMOS ring oscillator and 64 multiple states high efficient (>200TOPS/W) for Analog Memory Computing

○Min-Cheng Chen[1], Satoru Ohshita[2], Hidefumi Rikimaru[2], Yoshiyuki Kurokawa[2], Satoshi Watanabe[2], Yuki Imoto[2], Yoshinori Ando[2], Shang-Shiug Chuang[1], Hiroshi Yoshida[1], Ming-Han Liao[3], Shou-Zen Chang[1], Shunpei Yamazaki[2]
(1. Powerchip Semiconductor Manufacturing Corp. (Taiwan), 2. Semiconductor Energy Laboratory Co., Ltd. (Japan), 3. National Taiwan University (Taiwan))

We present a CAAC-IGZO/Si hybrid CMOS technology with monolithic 3D stacked high stability MIM/OS-FET in Si BEOL process. The insert OS-LSI process shows no impact on Si FEOL characteristic performance. A 51-stages CAAC-IGZO/Si hybrid CMOS ring oscillator capable of reducing 20% layout area has been successfully demonstrated. On the other hand, the CAAC-IGZO/Si Analog in-Memory Computing (AiMC) chip also achieves a multiple weighting states of 64, an operation efficiency of more than 200TOPS/W, and an inference accuracy larger than 90% (MNIST). We believe it is suitable for applications of decrypt encryption and/or IoT sensors.

11:00 AM - 11:15 AM

[E-4-06] Enabling area efficient oxide channel Fe-TFT based TCAM cell through monolithic 3D integration with low temperature annealing

○Hongrae Joh[1], Sooji Nam[2], Minhyun Jung[1], Sung Haeng Cho[2], Sanghun Jeon[1]
(1. Korea Advanced Institute of Science and Technology (KAIST) (Korea), 2. Electronics and Telecommunications Research Institute (Korea))

We demonstrate ferroelectric thin film transistor (Fe-TFT) devices with Al:IZTO oxide semiconductor channel through monolithic 3D (M3D) integration with low temperature (~250 °C) focused-microwave-annealing (FMA) process for area efficient ternary contents ad-dressable memory (TCAM) cell. The Fe-TFT shows large memory window (MW of 3.2 V), good endurance (108 cy-cles) and long retention properties. Furthermore, mono-lithically integrated Fe-TFTs based TCAM cells are demonstrated.

Session information

Oral Presentation

10: Thin Film Electronics: Oxide / Non-single Crystalline / Novel Process

[E-6] Advanced Oxide Sensors

Wed. Sep 28, 2022 1:30 PM - 3:30 PM 105 (1F)

Session Chair: Keisuke Ide (Tokyo Tech), Yusaku Magari (Shimane Univ.)

1:30 PM - 2:00 PM

[E-6-01 (Invited)] Robust Molecular Recognition Electronics using Metal Oxide Nanostructures

○Takeshi Yanagida[1] (1. Univ. of Tokyo / Kyushu Univ. (Japan))

2:00 PM - 2:15 PM

[E-6-02] Indium oxide-based thin film transistor with high CO_2 sensitive (400) plane

○Ayumu Nodera[1], Shun Mori[1], Shinya Aikawa[1] (1. Kogakuin University (Japan))

CO2 gas sensors operating at relatively low tempera-ture are demanded for many applications. In2O3 semi-conductor is a promising candidate in terms of material processability and gas sensitivity. In this study, we fabri-cated In2O3-based thin-film transistors (TFT) and inves-tigated their CO2 sensitivities at 150 °C. Pure In2O3 and In2O3 co-sputtered with CaO (In2O3:Ca) films were pre-pared as an active channel. The In2O3:Ca TFT showed better CO2 sensitivity, which the drain current was ap-proximately 3 times higher compared to the initial N2 environment. The In2O3:Ca films has a reactive (400) plane-rich crystal structure, thus, high CO2 sensitivity was obtained compared to the In2O3 TFT with a stable (222) plane.

2:15 PM - 2:30 PM

[E-6-03] Developing SnO_2 Based Flexible Humidity Sensor on Ultra-Soft Substrate for Breath Detection

○Moumita Deb[1], Po- Yi Chang[1,2,3], Pin- Hsuan Li[1], Ming- Jen Chen[4,5], Ya- Chuang Tian[4,5], Olivier Soppera[2,3], Hsiao- Wen Zan[1]
(1. Department of Photonics, College of Electrical and Computer Engineering, National Yang Ming Chiao Tung University, 1001 Ta Hsueh Rd. Hsinchu, Taiwan. (Taiwan), 2. Université de Haute-Alsace, CNRS, IS2M UMR 7361, F-68100 Mulhouse, France (France), 3. Université de Strasbourg, France (France), 4. Department of Medicine, Chang Gung University, Taoyuan 333, Taiwan (Taiwan), 5. Kidney Research Center and Department of Nephrology, Linkou Chang Gung Memorial Hospital, Taoyuan 333, Taiwan (Taiwan))

We have demonstrated SnO2 based flexible humidity sensor on food plastic wrap at low annealing tempera-ture (26.2 oC). As prepared sol-gel SnO2 film was an-nealed by low power near infrared (NIR) laser power 16 W/cm2. The proposed sensor has been tested under dif-ferent humidity (RH = 10 ~ 60%) with excellent resolu-tion (1.1% response per 0.1% RH). In addition, the sen-sor should be used to detect respiratory diseases by breath analysis.

2:30 PM - 2:45 PM

[E-6-04] A Novel Poly-Si/IGZO Thin-Film Transistor Process Platform for Sensor Applications

○Ping-Che Liu[1], Jen-Chi Liao[1], Chun-Jung Su[2], Pei-Wen Li[1], Horng-Chih Lin[1]
(1. Inst. of Electronics, National Yang Ming Chiao Tung Univ. (Taiwan), 2. Department of Electrophysics, National Yang Ming Chiao Tung Univ. (Taiwan))

We presented a novel three-mask scheme for fabricating a sensing cell consisting of a top-gated poly-Si thin-film transistor (TFT) and a bottom-gated IGZO TFT. The hybrid TFT sensing cell exhibits sharp transition with a high current ratio (≈ 1×10^5) between two switching levels.

2:45 PM - 3:00 PM

[E-6-05] The use of local etching and NiO capping layer to improve the performance of ultraviolet photodetectors based on SiZnSnO thin film transistors

○Wen-Hung Lai[1], Wei-Wen Chen[1], Rong-Ming Ko[2], Chao-Yen Chang[1], Chien-Hung Wu[3], Shui-Jinn Wang[1]
(1. Inst. of Microelectronics, Dept. of Electrical Eng., Univ. of National Cheng Kung University (Taiwan), 2. Academy of Innovative Semiconductor and Sustainable Manufacturing, Univ. of National Cheng Kung University (Taiwan), 3. Dept. of Optoelectronics and Materials Eng., Chung Hua University (Taiwan))

The use of a thick channel layer (Tch) with a locally etched region and a NiO capping layer (CL) thereon to release the trade-off between the dark current (Idark) and photo current (Iph) of UV photodetector based on SZTO TFT is demon-strated. The influences of the Tch and final thickness (Tchf) af-ter local etching, and NiO CL on the optoelectrical properties of SZTO TFTs are investigated. Experimental results show that the 100-nm-thick SZTO TFT with a Tchf of 40 nm and a NiO CL has excellent in Rph and Sph up to 1972 A/W and 1.9×10^7 A/A under UV irradiation at 275 nm, which are about 303 and 251 times larger than the conventional 30-nm-thick SZTO TFT. It's attributed to the use of a thick Tch and the formation of NiO CL/SZTO pn heterojunction maximize the harvest of photogenerated carriers to cause more negative ΔVth of TFT to boost Iph under UV irradiation, in addition, a thin effective Tch obtained from the local etching together with NiO CL is very effective in lowing Idark.

3:00 PM - 3:15 PM

[E-6-06] Ultraviolet photodetector based on a SiZnSnO thin film transistor with a stacked channel structure and a patterned NiO capping layer

○Hao-Che Cheng[1], Wei-Ting Chen[1], Rong-Ming Ko[2], Chao-Yen Chang[1], Chien-Hung Wu[3], Shui-Jinn Wang[1]
(1. Inst. of Microelectronics, Dept. of Electrical Eng., Univ. of National Cheng Kung University (Taiwan), 2. Academy of Innovative Semiconductor and Sustainable Manufacturing, Univ. of National Cheng Kung University (Taiwan), 3. Dept. of Optoelectronics and Materials Eng., Chung Hua University (Taiwan))

Ultraviolet photodetectors (UVPDs) based on SZTO thin-film transistors (TFTs) with a different carrier concentration of double channel layer (DCL) structure and NiO capping layer (CL) are reported. Experimental results indicate that proposed SZTO TFT UVPD with a 30-nm-thick upper layer stacked on a 50-nm-thick bottom layer and a patterned NiO CL has excellent detection performance in photoresponsivity and photosensitivity up to 1672 A/W and 1.03×10^7 A/A under illuminated at 275 nm, which increased by about 272 and 137 times than the conventional SZTO TFT with Tch of 30 nm. These improvements are due to the use of DCL increase the space for UV illumination and the use of NiO CL lowers the dark current and causes a considerable negative threshold voltage shift under UV irradiation to significantly boost the photocurrent.

3:15 PM - 3:30 PM

[E-6-07] Nitrogen incorporation in SnO_2 matrix for passivation of oxygen vacancy and hole generation

○Kotaro Watanabe[1], Takuma Kawaguchi[1], Shinya Aikawa[1] (1. Kogakuin Univ. (Japan))

For realization of high-performance p-type oxide-based semiconductors, nitrogen (N)-doping is one of the promising candidates. However, there still have unclear mechanism how hole is generated and where N atom is incorporated. In our previous study, we demonstrated n- to p-type conversion of SnOx film only by N2 annealing. Here, we show the role of N in n-type SnOx based on the detailed analysis of chemical binding states. The results suggest that N contributes important role in both VO passivation and hole generation in the SnOx film.

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-4] Emerging Memory Devices

Wed. Sep 28, 2022 9:00 AM - 10:15 AM 201 (2F)

Session Chair: Xu Bai (NanoBridge Semiconductor, Inc.), Atsushi Himeno (Panasonic Corporation)

9:00 AM - 9:15 AM

[F-4-01] Atomic Storage Random Access Memory for DRAM-like Applications

○Yu-Yu Lin[1], Feng-Min Lee[1], Dai-Ying Lee[1], Ming-Hsiu Lee[1], Keh-Chung Wang[1], Chih-Yuan Lu[1]
(1. Macronix International Co., Ltd. (Taiwan))

A high endurance atomic storage random access memory (AS-RAM) is proposed. The simple device structure provides potential advantage of scaling down and reaching larger cell density than DRAM devices at lower cost. The device configuration supports the random access feature and have low read and write latency due to the large read current and short programming pulse width down to 10ns. High program/erase endurance of more than 10^10 times is achieved. The AS-RAM is a promising candidate for DRAM-like memory.

9:15 AM - 9:30 AM

[F-4-02] Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates

○Koji Sakui[1], Nozomu Harada[1] (1. Unisantis Electronics Singapore Pte Ltd. (Singapore))

This paper proposes read non-destructive Dynamic Flash Memory (DFM). Similar to DRAM, refresh is required, but fast block refresh can improve the duty ratio. Analogous to Flash, “0” Erase, “1” Program, and Read are necessary, but the holes can be regenerated while read for realizing the read non-destructive DFM.

9:30 AM - 9:45 AM

[F-4-03] A Capacitorless DRAM Based on Bulk FinFET for the Immune of Work-Function Variation Effect

○Sang Ho Lee[1], Jin Park[1], So Ra Min[1], Geon Uk Kim[1], Ga Eon Kang[1], Jun Hyeok Heo[1], Young Jun Yoon[2], Jae Hwa Seo[3], Jaewon Jang[1], Jin-Hyuk Bae[1], Sin-Hyung Lee[1], In Man Kang[1]
(1. Kyungpook National Univ. (Korea), 2. Korea Atomic Energy Res. Inst. (Korea), 3. Korea Electrotechnology Res. Inst. (Korea))

9:45 AM - 10:00 AM

[F-4-04] NAND Memory Composed of Crystalline In-Ga-Zn Oxide FETs with Endurance of over 10^{13} Cycles at 20-ns Write Time without Batch Erase

○Shoki Miyata[1], Satoru Oshita[1], Hitoshi Kunitake[1], Yuki Okamoto[1], Hiroki Inoue[1], Hiromi Sawai[1], Kunihiro Fukushima[1], Yusuke Komura[1], Takanori Matsuzaki[1], Yoshiyuki Kurokawa[1], Tatsuya Onuki[1], Hajime Kimura[1], Shinya Sasagawa[1], Shunpei Yamazaki[1]
(1. Semiconductor Energy Laboratory Co., Ltd. (Japan))

Development of emerging memories for artificial intelligence is accelerating. Memory with In-Ga-Zn oxide FETs has an advantage of being monolithically stackable on Si CMOS, but the memory access needs to be improved. We propose NAND memory composed of crystalline oxide semiconductor (which we call "OS NAND"). Operation of OS NAND is different in principle from that of NAND flash memory or emerging nonvolatile memories; charge is written through a semiconductor layer in OS NAND. Our OS NAND has outstanding performance, such as endurance of over 10^13 cycles and write time of 20 ns.

10:00 AM - 10:15 AM

[F-4-05] Improving Synaptic Functionalities in Chitosan-based Electric-double-layer Transistors via Random Network Polysilicon Nanowire Channel

○KI-WOONG PARK[1], Won-Ju Cho[1] (1. Univ. of Kwangwoon (Korea))

In this study, the synaptic functionalities of artificial synaptic transistors were improved by nanowire-type polysilicon channel structures. The channel conductance, which is interpreted as synaptic plasticity, is efficiently modulated due to a high surface-to-volume ratio of the nanowire channel. As a result, the hysteresis window of the nanowire-type synaptic transistors was larger than that of the film-type synaptic transistors even in the same gate voltage sweeping range. In addition, the NW-type synaptic transistors were found to have superior short-term facilitation properties than the film-type ones through the measured PPF characteristics and frequency-dependent EPSC characteristics.

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-5] 3D NAND Flash Memory

Wed. Sep 28, 2022 10:45 AM - 12:00 PM 201 (2F)

Session Chair: E Ray Hsieh (National Central Univ.), Keiji Hosotani (KIOXIA Corp.)

10:45 AM - 11:15 AM

[F-5-01 (Invited)] Scaling Perspectives on 3D NAND Flash

○Akira Goda[1] (1. Micron (Japan))

11:15 AM - 11:30 AM

[F-5-02] Analysis of Grain Boundary Effect in GIDL-erase-scheme Vertical CTF Strings for High Stacked CMOS under Array 3-D NAND Flash

○Moonkyu Song[1], Joe Friedman[1], Sanjay K. Banerjee[1] (1. Univ. of Texas at Austin (United States of America))

11:30 AM - 11:45 AM

[F-5-03] Performance Improvement by Applying High-k Materials for 3D NAND Memory Block Oxide with a Lower Thermal Budget

○Sara Aoki[1], Loan Nguyenhong[1], Muneyuki Otani[2], Naonori Fujiwara[2], Genji Nakamura[1]
(1. Tokyo Electron Ltd. (Japan), 2. Tokyo Electron Technology Solutions Ltd. (Japan))

Alternative materials for Al2O3 used in block oxide in 3D NAND were investigated. Memory characteristics of ZrO2, HfO2, and HfSiO (Si: Hf = 6:94) were thoroughly examined considering the thermal budget. Materials with higher k-values outperformed Al2O3 in terms of window performance due to the improved erase characteristics. It was also discovered that the thermal processing after high-k deposition affects memory qualities and that lower thermal processing temperatures result in better memory characteristics. Degradation of characteristics during high temperature annealing is assumed to be due to mixing that occurred at the interface. The effect of distortion of band structure and increase of defects due to mixing on memory characteristics and its mechanism are discussed.

11:45 AM - 12:00 PM

[F-5-04] Microscopic Physical Origin of Charge Traps in 3D NAND Flash Memories

○Fugo Nanataki[1], Jun-ichi Iwata[2,3], Kenta Chokawa[4], Masaaki Araidai[1,4], Atsushi Oshiyama[4], Kenji Shiraishi[1,4]
(1. Univ. of Nagoya (Japan), 2. Tokyo Inst. of Tech. (Japan), 3. Quemix Inc. (Japan), 4. Inst. of Materials and Systems for Sustainability (Japan))

We investigated hydrogen (H) impurity and nitrogen (N) vacancy complexes by the first-principles calculations to clarify the origin of charge traps inside SiN layer in 3D-NAND flash memories. We revealed that N vacancies attract H impurities. One Si dangling bond on N vacancies (VN) is saturated with one H atom and other two Si atoms form Si-Si bond (VN-H complex). We also examined the electronic structures and stable charge states of VN-H complexes and revealed that the complex can capture charge. In conclusion, we have found that VN and a H impurity are likely to form a VN-H complex and that the VN-H complex is the origin of charge traps in 3D NAND flash memories.

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-6] Charge-Based Memory Devices for AI Applications

Wed. Sep 28, 2022 1:30 PM - 3:00 PM 201 (2F)

Session Chair: Hiroki Sasaki (MIRISE Technologies Corp.), E Ray Hsieh (National Central Univ.)

1:30 PM - 1:45 PM

[F-6-01] CMOS-compatible Charge-trap Transistors with Engineered Tunnel-barrier for Artificial Synaptic Electronics

○KI-WOONG PARK[1], Won-Ju Cho[1] (1. Univ. of Kwangwoon (Korea))

In this study, we proposed the silicon-on-insulator (SOI)-based charge-trap synaptic transistors with engineered tunnel barrier. The charge-trap transistors with mature CMOS-compatible technology can gradually and stably modulate channel conductance through the charge trapping layer and electron tunneling. The engineered charge trapping layer realized artificial synaptic operation by emulating the excitatory post-synaptic current (EPSC) response and long-term potentiation/depression behaviors for multiple gate stimulation. In addition, the charge-trap transistors reliable mimicked the synaptic operation even at a high temperature of 125 oC. As a result, we proposed the in-memory computing possibility for artificial neural network systems with charge-trap synaptic transistors.

1:45 PM - 2:00 PM

[F-6-02] Synaptic Devices Based on 3D-Semicircular NAND Flash Memory

○Seongbin Oh[1,2], Seungwhan Kim[1,2], Ho-Nam Yoo[1,2], Woo Young Choi[1,2], Jong-Ho Lee[1,2]
(1. Seoul National Univ. (Korea), 2. Inter-University Semiconductor Research Center (Korea))

A novel 3D NAND flash memory is proposed which
uses a single hole as two strings (1H2S) for low-power and
high-density neuromorphic computing. Independent operation of two strings and selective program/erase operation were verified by using 3D-TCAD simulation. Finally,
the spiking neural networks (SNNs) based on a 3D NAND
synaptic array achieved 88.25% accuracy when applied to
the CIFAR-10 data sets.

2:00 PM - 2:15 PM

[F-6-03] Variation-robust Binary Matrix-vector Multiplication Method

○Hyeongsu Kim[1], Inseok Lee[1], Woo Young Choi[1], Byung-Gook Park[1], Jong-Ho Lee[1] (1. Seoul Nat'l Univ. (Korea))

Using two Flash memory devices and one capacitor as a synaptic cell, we present a variation-robust cal-culation method for binary matrix-vector multiplica-tion in this study. Spice simulation is used to examine the Vth variation impacts on the conventional current summation method and the proposed method. The sim-ulation results demonstrate that the proposed strategy is much more tolerant of Vth variation.

2:15 PM - 2:30 PM

[F-6-04] Implementation of Homeostasis Functionality in Hardware-Based Spiking Neural Networks Using an STDP Learning Rule

○Jangsaeng Kim[1], Woo Young Choi[1], Byung-Gook Park[1], Jong-Ho Lee[1] (1. Seoul National University (Korea))

We propose the two implementation methods of homeostasis functionality in hardware-based spiking neural networks (SNNs). The performance of the proposed implementation methods was evaluated through the MNIST dataset classification. Both implementation methods show high performance and a significantly higher recognition rate (~92%) than when homeostasis functionality was not used (~80%). The TFT-type flash memory cells are used as synaptic devices.

2:30 PM - 2:45 PM

[F-6-05] Effects of Static Current in AND-Type TFT Synaptic Devices on Supervised On-Chip Training

○Dongseok Kwon[1], Soochang Lee[1], Seongbin Oh, Chul-Heung Kim[1], Jae-Joon Kim[1], Jong-Ho Lee[1] (1. Seoul National Univ. (Korea))

2:45 PM - 3:00 PM

[F-6-06] Junctionless Based Charge Trapping Memory for Neuromorphic Applications

○Md. Hasan Ansari[1], Nazek El Atab[1] (1. King Abdullah University of Science and Technology (Saudi Arabia))

In this work, a double gate Junctionless transistor with independent gate operations mimics human behaviors. The front gate with charge trapping in the nitride layer operates as a non-volatile memory, capturing the long-term potentiation (LTP) and depression (LTD). The back gate with single oxide operates as a floating body memory and captures the short-term potentiation (STP) of human behavior. Furthermore, the estimated conductance values are utilized for deep neural networks for image recognition where they are shown achieve 95.37% accuracy for (MNIST) pattern recognition task.

Session information

Oral Presentation

Focus Session 1 (Area1&2&9)

[G-4] Quantum Computing 2

Wed. Sep 28, 2022 9:00 AM - 10:15 AM 301 (3F)

Session Chair: Yuichiro Matsuzaki (AIST), Takashi Matsukawa (AIST)

9:00 AM - 9:30 AM

[G-4-01 (Invited)] High Volume Cryogenic Characterization of Silicon Spin Qubit Devices from a 300mm Process Line

○Otto Zietz[1], Samuel Neyens[1], Ravi Pillarisetty[1], Thomas Watson[1], Hubert George[1], Eric Henry[1], Florian Luthi[1], Roza Kotlyar[1], Lester Lampert[1], Guoji Zheng[1], Joelle Corrigan[1], Stephanie Bojarski[1], Jeanette Roberts[1], Jim Clarke[1]
(1. Intel (United States of America))

9:30 AM - 10:00 AM

[G-4-02 (Invited)] Challenge and Opportunity of Low-power Nonvolatile FPGA using NanoBridge for Cryogenic Quantum Controller

○Munehiro Tada[1] (1. NanoBridge Semiconductor, Inc. (Japan))

10:00 AM - 10:15 AM

[G-4-03] Single-Electron Transport Control for Qubit Initialization in Silicon Quantum Dot Arrays

○Takeru - Utsugi[1], Noriyuki - Lee[1], Ryuta - Tsuchiya[1], Toshiyuki - Mine[1], Gou - Shinkai[1], Itaru - Yanagi[1], Yusuke - Kanno[1], Tomonori - Sekiguchi[1], Satoru - Akiyama[1], Takayasu - Norimatsu[1], Yusuke - Wachi[1], Raisei - Mizokuchi[2], Jun - Yoneda[2], Tetsuo - Kodera[2], Shinichi - Saito[1], Digh - Hisamoto[1], Hiroyuki - Mizuno[1] (1. Hitachi, Ltd. (Japan), 2. Tokyo Inst. of Tech. (Japan))

We demonstrated a single-electron transport in a quantum dot (QD) array. We used the parallel gates in the array as a single electron pump (SEP) and synchronously operated the subsequent gates of the SEP as QD shutters, loading a single electron into each QD in the array. The SEP can operate at 100 MHz with the accuracy of 99% at 4 K. By controlling the timing of the shutter operation, the jitter representing electron transfer timing fluctuation is less than 10 ns, which is much shorter than the expected operation time of the silicon qubits. Therefore, the developed single-electron transport can be used for performing qubit initialization in a silicon-based quantum computer.

Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[G-5] Image Sensor Technology

Wed. Sep 28, 2022 10:45 AM - 12:15 PM 301 (3F)

Session Chair: Takashi Matsukawa (AIST), Hidetoshi Oishi (Sony Semiconductor Solutions Corp.)

10:45 AM - 11:15 AM

[G-5-01 (Invited)] 3D Sequential Process Integration for CMOS Image Sensor

○Junpei Yamamoto[1], Keiichi Nakazawa[1], Shigetaka Mori[1], Shintaro Okamoto[1], Akito Shimizu[1], Koichi Baba[1], Nobutoshi Fujii[1], Mutsuo Uehara[1], Katsunori Hiramatsu[1], Hideomi Kumano[1], Akira Matsumoto[1], Koichiro Zaitsu[1], Hidetoshi Onuma[1], Keiji Tatani[1], Tomoyuki Hirano[1], Hayato Iwamoto[1] (1. Sony Semiconductor Solutions Corp. (Japan))

11:15 AM - 11:30 AM

[G-5-02] Quantitative Analysis of Petal Flare depending on Pixel Size in CMOS Image Sensors

○SANGIN BAE[1], Jinmyoung Mok[1], Jeongmin Bae[1], Hyung-Keun Gweon[1], Yunki Lee[1], Younggyu Jeong[1], Bumsuk Kim[1], Jungchak Ahn[1] (1. Samsung Electronics Corp., Ltd. (Korea))

A petal flare that are determined by a periodic struc-ture of CMOS image sensor produces repetitive virtual images in specific direction and severely affects image quality. Since theoretical modeling for the cause of petal flare is still insufficient, it is difficult to quantitatively compare different petal flares from different types of CMOS image sensors. In this paper, we introduce an ana-lytical flare model by coupling pixel-level wave optic simulation and module-level ray optic simulation, and suggest a novel evaluation method to quantitatively measure the flare level. A flare index (F.I.) defined from the intensity profile of flare image clearly shows that the pixel size mainly affects the flare pattern as well as dif-fraction efficiency. The novel quantitative analysis and evaluation of petal flare will contribute to overcoming physical obstacles towards sub-micron CMOS image sensor.

11:30 AM - 11:45 AM

[G-5-03] Influence of Neutron Irradiation on CMOS Image Sensors

○Gyeong Jin Lee[1], Hyungchae Kim[1], Junghyun Kim[1], Myeongeon Kim[1], Seunghan Hong[1], Jonghoon Park[1], Yunki Lee[1], Bumsuk Kim[1], JungChak Ahn[1] (1. Samsung Electronics Co., Ltd. (Korea))

In this article, we investigated the influence of neutron irradiation in the perspective of white spot (WS) creation. By irradiating neutron on CMOS image sensors (CISs), it was found that the number of WS creation was directly governed by exposure time and the distance from neutron source. By shielding the neutron flux, we further con-firmed both high energy and thermal neutrons made WS. In addition, we calculated activation energy of the defects and concluded that the defects were formed in silicon bulk by displacement damage of neutrons.

11:45 AM - 12:00 PM

[G-5-04] Flexible Integrated Circuits Developed by Layer Transfer Process of FDSOI MOSFETs

○Masahide Goto[1], Shigeyuki Imura[1] (1. NHK Sci. & Tech. Res. Labs. (Japan))

We report flexible integrated circuits (ICs) via the layer transfer process of fully depleted silicon-on-insulator (FDSOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) onto a plastic substrate. Our device combines the high performance of single crystalline silicon (sc-Si) MOSFETs and the flexibility of plastic. A 6-μm thick FDSOI device with 50-nm thick MOSFET active layers and aluminum wires is successfully transferred to a plastic substrate. In addition to mechanical flexibility, operation of ICs including complementary metal-oxide semiconductor (CMOS) inverters and 101-stage ring oscillators is confirmed, indicating their potential in flexible highly integrated devices, such as image sensors and displays.

12:00 PM - 12:15 PM

[G-5-05 (Late News)] Near-Infrared Sensitivity Enhancement of Silicon Image Sensor by Photon Confinement with Plasmonic Diffraction

○Takahito Yoshinaga[1], Kazuma Hashimoto[1], Nobukazu Teranishi[2], Atsushi Ono[1,2]
(1. Shizuoka Univ. (Japan), 2. RIE Shizuoka Univ. (Japan))

Session information

Oral Presentation

Joint Session (Area1&2)

[G-6] Ferroelectric Devices

Wed. Sep 28, 2022 1:30 PM - 3:15 PM 301 (3F)

Session Chair: Halid Mulaosmanovic (GlobalFoundries), Masaharu Kobayashi (Univ. of Tokyo)

1:30 PM - 1:45 PM

[G-6-01] The First Demonstration of High-performance Top-gated BEOL Ferroelectric Memtransistor thorough ITO-IGZO Heterojunction Channel Engineering

○ChunKuei CHEN[1], Sonu Hooda[1], Zihang Fang[1], Shih-Hao Tsai[1], Evgeny Zamburg[1], Aaron Voon-Yew Thean[1]
(1. Univ. of Singapore (Singapore))

For the first time, we demonstrate high-performance top-channel ferroelectric FETs by engineering an InSnOx/InGaZnOx heterojunction interface with HfZrOx. The device process thermal budget is very low, making it highly suitable for monolithic 3D integration with low-k/Cu back-end-of-line. Reliable top-gated channel FeFETs with sputter-deposited IGZO is notoriously difficult to achieve, due to the poor quality assurance of gate-channel interface, which is further challenged by the BEOL thermal budget constraints. Through heterojunction channel engineering, our top-gated FeFETs spot record performance metrics that are among the best-in-class IGZO FeFETs reported to date, featuring low interface/bulk trap density, high electron mobility of 57cm2/Vs, near-ideal subthreshold swing (S.S.) of 64mV/dec., and high endurance exceeding 107 cycles.

1:45 PM - 2:00 PM

[G-6-02] Comprehensive Evaluation of Ferroelectric-Metal FET with Stacked-Nanosheet Architecture for Memory and Synapse Applications

○Heng Li Lin[1], Pin Su[1] (1. Inst. of Electronics, Univ. National Yang Ming Chiao Tung (Taiwan))

We have conducted a comprehensive evaluation for the ferroelectric-metal FET with stacked-nanosheet architecture (FeM-Nanosheet) using Monte-Carlo simulations with nucleation-limited-switching (NLS) based model. In addition to the area-ratio (AR) effect enabled by increasing the number of tiers, our study suggests that adequately adjusting the FE (orthorhombic phase) percentage can further boost the memory window of the FeM-Nanosheet NVM. Moreover, using the FE percentage as a knob, the interlayer field which is crucial to reliability and the depolarization field which is important to data retention can also be reduced. For synapses conductance response, our study indicates that the AR can raise the effective W/L to boost the drain current and Gmax/Gmin, while adjusting the FE percentage can be used to optimize the conductance response including linearity and symmetry for the FeM-Nanosheet synapse under the stimulation of identical pulse chain.

2:00 PM - 2:15 PM

[G-6-03] Investigation and Mitigation of Write Disturb for 1T FeFET NVM considering Accumulation Effect

○Po-Yi Lee[1], Yi-Chin Luo[1], Pin Su[1] (1. Inst. of Electronics, Univ. of National Yang Ming Chiao Tung (Taiwan))

We have investigated the write disturb problem for 1T-FeFET NVM by using time-domain Monte-Carlo simulations with nucleation-limited switching (NLS) model that can capture the ferroelectric accumulative switching behavior. Our study indicates that the accumulation effect is crucial to the FeFET dynamic response under disturb cycles, and adequately reducing the writing voltage (Vw) or employing Vw/3 inhibition scheme can significantly mitigate the disturb. Besides, we have explored the feasibility of utilizing textured ferroelectric with (111)-orientation to mitigate the write disturb problem for the 1T-FeFET NVM.

2:15 PM - 2:30 PM

[G-6-04] Boosting the Erase Efficiency of FDSOI FeFET by the Band-to-Band Tunneling Process

○Xiaole Jia[1], Chengji Jin[1], Jiajia Chen[1], Lulu Chou[2], Huan Liu[1], Zhi Gong[1], Yue Peng[2], Yan Liu[2], Xiao Yu[1], Genquan Han[2]
(1. Zhejiang Lab (China), 2. Xidian University (China))

We have theoretically investigated the memory characteristics, especially for erase operation of fully-depleted sili-con-on-insulator (FDSOI) ferroelectric field-effect transistor (FeFET) by considering the band-to-band tunneling (BTBT). It is found that the significantly increased hole concentration in the channel region due to BTBT is more favorable in the po-larization switching during erase operation. As a result, the BTBT boosts erase efficiency and memory window of the FDSOI FeFET.

2:30 PM - 2:45 PM

[G-6-05] Impact of Polarization States Changing on Effective Carrier Mobility of HfZrO*x* Ferroelectric Field-Effect Transistor

○Fenning Liu[1], Yue Peng[1,2], Genquan Han[1,2,3], Yan Liu[1,2], Yue Hao[1]
(1. Wide Bandgap Semiconductor Technology Disciplines State Key Laboratory, School of Microelectronics Xidian Univ. (China), 2. Zhejiang Lab. (China), 3. Hangzhou Institute of Technology, Xidian University (China))

The impact of polarization states changing on effective carrier mobility (μeff) of HfZrOx (HZO) ferroelectric field-effect transistor (FeFET) is demonstrated. The μeff of the HZO FeFET decreases with the increase of erase pulses, while increases with the write pulses. The results show that the μeff of the HZO FeFET at different polarization states is smaller than that in the initial state, which was caused by the positive charges (e.g. oxygen vacancies V_O^(2+)) detrapping/trapping.

2:45 PM - 3:00 PM

[G-6-06] ZrO_2/Si Gate Stack for Antiferroelectric MFIS Capacitors and Antiferroelectric Si n-FETs

○Xuan Luo[1], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1] (1. Univ. of Tokyo (Japan))

We investigate the properties of antiferroelectric (AFE) ZrO2 ultrathin films on Si in MFIS capacitors and AFE FETs. ZrO2 directly deposited on Si with Si chemical oxides shows a low interface trap density and exhibits AFE characteristics with double hysteresis loops. An n-channel FET with the AFE ZrO2 gate insulator shows polarization switching in P-V characteristics and ferroelectric hysteresis in Id-Vg characteristics under unipolar voltage operation.

3:00 PM - 3:15 PM

[G-6-07 (Late News)] Modeling and Simulation of Antiferroelectric FETs with Oxide Semiconductor Channel Using Half-Loop Hysteresis for Memory Applications

○Xingyu HUANG[1], Yuki ITOYA[1], Zhuo LI[1], Takuya SARAYA[1], Toshiro HIRAMOTO[1], Masaharu KOBAYASHI[1] (1. Univ. of Tokyo (Japan))

Session information

Oral Presentation

08: Low Dimensional Devices and Materials

[H-4] Device Application I: Low Dimensional Devices and Materials

Wed. Sep 28, 2022 9:00 AM - 10:00 AM 302 (3F)

Session Chair: Takamasa Kawanago (Tokyo Tech), Takayuki Arie (Osaka Metropolitan Univ.)

9:00 AM - 9:15 AM

[H-4-01] Efficient and Chiral Electroluminescence from In-Plane Heterostructure of Transition Metal Dichalcogenide Monolayers

○Jiang Pu[1], Naoki Wada[2], Yuhei Takaguchi[2], Wenjin Zhang[3], Zheng Liu[4], Takahiko Endo[2], Toshifumi Irisawa[4], Kazunari Matsuda[3], Yuhei Miyauchi[3], Yasumitsu Miyata[2], Taishi Takenobu[1]
(1. Nagoya Univ. (Japan), 2. Tokyo Metropolitan Univ. (Japan), 3. Kyoto Univ. (Japan), 4. AIST (Japan))

This study demonstrated interfacial electrolumines-cence (EL) in diverse transition metal dichalcogenide (TMDC) in-plane heterostructures. Various combina-tions of single-crystalline in-plane heterostructures with sharp interfaces were grown by chemical vapor deposition (CVD), followed by adopting electro-lyte-based light-emitting devices (LEDs) to observe EL. The fine heterostructures enabled the capture of the linear-shaped EL fixed along the junction interfaces. Significantly, the WS2/WSe2 in-plane heterostructures exhibited circularly polarized EL with a polarizability of 10% at room temperature. These findings pave the way for monolayer in-plane heterostructures to use in functional optoelectronic devices.

9:15 AM - 9:30 AM

[H-4-02] In-plane Gate Graphene Transistor with Epitaxially Grown Molybdenum Disulfide Passivation Layers

○Po-Cheng Tsai[1], Chun-Wei Huang[2], Che-Jia Chang[2], Shu-Wei Chang[2], Shih-Yen Lin[2]
(1. Univ. of Taiwan (Taiwan), 2. Res. of Applied Sciences (Taiwan))

9:30 AM - 9:45 AM

[H-4-03] Work function modulation of Au/Bi bilayer system toward *p*-type WSe_2 FET

○Ryuichi Nakajima[1], Tomonori Nishimura[1], Keiji Ueno[2], Kosuke Nagashio[1]
(1. The Univ. of Tokyo (Japan), 2. Saitama Univ. (Japan))

Au/ultrathin Bi bilayer contact was studied to acquire high performance p-type FET by suppressing defect-related Fermi level pinning. Low melting point and low density of states of Bismuth provide the damage-free contact and the modulation of effective work function by forming the bilayer contact. The modulation of effective work function was certainly observed by C-V measurement as a function of Bi thickness and p-type WSe2 Schottky FET was clearly demonstrated with Au/2-nm Bi electrodes.

9:45 AM - 10:00 AM

[H-4-04 (Late News)] Magnetic Domain Control and Magnetization Switching of Ferromagnetic Ni Nanolayer Patterns Designed as An Electrode for Si Nanowire Devices

○Zhe-rui Gu[1], Shinjiro Hara[1] (1. Univ. of Hokkaido (Japan))

Session information

Oral Presentation

08: Low Dimensional Devices and Materials

[H-5] Device Application II: Low Dimensional Devices and Materials

Wed. Sep 28, 2022 10:45 AM - 11:45 AM 302 (3F)

Session Chair: Shu Nakaharai (NIMS), Takeshi Yanagida (Univ. of Tokyo)

10:45 AM - 11:15 AM

[H-5-01 (Invited)] Heterostructures based on two-dimensional semiconductors

○Ryo Kitaura[1,2] (1. NIMS (Japan), 2. Nagoya Univ. (Japan))

11:15 AM - 11:30 AM

[H-5-02] Continuous Color-Tunable Light-Emitting Devices Based on Compositionally Graded Monolayer Transition Metal Dichalcogenide Alloys

○Hao Ou[1], Jiang Pu[1], Tomoyuki Yamada[1], Naoki Wada[2], Hibiki Naito[2], Zheng Liu[3], Toshifumi Irisawa[4], Yusuke Nakanishi[2], Yasumitsu Miyata[2], Taishi Takenobu[1]
(1. Nagoya Univ. (Japan), 2. Tokyo Metropolitan Univ. (Japan), 3. AIST (Japan), 4. AIST (Japan))

A color-tunable light-emitting device using composi-tionally graded monolayer transition metal dichalco-genide alloy was fabricated. The monolayer WS2/WSe2 alloy was grown by chemical vapor deposition and showed bandgap variation from 2.1 eV to 1.7 eV, from WS2-rich side to WSe2-rich side. By using electro-lyte-based light-emitting device structure, the recombi-nation zone of the device could be tuned laterally. With the graded composition inside the channel region, the light-emitting device exhibited continuous and reversi-ble color tunability when emitting light at different voltages. Our results provide a new approach for the exploration of broadband optoelectronics based on monolayer semiconductors.

11:30 AM - 11:45 AM

[H-5-03] Improved Spectral Range and Responsivity with Mixed Dimensional (0D WS_2 QDs/ 2D MoS_2) Broadband Photodetector

○Parikshit Sahatiya[1], Venkatarao Selamneni[1], Chandra Sekhar Reddy Kolli [1] (1. BITS pilani, Hyderabad campus (India))

Mixed dimensional heterostructures are gaining a lot of attention to increase the spectral range of the photo-detector. In this work, high-performance broadband (UV-visible) photodetector was demonstrated by dec-orating zero-dimensional (0D) WS2-QDs on two-dimensional (2D) monolayer MoS2. WS2-QDs have absorbance in UV range and MoS2 is sensitive to visi-ble light. By proper contact engineering and discrete distribution of WS2 QDs over monolayer MoS2, the spectral range of MoS2 have been increased towards UV. The maximum responsivity was found to be ~ 392 A/W at 554 nm wavelength. In this report, not only the photodetection range is increased but also responsivity is improved which is a major step in the development of next-generation optoelectronics.

Session information

Oral Presentation

08: Low Dimensional Devices and Materials

[H-6] Growth and Synthesis: Low Dimensional Devices and Materials

Wed. Sep 28, 2022 1:30 PM - 3:00 PM 302 (3F)

Session Chair: Reina Kaji (Hokkaido Univ.), Shengnan Wang (NTT Basic Research Laboratories)

1:30 PM - 2:00 PM

[H-6-01 (Invited)] Growth of quantum dots and light source applications

○Kouichi Akahane[1], Atsushi Matsumoto[1], Toshimasa Umezawa[1], Naokatsu Yamamoto[1], Atsushi Kanno[1]
(1. National Inst. of Info. and Communications Tech. (Japan))

2:00 PM - 2:15 PM

[H-6-02] Control of the 3D SML Nanostructure Density by Topmost InAs Cycle Amount

○Ronel Christian Roca[1], Itaru Kamiya[1] (1. Toyota Tech. Inst. (Japan))

A wide control of the 3D SML nanostructure density in 10-stack SML nanostructures by varying the amount of InAs in the topmost and last cycle is demonstrated. By keeping the first 9 InAs SML cycles at 0.4 ML and only changing the last cycle from 0.5 to 0.9 ML, fine control across the transition from 2D to 3D SML growth regime can be realized. By uti-lizing this method, a high degree of control of the 3D SML nanostructure density is achieved, allowing for application specific density engineering of the SML nanostructures.

2:15 PM - 2:30 PM

[H-6-03] Near-IR and UV Photon Emissions from SiGe- and C-Quantum-Dots Fabricated by Hot-Ion Implantation into Si-Oxide Layers

○Tomohisa Mizuno[1], Kohki Murakawa [1], Hayato Ban[1], Takashi Aoki[1], Toshiyuki Sameshima[2]
(1. Kanagawa University (Japan), 2. Tokyo Univ. Agri. Tech. (Japan))

2:30 PM - 2:45 PM

[H-6-04] Chemical Properties of a PVD-ZrS_2 Film Underneath Scaled-High-*k*/IL-ZrO_2 Insulator Systems

○Masaki Otomo[1], Masaya Hamada[1], Ryo Ono[1], Iriya Muneta[1], Kuniyuki Kakushima[1], Kazuo Tsutsui[1], Hitoshi Wakabayashi[1]
(1. Tokyo Inst. of Tech. (Japan))

A ZrS2 film, which is a 2D-TMDC, stabilizes in air with a zirconium oxide film, which functions as a high-k interfacial layer. We fabricated high-k/PVD-ZrS2 stacks by introducing self-oxidized ZrO2 and analyzed their chemical properties. The results clarified that sulfur-vapor annealing (SVA) is essential for fabricating high-quality ZrS2 films by PVD and that the change in surface potential of the ZrS2 film due to interface dipoles between the high-k and ZrO2 films is suppressed with scaling of the high-k film thickness. In addition, SVA through the high-k film enhanced the quality of the ZrS2 film without affecting the surface potential, possibly enabling control of the threshold voltage in a ZrS2 MISFET.

2:45 PM - 3:00 PM

[H-6-05] Electromigration at nanocontacts of metal species of high-melting temperatures

○Yue Tian[1], Shaoqing Du[1,2], Kazuhiko Hirakawa[1,3]
(1. Inst. of Indus Sci., Univ. of Tokyo (Japan), 2. Shanghai inst. of microsystem and info. Tech. (China), 3. Inst. for Quantum Info. Electronics, Univ. of Tokyo (Japan))

We have investigated elementary processes of electromi-gration (EM) at Ni nanocontacts and observed that they are very different from those for Au nanocontacts. The critical voltage for EM, where metal atoms are removed by electri-cal stress, show a value determined by the surface diffusion potential of the metal and they do not show a dependence expected for Joule heating. We propose a model thata a very small fraction of electrons fly ballistically over the nanocontact region and transfer their kinetic energy to met-al atoms. The proposed model reasonably explains the lat-tice temperature dependence.

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-4] Ultrawide Bandgap Semiconductor Devices

Wed. Sep 28, 2022 9:00 AM - 10:15 AM 303 (3F)

Session Chair: Heiji Watanabe (Osaka Univ.), Hironori Okumura (Univ. of Tsukuba)

9:00 AM - 9:30 AM

[J-4-01 (Invited)] Beyond SiC: What's Next for Kilovolts Power Devices?

〇Yuhao Zhang[1] (1. Virginia Tech (United States of America))

9:30 AM - 9:45 AM

[J-4-02] Effect of Lattice Constraint on Structural Stability and Miscibility of (AlxGa1-x)2O3 Films: A First-Principles Study

〇Shuri Fujita[1], Toru Akiyama[1], Takahiro Kawamura[1], Tomonori Ito[1] (1. Mie Univ. (Japan))

The structural stability and miscibility of (AlxGa1-x)2O3 alloys is theoretically investigated by means of elec-tronic structure calculations within density functional theory. Effects of lattice constraint due to sapphire sub-strate on the structural stability and miscibility are eval-uated from the energy difference between α-phase and β-phase (AlxGa1-x)2O3 and excess energies. For constrained systems due to sapphire substrate, only α-phase (AlxGa1-x)2O3 is found to be stabilized. Furthermore, the calcu-lated excess energies indicate that the lattice constraint drastically improve the miscibility of (AlxGa1-x)2O3. These results suggest that the lattice constrain is crucial for the stability and miscibility of (AlxGa1-x)2O3 alloys.

9:45 AM - 10:00 AM

[J-4-03] 2DHG diamond MOSFETs with multi-finger structure for gate width expansion and improved RF characteristics

〇Akira Takahashi[1], Masakazu Arai[1], Yukiko Suzuki[1], Fuga Asai[1], Atsushi Hiraiwa[1], Masaomi Tsuru[3], Yutaro Yamaguchi[3], Yuji Komatsuzaki[3], Ken Kudara[3], Hiroshi Kawarada[1,2]
(1. Waseda univ Kawarada lab. (Japan), 2. Kagami Memorial Res. (Japan), 3. Mitsubishi Electric Corp. (Japan))

We have fabricated a high frequency 2DHG diamond
MOSFET with an air-bridge structure to increase the
gate width for further increasing the MOSFET power.
We succeeded in realizing a multi-finger structure with an increased number of gate fingers from the conventional double-finger structure. DC and RF performance of the double-finger devices and multi-finger devices were compared and investigated. As a result, the multi-finger devices did not degrade the current density due to the increase of gate width (WGT), and the maximum oscillation frequency (fmax) was increased by 1.5 times.

10:00 AM - 10:15 AM

[J-4-04 (Late News)] Efficient Optimization of Power Device Structure by Active Learning

〇Hayate Yamano[1], Alexander Kovacs[2], Johann Fischbacher [2], Katsunori Danno [1], Yusuke Umetani [1], Tetsuya Shoji [1], Thomas Schrefl [2] (1. Toyota Motor Corp. (Japan), 2. Danube Univ. Krems (Austria))

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-5] SiC Processes and Characterizations

Wed. Sep 28, 2022 10:45 AM - 12:00 PM 303 (3F)

Session Chair: Kung-Yen Lee (National Taiwan Univ.), Naoki Watanabe (Hitachi, Ltd.)

10:45 AM - 11:00 AM

[J-5-01] Structural Analysis of Bar-Shaped Single Shockley-Type Stacking Fault near the Substrate/Epilayer Interface and the Epitaxial Surface of 4H-SiC

○Johji Nishio[1], Chiharu Ota[1], Ryosuke Iijima[1] (1. Corporate R&D Center, Toshiba Corp. (Japan))

Partial dislocation combinations near the substrate/epilayer interface and the epilayer surface of 4H-SiC are analyzed for bar-shaped single Shockley-type stacking faults (1SSFs). Although the partial dislocations are found to have a zigzag structure similar to that found in triangular 1SSF, the combination is thought to be different. The features of the original basal plane dislocation are speculated on.

11:00 AM - 11:15 AM

[J-5-02] Influence of surface steps on the contraction of 4H-SiC basal plane dislocations

○Atsuo Hirano[1], Hiroki Sakakima[1], Asuka Hatano[1], Satoshi Izumi[1] (1. Univ. of Tokyo (Japan))

We investigated the dependence of the activation energy of the contraction of the BPD partial disloca-tions on the height of the surface step. We found that the steps could prevent the contraction of BPD partial dislocations in the case of the pair of Burgers vectors is open toward the step.

11:15 AM - 11:30 AM

[J-5-03] Auger recombination coefficient in 4H-SiC under the high injection condition

○Kazuhiro "-" TANAKA[1], Keisuke NAGAYA[1], Masashi KATO[1] (1. Nagoya Institute Technology (Japan))

We observed carrier recombination in 4H-SiC under the high injection condition by time resolved free carrier absorption measurements. Based on the observed decay curves, we estimated the Auger recombination coefficient. As a result, we found dependence of the Auger recombination coefficient on the excited carrier density.

11:30 AM - 11:45 AM

[J-5-04] Development of a Real-Time Temperature Measurement Technique for SiC Wafer During Ultra-Rapid Thermal Annealing Based on Optical-Interference Contactless Thermometry (OICT)

○Jiawen Yu[1], Kotaro Matsuguchi[1], Takuma Sato[1], Hiroaki Hanafusa[1], Seiichiro Higashi[1] (1. Hiroshima Univ. (Japan))

Heat diffusion of SiC wafer in planar and depth direction during atmospheric pressure thermal plasma jet performed ultra-rapid thermal annealing (URTA) has been visualized by an optical-interference contactless thermometry (OICT) imaging technique. A software program has been developed on the basis of image preprocessing and database to extract 3.5-dimensional (D) (x, y, z, and time) temperature distributions from observations in reflectance. The combination of OICT imaging and this software program achieves to obtain a 3.5-D temperature distribution in 3 seconds and demonstrated that it has potential real-time temperature measurement technique on URTA systems.

11:45 AM - 12:00 PM

[J-5-05] Doping properties of 4H-SiC using KrF excimer laser ablation with SiNx thin film

○Takuma - Yasunami[1], Daisuke - Nakamura[1], Keita - Katayama[1], Yoshiaki - kakimoto[1,2], Toshifumi - Kikuchi[1], Hiroshi - Ikenoue[1,2] (1. Univ. of Kyushu (Japan), 2. Department of Gigaphoton NEXT GLP (Japan))

KrF excimer laser was irradiated to 4H-SiC with an SiNx thin film and nitrogen was doped into 4H-SiC. We investigated the effect of changing the laser fluence and the number of irradiations on the doping properties. At a fluence of 2.5 J/cm², high-concentration doping was achieved while maintaining the surface flatness by solid-phase diffusion, whereas at a fluence of 2.8 J/cm², surface roughness was increased by melt diffusion. By increasing the number of irradiations, the internal diffusion of nitrogen was induced in the deep region while maintaining the surface flatness. Irradiation of 100 or more shots increased the contact resistance, suggesting the formation of defects inside the crystal during the solid-phase diffusion process.

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-6] Interface Technologies

Wed. Sep 28, 2022 1:30 PM - 3:45 PM 303 (3F)

Session Chair: Yuichi Onozawa (Fuji Electric Corp.), Shinsuke Harada (AIST)

1:30 PM - 1:45 PM

[J-6-01] Improvement of Channel Mobility in AlSiO/GaN MOSFETs using Thin Interfacial Layers to Reduce Border Traps

○Kenji Ito[1], Kazuyoshi Tomita[2], Daigo Kikuta[1], Masahiro Horita[2], Tetsuo Narita[1]
(1. Toyota Central R&D Labs., Inc. (Japan), 2. Nagoya Univ. (Japan))

The improvement of channel mobility for AlSiO/p-type GaN-based metal-oxide-semiconductor field-effect transistors (MOSFETs) were demonstrated. By inserting thin AlN interfacial layer (IL) at the oxide-semiconductor interface, the hysteresis in transfer characteristic was reduced and the channel mobility was improved to around 100 cm2/Vs. The interfacial layer was oxidized after post-deposition annealing (PDA) and disappeared. The results suggest the interfacial layer suppress the reaction at the AlSiO/GaN interface during PDA, resulting in reducing the border traps.

1:45 PM - 2:00 PM

[J-6-02] Suppression of GaO_x interlayer growth towards stable SiO_2/GaN MOS devices

○Kentaro Onishi[1], Takuma Kobayashi[1], Hidetoshi Mizobata[1], Mikito Nozaki[1], Akitaka Yoshigoe[2], Takayoshi Shimura[1], Heiji Watanabe[1] (1. Osaka Univ. (Japan), 2. JAEA (Japan))

Although a growth of GaOx interlayer at the SiO2/GaN interface improves the MOS interface properties, a recent study suggested that the GaOx interlayer is easily reduced during the annealing process, inducing positive fixed charge at the interface. In the present study, we formed SiO2 by sputter deposition to minimize the growth of unstable GaOx interlayer. With post-deposition annealing (PDA) at 800°C, SiO2/GaN MOS structure with a small C-V hysteresis was obtained. Furthermore, the negative shift of VFB during the annealing was suppressed, thanks to the minimization of GaOx interlayer formaiton.

2:00 PM - 2:15 PM

[J-6-03] Characterization of Trap States of SiO_2/GaN Interface and SiO_2 Layer by Deep Level Transient Spectroscopy

○Shingo Ogawa[1], Hidetoshi Mizobata[2], Takuma Kobayashi[2], Takayoshi Shimura[2], Heiji Watanabe[2]
(1. Toray Research Center (Japan), 2. Osaka Univ. (Japan))

The interface trap states and the oxide trap states of the SiO2/GaN MOS capacitors were investigated using DLTS. The energy distribution of the trap states were estimated and as a result, the dispersed oxide trap states at around 0.2 eV and 0.8 eV from the conduction band minimum of GaN were confirmed for the capacitor without the thermal annealing. The interface state density was proven to decrease to around 1e10 cm-2eV-1 by the thermal annealing.

2:15 PM - 2:30 PM

[J-6-04] High Quality Al_2O_3/SiC Gate Stack Fabricated by Microwave Plasma Annealing

○Nannan You[1,2], Xinyu Liu[1,2], Qian Zhang[1,2], Jiayi Wang[1], Yang Xu[1], Yu Wang[1,2], Shengkai Wang[1,2]
(1. Inst. of Beijing (China), 2. Univ. of Beijing (China))

The post deposition microwave plasma annealing (MPA) is developed to obtain high quality Al2O3/SiC gate stacks. By optimizing the plasma power, the in-terface state density is reduced by 1 order of magni-tude to 6 × 1011 cm-2eV-1, the breakdown electric field is increased, and the voltage shift is effectively sup-pressed. XPS results show the oxygen plasma enters the Al2O3 dielectric and fills the incomplete lattice during the MPA process, meanwhile, the interface has not been further oxidized.

2:30 PM - 2:45 PM

[J-6-05] Analysis of leakage current mechanisms in NO-nitrided SiC(1-100) MOS devices

○Asato Suzuki[1], Takato Nakanuma[1], Takuma Kobayashi[1], Mitsuru Sometani[2], Mitsuo Okamoto[2], Akitaka Yoshigoe[3], Takayoshi Shimura[1], Heiji Watanabe[1] (1. Osaka Univ. (Japan), 2. AIST (Japan), 3. JAEA (Japan))

Leakage characteristics of NO-nitrided SiC(1-100) MOS devices were investigated. From the current densi-ty-oxide field (Ig-EOX) characteristics at 25°C, we found that the nitridation at 1250°C reduces the conduction band offset (ΔEC) at the SiO2/SiC interface by about 0.3 eV, which was also confirmed by synchrotron radiation XPS (SR-XPS) measurements. The Ig-EOX characteristics near the onset of leakage were reproduced by considering Fowler-Nordheim (FN) and Poole-Frenkel (PF) currents for samples with various nitridation conditions over a wide measurement temperature (25 – 200°C).

2:45 PM - 3:00 PM

[J-6-06] 4H-SiC surface nitridation kinetic model in high temperature N_2 (+O_2) annealing focusing on the effects of annealing temperature and O_2 partial pressure

○Tianlin Yang[1], Koji Kita[1,2]
(1. Department of Materials Engineering, School of Engineering, Univ. of Tokyo (Japan), 2. Department of Advanced Materials Science, Graduate School of Frontier Sciences, Univ. of Tokyo (Japan))

An SiC surface nitridation kinetic model was build up
considering the reaction rates of N-incorporation (Nr) and N-removal (k). According to our model, the saturated surface N density (AN) is determined by the ratio Nr/k. Based on this model, the effects of the annealing temperature (T) and O2 partial pressure on the saturated AN for 4H-SiC(0001) were investigated for high-T N2 annealing systematically. Experimentally, the saturated AN was observed to increase with T but decrease with the O2 partial pressure, which is understandable by considering our model.

3:00 PM - 3:15 PM

[J-6-07] First-principles study on electronic structure at step edge of SiC/SiO_2 interface

○Kazuma Yokota[1], Mitsuharu Uemoto[1], Tomoya Ono[1] (1. Kobe Univ. (Japan))

We investigate electronic structures at the step edge of 4H-SiC/SiO2 interface by first-principles electronic-structure calculation. The local density of states and the spatial distribution of the charge density of the conduction band minimum (CBM) are investigated. It is found that the CBM at the upper terrace of the steps are significantly affected by the local atomic structure of the SiO2 side and the presence of the step edges.

3:15 PM - 3:30 PM

[J-6-08 (Late News)] Improvement of SiO_2/4H-SiC MOS Interface Characteristics via a Concentration-Tunable Boron Incorporation Process

○Runze Wang[1], Munetaka Noguchi[2], Hiroshi Watanabe[2], Koji Kita[1]
(1. The Univ. of Tokyo (Japan), 2. Mitsubishi Electric Corp. (Japan))

3:30 PM - 3:45 PM

[J-6-09 (Late News)] Theoretical Study of the Influence of GaO_x Layer on the SiO_2/GaN Interface

○Shuto Hattori[1], Atsushi Oshiyama[2], Seiichi Miyazaki[1], Heiji Watanabe[3], Katsunori Ueno[4], Ryo Tanaka[4], Tsurugi Kondo[4], Shinya Takashima[4], Masaharu Edo[4], Kenji Shiraishi[2,1]
(1. Graduate School of Eng., Nagoya Univ. (Japan), 2. IMaSS, Nagoya Univ. (Japan), 3. Graduate School of Eng., Osaka Univ. (Japan), 4. Fuji Electric Co., Ltd. (Japan))

Session information

Oral Presentation

03: Interconnect / 3D Integrations / MEMS

[K-4] Design, Process, and Technology for High-performance Chiplet II/3D Integration and Advanced Packaging II

Wed. Sep 28, 2022 9:00 AM - 10:15 AM 304 (3F)

Session Chair: Takeyasu Saito (Osaka Metropolitan Univ.), Xun Gu (ASM Japan)

9:00 AM - 9:30 AM

[K-4-01 (Invited)] Heterogenous Integration on Flexible Substrates

○Subramanian S. Iyer[1] (1. ULCA (United States of America))

9:30 AM - 9:45 AM

[K-4-02] Failure Analyses and Yield Enhancement of Electroplated Cu Direct Bonding for Heterogeneous 3D and Micro-LED Integration

○Yuki Susumago[1], Tadaaki Hoshi[1], Chang Liu[1], Atushi Shinoda[2], Hisashi Kino[3], Tetsu Tanaka[1,3], Takafumi Fukushima[1,3]
(1. Graduate School of Eng., Tohoku Univ. (Japan), 2. School of Eng., Tohoku Univ. (Japan), 3. Graduate School of Biomed. Eng., Tohoku Univ. (Japan))

This paper describes the electroplated Cu direct bonding technology for stacking micro-LEDs on 3D-ICs. Conventional bonding methods using thermal compression bonding with solder or conductive pastes for micro-LEDs have serious problems in fine-pitch interconnection and thermomechanical stress. This paper works on the failure analyses and challenges the yield enhancement of room-temperature micro-LED integration. The metallization yield is greatly improved nearly 100% by optimizing the electroplated Cu direct bonding processes. Finally, 900 pcs. of blue micro-LEDs with a side length of 0.1 mm are interconnected and successfully operated.

9:45 AM - 10:00 AM

[K-4-03] Surface Activated Bonding of ALD Al_2O_3 films

○Junsha Wang[1], Ryo Takigawa[2], Tadatomo Suga[1] (1. Meisei Univ. (Japan), 2. Kyushu Univ. (Japan))

Al2O3 films deposited on Si wafers by plasma enhanced atomic layer deposition (PEALD) were successfully bonded by surface activated bonding (SAB) at room temperature. Results show that Si wafers covered by different ALD Al2O3 films were bonded well without big voids. The increase of deposition plasma power promotes the crystallization of Al2O3, and the additional H2 plasma post-treatment changes the number of -OH on film surface. However, both methods failed to improve the bond strength of ALD Al2O3 films. The measurement atmosphere affects the bond strength of ALD Al2O3 films and sapphire/sapphire. The bond strength measured in air was smaller than that in vacuum and in N2. Under the same measured atmosphere, the bond strength of Al2O3 films was only slightly lower than that of sapphire/sapphire.

10:00 AM - 10:15 AM

[K-4-04] Modeling of Redistribution Layers and Through Glass Vias on Glass Interposers

Kai Zhao[1], ○Haitao He[1], Junchen Dong[1], Yudi Zhao[1] (1. Beijing Information Science and Technology University (China))

Analytical models of redistribution layers and through glass vias are proposed. Multi-channel effects including attack and victim lines are taken into account. The calculated S-parameters and eye diagrams are in good agreement with electromagnetic field simulation results.

Session information

Oral Presentation

12: Advanced Circuits / Systems Interacting with Innovative Devices and Materials

[K-5] Advanced Neuron and AI Systems

Wed. Sep 28, 2022 10:45 AM - 12:00 PM 304 (3F)

Session Chair: Takeshi Yoshida (Hiroshima Univ.), Yitao Ma (Tohoku Univ.)

10:45 AM - 11:15 AM

[K-5-01 (Invited)] Hiddenite: CNN Inference Accelerator for Randomly Weighted Neural Networks

〇Jaehoon Yu[1], Kazutoshi Hirose[1], Kota Ando[1], Yasuyuki Okoshi[1], Angel Lopez Garcia-Arias[1], Junnosuke Suzuki[1], Thiem Van Chu[1], Kazushi Kawamura[1], Masato Motomura[1] (1. Tokyo Ins. of Tech. (Japan))

11:15 AM - 11:30 AM

[K-5-02] A 1.2nJ/Classification 2.4mm^2 Wired-Logic Neuron Cell Array Using Logically Compressed Non-Linear Function Blocks in 0.18µm CMOS

〇Rei Sumikawa[1], Kota Shiba[1], Atsutake Kosuge[1], Mototsugu Hamada[1], Tadahiro Kuroda[1] (1. Univ. of Tokyo (Japan))

A 5.3 times smaller and 2.6 times more energy-efficient wired-logic processor which infers MNIST with 90.6% accuracy and 1.2nJ of energy consumption is developed. To improve area efficiency of wired-logic architecture, non-linear neural network (NNN), which is a neuron and synapse efficient network, and a logical compression technology which downsizes the circuit area of neurons are proposed. Since all of the neuron cell array is composed of combinational circuits, low voltage operation of 0.9V (half of the rated voltage in 0.18µm) is realized.

11:30 AM - 11:45 AM

[K-5-03] Neutron-induced stuck error bits and their recovery in DRAMs on GPU cards

〇Masanori Hashimoto[1], Yangchao Zhang[2], Kojiro Ito[2] (1. Kyoto Univ. (Japan), 2. Osaka Univ. (Japan))

Although soft error occurs randomly in neutron-irradiated DRAM, some bits repeatedly cause multiple errors during and even after neutron irradiation. Such a stuck bit error has been reported in the literature. This work conducted several error-checking experiments for DRAM on GPU cards to understand this phenomenon thoroughly. We observed stuck bit errors remaining for months. Also, we found that stuck block error could occur and revealed its temporal behavior of address shifting.

11:45 AM - 12:00 PM

[K-5-04] Design of an Energy-Efficient Nonvolatile Lookup Table Circuit Using Active-Load-Localized Circuitry with Self-Terminated Writing/Reading

〇Daisuke Suzuki[1], Takahiro Hanyu[2] (1. The University of Aizu (Japan), 2. Tohoku University (Japan))

An energy-efficient nonvolatile lookup table (LUT) circuit, where both write and read currents are automatically terminated if desired write/read operations are completed, is proposed. The use of self-terminated writing makes it possible to cut off wasted write current by continuously monitoring voltage transition due to the resistance change in the storage element. Moreover, wasted read current can also be cut off by utilizing voltage drop in active-load-localized circuitry as read completion signal. In fact, the proposed 6-input LUT circuit reduces 59% of write energy and 38% read energy with only 5% of hardware overhead compared to those of a conventional circuitry under 45nm CMOS technology.

Session information

Oral Presentation

03: Interconnect / 3D Integrations / MEMS

[K-6] MEMS and Advanced Metallization I

Wed. Sep 28, 2022 1:30 PM - 3:30 PM 304 (3F)

Session Chair: Shigeo Yasuhara (Japan Advanced Chemicals Ltd.), Kenji Shiojima (Univ. of Fukui)

1:30 PM - 2:00 PM

[K-6-01 (Invited)] Further Scaling Challenges and Opportunities

○Takashi Hayakawa[1] (1. TEL (Japan))

2:00 PM - 2:15 PM

[K-6-02] Evaluating Sintered Silver Die-attach Thermal Cycling Degradation by Nine Point Cycling Bending Test

○Keisuke Wakamoto[1,2], Takukazu Otsuka[1], Ken Nakahara[1], Takahiro Namazu[2]
(1. Rohm Co., Ltd (Japan), 2. Kyoto University of Advanced Science (Japan))

This paper investigates the nine-point bending test (NBT) evaluations for verifying the sintered silver (s-Ag) die degradation m during thermal shocked test (TST) that reflects practical operation in silicon carbide (SiC) power module products. SiC chip was s-Ag bonded at 300°C un-der a pressure of 60MPa with 64Titanium (64Ti) sub-strate. The assembly was flipped to place onto the eight rounded tip shape pin support jigs arranged in an octag-onal position. The other push pin was motion controlled under triangle wave form with the cycle period in 180 sec, force amplitude in 300N under 150°C. The scanning acoustic tomography (SAT) image was utilized for die de-lamination evaluation during NBT. The delamination was occurred after 400 cycles at the corner of chip, then progressed for in-plane direction. The delamination rate transition during NBT showed similar trends with that in TST up to 800 cycles. That is, mechanical stress plays a main role in the die degradation during TST.

2:15 PM - 2:30 PM

[K-6-03] Concentration Monitoring of H_2O_2 Based Slurry for Metal Chemical Mechanical Planarization (CMP) using Raman Spectroscopy

○Jinhyun Choe[1], Jinseok Kim[1], Dawon Ahn[1], Eunsu Jung[1], Sunggyu Pyo[1] (1. Chung-Ang University (Korea))

Raman spectroscopy is a non-destructive, highly sensitive, rapid analysis method that measures the degree of Raman scattering of light to detect a specific component and is easy to use for liquid phase analysis due to low water interference. In this study, the feasibility of quantitative concentration monitoring was shown using Raman spectroscopy to detect H2O2 in slurry for Copper Chemical Mechanical Planarization (CMP) process. Through Raman analysis of H2O2 based slurry, it was found that the degree of Raman scattering was linearly changed ac-cording to the concentration of H2O2 in the slurry solution, and the equation showed high linearity with an R^2 value of 0.99. This result indicates that quantitative concentration analysis of H2O2 based slurry is possible using Raman spectroscopy.

2:30 PM - 2:45 PM

[K-6-04 (Late News)] Growth of SiC Thin Film on Various Metal Substrates by CVD Using Vinylsilane

○Koki Ono[1], Takashi Koide[1], Yong Jin[2], Yuuki Tsutiizu[1], Takuhiro Hasegawa[1], Shigeo Yasuhara[2], Wakana Takeuchi[1]
(1. Aichi Institute Technology (Japan), 2. Japan Advanced Chemicals Ltd. (Japan))

2:45 PM - 3:00 PM

[K-6-05 (Late News)] Evaluation of Reactive Sputtered Ti-group MAX Alloy for Wiring Material

○Takeyasu Saito[1], Kazunobu WAKAMATSU[1], Kazuki UEDA[1], Naoki OKAMOTO[1] (1. Osaka Metropolitan Univ. (Japan))

3:00 PM - 3:15 PM

[K-6-06] 18nm pitch EUVL Line/Space double-patterning exploration for N3 BEOL

○Stephane LARIVIERE[1], Stefan DECOSTER[1], Sara PAOLILLO[1], Vincent RENAUD[1], Diana TSVETANOVA[1], Bart KENENS[1], Hanne DE COSTER[1], Quoc Toan LE[1], Yusuke ONIKI[1], Alfonso SEPULVEDA MARQUEZ[1], Karen STIERS[1], Felix SEIDEL[1], Martin O'TOOLE[1], Mircea DUSA[1], Kurt RONSE[1], Chris WILSON[1] (1. imec (Belgium))

At N3, metal interconnect logic Back End of Line (BEoL) wiring could not be Cu metallization anymore as resistance will dramatically increase due to the Critical Dimension (CD) downscaling. Many studies have identi-fied Ruthenium (Ru) as a relevant alternative metal, which, with a suitable hard mask (HM), can be directly patterned at that node in a dry etch scheme (Direct Metal Etch, aka DME). Waiting for 0.55 high-NA EUV single exposure availability, multi patterning schemes circum-vent the challenge of chip scaling down to 18 nm pitch (MP18) gratings.
In this work, we will present the development of a double patterning EUV flow for sub-20 nm L/S (line/Space) where the HM grating output is delivered to etch design-friendly variable metal CD lines with DME.

3:15 PM - 3:30 PM

[K-6-07] Demonstrating 1T1R Memory Cell by Heterogeneous Integration of Zinc Oxide Thin-Film Transistor with SiC-based Memristor

○Ben Daniel Rowlinson[1], Omesh Kapur[1], Dongkai Guo[1], Ruomeng Huang[1], C.H. de Groot[1], Harold Chong[1]
(1. University of Southampton (UK))

Wide-bandgap metal-oxide thin-film transistors are a promising technology for enabling future advances in heterogeneous integration, thanks to the phenomenally low leakage current, high mobility and excellent switching characteristics. In this work, we demonstrate a novel integration of an ultra-low leakage ZnO TFT with a high-endurance SiC memristor to form a single 1T1R (one transistor, one memristor) memory cell with high selectivity, low current leakage below 100 fA, and scalability to larger memory arrays.