2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

05: Photonics: Devices / Integration / Related Technology

[A-9] Imaging Sensors and Detectors

Thu. Sep 29, 2022 1:30 PM - 3:15 PM 101 (1F)

Session Chair: Mizuki Shirao (Mitsubishi Electric Corp.), Frederic Boeuf (STMicroelectronics)

1:30 PM - 1:45 PM

[A-9-01] Photonic Band Imaging using Hyperspectral NIRFIS

○Sho Okada[1], Tomohiro Amemiya[1,2], Hibiki Kagami[1], Yahui Wang[1], Nobuhiko Nishiyama[1,2], Xiao Hu[3]
(1. Tokyo Tech. (Japan), 2. IIR. (Japan), 3. WPI-MANA, NIMS (Japan))

We have proposed photonic band imaging based on hyperspectral near-infrared Fourier image spectroscopy. This method makes it possible to obtain mapping images that reflect structure-derived information determined by specified parameters within photonic bands.

1:45 PM - 2:00 PM

[A-9-02] Development of Test Element Group Methodology for Time-of-Flight CMOS Image sensor

○Jungwook Lim[1], Seunghyun Lee[1], Sungyoung Seo[1] (1. Samsung Electronics Co., Ltd. (Korea))

We developed and analyzed Test Element Group (TEG) module to model Full Well Capacity (FWC) and Dark Level (DL) of Indirect Time-of-Flight (iToF) pixel. To increase the depth accruacy of iToF sensor, high SNR is required and it is affected by FWC, DL, and so on. However, unlike the conventional Photodiode (PD) structure, it is difficult to estimate FWC and DL in iToF pixels because multiple devices including MOSCAP storage are connected in a chain structure. For this reason, a novel TEG suitable for this structure needs to be designed. In this paper, we analyzed FWC and DL of MOSCAP by measuring TEG module, which consists of electric potential, C-V curve, and charge pump.

2:00 PM - 2:15 PM

[A-9-03] Wide-range Si-based non-contact temperature sensor using single-photon avalanche diodes

○Yao Lun Liu[1], Sheng Di Lin[1], Chun Hsien Liu[1], Chun Hao Tsai[1], Ce Fang Shih[1], Jau Yang Wu[1], Chia Ming Tsai[1]
(1. Univ. of National Yang Ming Chiao Tung (Taiwan))

A wide-range non-contact temperature sensor using a 64x128 pixels SPAD array with tunable macro-pixel has been demonstrated. The detectable temperature, defined by noise-equivalent temperature difference less than 1°C, from 230 °C to 1050 °C has been achieved. This work reveals the high potential of SPADs for radiometric temperature measurement.

2:15 PM - 2:30 PM

[A-9-04] Investigation of Au-InGaAs Alloy for Plasmonic InGaAs Waveguide Photodetector

○Taketoshi Nakayama[1], Kasidit Toprasertpong[1], Shinichi Takagi[1], Mitsuru Takenaka[1] (1. Univ. of Tokyo (Japan))

Au-InGaAs, which is an alloy of Au and InGaAs, was evaluated for fabricating a plasmonic InGaAs waveguide photodetector (PD). Spectroscopic ellipsometry revealed that Au-InGaAs has a negative permittivity, similar to Au, enabling a surface plasmon polariton at the Au-InGaAs/InGaAs interface. Using the measured permittivity, we numerically confirmed the existence of the plasmonic mode in the Au-InGaAs/InGaAs/Au-InGaAs waveguide, revealing the feasibility of a plasmonic InGaAs waveguide PD using alloy formation.

2:30 PM - 2:45 PM

[A-9-05] Observation of Reversible Refractive Index Change of CMOS-Compatible Silicon Nitride Film

○Yuriko Maegami[1], Gangwei Cong[1], Morifumi Ohno[1], Toshihiro Narushima[1], Noritsugu Yamamoto[1], Hitoshi Kawashima[1], Koji Yamada[1]
(1. AIST (Japan))

We report a reversible refractive index change of a silicon nitride film deposited by plasma-enhanced chemical vapor deposition. The reversible change was observed in alternately processing of annealing and ultraviolet irradiation. The reversible index change has a potential to be applicable to non-volatile photon-ic interference circuits.

2:45 PM - 3:00 PM

[A-9-06] Novel Process Optimization for Higher SNR of Small Pixel Sized CMOS Image Sensor with FDTI Structure.

○Hyungeun Yoo[1], Junghyun Kim[1], Taesung Lee[1], Jonghoon Park[1], Yunki Lee[1], Bumsuk Kim[1], Jungchak Ahn[1]
(1. Samsung electronics Co., Ltd (Korea))

With increasing market demand of high resolution CMOS(Complementary Metal Oxide Semiconductor) image sensors, its unit pixel size has dramatically de-creased over the years. Therefore, Number of pho-tons entering unit pixel on an integration time have been decreased as unit pixel size decreases inevitably resulting in lower sensitivity of each pixel. Various technologies to increase the sensitivity have been researched and applied in recent image sensors with small sized pixel. In this paper, we introduce optimization method for higher sensitivity in CMOS image sensor and inevitable side ef-fects are successfully reduced.

3:00 PM - 3:15 PM

[A-9-07] Fabrication of 3 µm Pixel Pitch InGaAs Photodiodes using Be Implantation Doping for SWIR sensing

○Jules Tillement[1,2,3], Cyril Cervera[2], Jacques Baylet[2], Olivier Gravrand[2], Quentin Lalauze[2], Christophe Jany[2], Thomas Di Rito[2], Olivier Saxod[2], Norbert Moussy[2], Thierry Baron[3], Francois Roy[1], Frederic Boeuf[1]
(1. STMicroelectronics (France), 2. Universite Grenoble Alpes, CEA Leti (France), 3. Universite Grenoble Alpes CNRS, LTM (France))

In this work, we present a process of InGaAs photodiode manufacturing with Be implantation as the p-type doping method. We show successful realization of photodiodes arrays by spectral response for pixel pitch ranging from 15µm to 3µm, which is the lowest published pixel pitch to date for InGaAs photodetectors. The measured dark current density for our best case presented here is 10-6 A.cm-2 at -0.2V at 300K. Be profile and defects density after activation anneal are discussed as potential leads for further optimization.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

05: Photonics: Devices / Integration / Related Technology

[A-10] Integrated Photonic Devices

Thu. Sep 29, 2022 4:00 PM - 6:00 PM 101 (1F)

Session Chair: Keijiro Suzuki (AIST), Karim Hassan (CEA-LETI)

4:00 PM - 4:15 PM

[A-10-01] Demonstration of an Efficient Light Coupler to a Valley Photonic Crystal Waveguide Formed at a Bearded Interface

○Hironobu Yoshimi[1,2], Takuto Yamaguchi[1,2], Satomi Ishida[1,2], Yasutomo Ota[3,4], Satoshi Iwamoto[1,2,4]
(1. RCAST, The Univ. of Tokyo (Japan), 2. IIS, The Univ. of Tokyo (Japan), 3. Keio Univ. (Japan), 4. NanoQuine, The Univ. of Tokyo (Japan))

We demonstrate an efficient light coupler between a valley photonic crystal waveguide formed at a bearded interface and a wire waveguide. Numerically calculated coupling loss is less than 1 dB/coupler. We fabricated the couplers in a Si slab and experimentally observed a low coupling loss of 1.1 dB/coupler. These results will lay ground work for low-loss photonic circuits with topological waveguides.

4:15 PM - 4:30 PM

[A-10-02] Optical Unitary Conversion of Multi-Wavelength Dual-Polarization Channels using Integrated Multi-Plane Light Converter

○Ryota Tanomura[1], Takuo Tanemura[1], Yoshiaki Nakano[1] (1. Univ. of Tokyo (Japan))

Integrated optical unitary converter (OUC) is re-ceiving a great interest for optical communication, quantum computing, and deep learning applications. Previously demonstrated OUCs assume a fixed wave-length and a polarization state at the input. In this paper, we demonstrate that the multi-plane light conversion (MPLC)-based OUC with multiport directional couplers (DCs) can provide arbitrary and independent unitary conversions to dual-polarization multiple-wavelength channels at the same time. This is due to the inherent flexibility of the MPLC concept as well as strong polari-zation/wavelength dependence of a silicon-photonic mul-tiport DC.

4:30 PM - 4:45 PM

[A-10-03] Polarization-Independent Enhancement of Optical Absorption in a GaAs Quantum Well Embedded in an Air-bridge Bull's-eye Cavity

○Sangmin Ji[1], Takeyoshi Tajiri[2], Xiao-Fei Liu[3], Haruki Kiyama[3,4], Akira Oiwa[3], Julian Ritzmann[5], Arne Ludwig[5], Andreas Dirk Wieck[5], Satoshi Iwamoto[1]
(1. The Univ. of Tokyo (Japan), 2. Univ. of Electro-Communications (Japan), 3. Osaka Univ. (Japan), 4. Kyushu Univ. (Japan), 5. Ruhr-Universität Bochum (Germany))

Bull's-eye structures containing optically active media provide an attractive platform for implementing efficient photonic quantum interfaces. By exploiting their symmetric nature, we previously designed a bull's-eye optical cavity that enhances the optical absorption without polarization dependence, which can be applied to an efficient photon–spin converter using a gate-defined quantum dot (GQD). In this correspondence, we experimentally demonstrate that our bull's-eye cavity can enhance the optical absorption of a quantum well (QW) without polarization dependence. Photoluminescence excitation spectra from the fabricated cavities show the maximum 12-times enhancement of QW absorption. The enhancement is almost identical for orthogonal polarizations.

4:45 PM - 5:00 PM

[A-10-04] Compact, Low-loss, Fabrication-tolerant, and Thermally Stable 2x2 Si Optical Coupler Designed by CMA-ES

○Yuto Miyatake[1], Kasidit Toprasertpong[1], Shinichi Takagi[1], Mitsuru Takenaka[1] (1. Univ. of Tokyo (Japan))

In this paper, we propose a 2x2 optical coupler on a Si photonic platform designed using a covariance matrix adaptation evolution strategy (CMA-ES). The optimized 2x2 coupler has a small footprint (1.5 um x 10 um), low excess loss (less than 0.03 dB), and much better fabrication tolerance and thermal stability than conventional ones. These features make the proposed coupler promising for a building block of large-scale photonic integrated circuits.

5:00 PM - 5:30 PM

[A-10-05] Analog photonic computing for Deep Neural Network Application

○Nikos Pleros[1] (1. Aristotle Univ. of Thessaloniki (Greece))

5:30 PM - 5:45 PM

[A-10-06] Experimental Demonstration of a Novel Self-adaptive Photonic Tensor Core on the SOI Platform with Noise Suppression towards High Precision and Computational Efficiency

○Rui Shao[1], Gong Zhang[1], Xuanqi Chen[1], Haibo Wang[1], Yue Chen[1], Yuxuan Wang[1], Xiao Gong[1]
(1. National Univ. of Singapore (Singapore))

We report the first self-adaptive photonic tensor core employing noise suppressing structures using cascaded programmable Mach-Zehnder modulators (MZMs) on the standard 220 nm SOI photonic platform. We take advantage of the waveguide crossing structures to help achieve a significant reduction of errors when the number of MZMs raises. We further propose and utilize the self-adaptive mechanism to realize a ±0.5 dB dynamic control. By using our self-adaptive photonic tensor core to realize the deep convolution neural network (DCNN) with 15 convolutional layers, we demonstrate the lowest accuracy degradation (~0.2%) with high computational efficiency (~333 FLOP/W) among reported silicon photonic hardware.

5:45 PM - 6:00 PM

[A-10-07] Modulation of C-band III-V/Si hybrid Lasers for FMCW LiDAR Applications

○Josserand GAUDY[1,2,3], Cédric Rostaing[2], Christophe Jany[2], Karim Hassan[2], Frédéric Boeuf[1], Jean-Emmanuel Broquin[3]
(1. ST Microelectronics Crolles (France), 2. CEA-Leti, Univ. Grenoble Alpes (France), 3. Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LaHC (France))

We present the work done on III-V/Si bonded Lasers
to use them for FMCW. The Lasers are suitable for a
proof of concept of thermo-optic FMCW.

2022 International Conference on
ssdm Solid State Devices and Materials
2022 September 26-29, 2022

Session information

Oral Presentation

11: Advanced Materials: Synthesis / Crystal Growth / Characterization

[B-8] Group IV Materials II

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 102 (1F)

Session Chair: Kentaro Watanabe (Shinshu Univ.), Tomohiro Yamaguchi (Kogakuin Univ.)

10:45 AM - 11:15 AM

[B-8-01] Layer exchange of group IV materials: crystal growth and device applications

○Kaoru Toko[1] (1. Univ. of Tsukuba (Japan))

11:15 AM - 11:30 AM

[B-8-02] Evaluation of Chemical Structure and Si Segregation of Al/Si(111)

○Taiki Sakai[1], Akio Ohta[1], Keigo Matsushita[1], Noriyuki Taoka[1], Katsunori Makihara[1], Seiichi Miyazaki[1]
(1. Nagoya University (Japan))

Controls of diffusion and segregation of Si atoms through a thin metal layer from stacked Si structure is one of the effective techniques to grow two dimensional (2D) or ultrathin Si crystals. In this study, an 30 nm-thick Al layer was formed on Si(111) substrate as a crystalline growth template of segregated Si atoms. Si segregation on Al(111) surface with keeping surface flatness was demonstrated by post annealing in N2 ambient at temperature below 500 ºC.

11:30 AM - 11:45 AM

[B-8-03] Improved Carrier Mobility of Sn-Doped Ge Ultrathin (<50) Films on Insulator by a-Si Capping in Solid-Phase Crystallization

○Takaya Nagano[1], Ryutaro Hara[1], Kenta Moto[1], Keisuke Yamamoto[1], Taizoh Sadoh[1] (1. Univ. of Kyushu (Japan))

Thin poly-Ge films (thickness: below 50 nm) having high carrier mobility are required for advanced thin-film devices. However, carrier mobility of poly-Ge films obtained by conventional solid-phase crystallization (SPC) significantly decreases with decreasing thickness below 50 nm. To solve this problem, we develop an interface-modulated SPC of Sn-doped Ge combined with a-Si capping. In the present study, we investigate growth characteristics of a-Si capped Sn-doped Ge films on insulator. It is clarified that a-Si capping enhances SPC of Sn-doped Ge films and results in large crystal grains, which improves the carrier mobility of Sn-doped Ge thin films. This technique will be useful to realize advanced thin-film devices for next-generation electronics.

11:45 AM - 12:00 PM

[B-8-04] Ultrathin Large Grain Si Films on Insulator by Solid-Phase Crystallization Combined with Sn-Doping

○kota - okamoto[1] (1. kyushu university (Japan))

2022 International Conference on
ssdm 2022 Solid State Devices and Materials
September 26-29, 2022

Session information

Oral Presentation

09: Novel Functional / Quantum / Spintronic Devices and Materials

[C-8] Spintronics 1

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 103 (1F)

Session Chair: Shinobu Ohya (Univ. of Tokyo), Hiromasa Shimizu (Tokyo Univ. of Agriculture and Technology)

10:45 AM - 11:15 AM

[C-8-01] Ferrimagnetic Spintronics

○Kyung-Jin Lee[1] (1. KAIST (Korea))

11:15 AM - 11:30 AM

[C-8-02] Magnetic anisotropy of *n-type* ferromagnetic semiconductor (In, Fe)Sb studied by ferromagnetic resonance: Control by epitaxial strain

○Akhil Sanjaya Kumar Pillai[1], Shobhit Goel[1], Le Duc Anh[1,2,3], Masaaki Tanaka[1,3]
(1. Univ. of Tokyo (Japan), 2. PRESTO (Japan), 3. CSRN (Japan))

We report the first comprehensive study on the magnetic anisotropy of n-type ferromagnetic semiconductor (FMS) (In,Fe)Sb grown on different buffer layers (InSb, AlSb, GaSb, InAs), using ferromagnetic resonance studies. When the epitaxial strain induced in (In,Fe)Sb is changed from tensile to compressive, we see a change in the values of magneto-crystalline anisotropy constant, favoring perpendicular magnetization. However, due to strong shape anisotropy, effective magnetization is still of in-plane nature. This work suggests the ability to control magnetic anisotropy in (In,Fe)Sb using strain.

11:30 AM - 11:45 AM

[C-8-03] Generation of spin-polarized electrons in n^+-Si by spin injection through a ferromagnetic tunnel junction: Role of the band diagram

○Baisen Yu[1], Shoichi Sato[1,2], Masaaki Tanaka[1,2], Ryosho Nakane[1] (1. Univ. of Tokyo (Japan), 2. CSRN (Japan))

We studied electron spin polarization in the n+-Si channel of a lateral spin device having Fe-based ferromagnetic tunnel junctions for source and drain electrodes, from both experimentally and theoretically. We proposed an original spin transport model for spin injection/detection polarization (Pinj/ Pdet) by taking into account the band diagram of the ferromagnetic tunnel junction. We demonstrated that our model can explain all the experimental Pinj and Pdet in a wide range of the junction voltage drop. Main findings are as follows: (1) Pinj and Pdet simply originate from the band diagram of the ferromagnetic tunnel junction, namely, spin filtering in the tunnel barrier is not necessary. (2) Pdet is closely related to the electron density near the Si surface facing the tunnel barrier. Our model provides a deep insight into the spin-related physics in Si-based magnetic tunnel junctions.

11:45 AM - 12:00 PM

[C-8-04] Bias voltage and temperature dependence of electron-spin polarization in InAs quantum dots tunnel-coupled with a GaNAs quantum well

SOYOUNG PARK[1], ○HIROTO KISE[1], SATOSHI HIURA[1], JUNICHI TAKAYAMA[1], KAZUHISA SUEOKA[1], AKIHIRO MURAYAMA[1]
(1. Hokkaido Univ. (Japan))

Bias voltage and temperature dependence of electron-spin polarization in InAs quantum dots (QDs) tunnel-coupled with a GaNAs quantum well have been investigated. The state filling effect in QDs becomes suppressed with increasing temperature because of the thermal excitation and thermal escape of
electron spins, leading to the enhanced circular polarization degree of QD luminescence. We also observe a large difference in the electron-spin polarization at QD excited states by changing the applied bias voltage at higher temperature of 260 K. The high spin polarization can be attributed to the thermally activated spin filtering in a GaNAs quantum well.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

06: Photovoltaic / Energy Harvesting / Battery-related Technology

[C-9] Thermoelectric Devices

Thu. Sep 29, 2022 1:30 PM - 3:30 PM 103 (1F)

Session Chair: Shinya Kato (Naogya Inst. of Technology), Takuya Hoshii (Tokyo Tech)

1:30 PM - 2:00 PM

[C-9-01] Composite Effects on Thermoelectric Properties: A New Design of Practical Thermoelectric Generators

○Tsunehiro Takeuchi[1] (1. Toyota technological Inst. (Japan))

2:00 PM - 2:15 PM

[C-9-02] " Experimental Demonstration of The Cavity-Free GeSn and Si Wire Thermoelectric Generators "

○MD Mehdee Hasan Mahfuz[1], Motohiro Tomita[1], Kazuaki Katayama[1], Ito Yoshitsune[2], Kazuaki Fujimoto[2], Takanobu Watanabe[1], Kurosawa Masashi[2], Takeo Matsuki[3]
(1. Waseda Univ. (Japan), 2. Nagoya Univ. (Japan), 3. National Inst. of Advanced Indus. Sci. and Tech. (Japan))

This work demonstrates the thermoelectric (TE) performance of the cavity-free thermoelectric generators (TEGs) using GeSn and Si wires. In the Cavity-free structure, one side of the TEG is heated and the back of the substrate is cooled. Thus, the heat energy flows mainly in the vertical direction but also exudes horizontally. This horizontal heat flow forms a steep temperature gradient in the wires, which is ranged hundreds of nm. In this work, with the identical patterning design, the Seebeck coefficient, power-factor and TE performance of the generators were characterized. The obtained results were then used to compare the TEGs which prefer the superiority of the GeSn-TEG over the Si-TEG.

2:15 PM - 2:30 PM

[C-9-03] Experimental Demonstration of Spreading Resistance Effect in A Miniatrized Bileg Thermoelectric Generator

○Motohiro Tomita[1], Tsubasa Kashizaki[1], Takumi Hoshina[1], Shuhei Arai[1], Takeo Matsuki[1,2], Takanobu Watanabe[1]
(1. Waseda Univ. (Japan), 2. AIST (Japan))

The effect of the spreading resistance on the bileg thermoelectric generator (TEG) was experimentally evaluated. In the bileg-TEG at the μm-scale, the electrical resistance becomes larger than a simple estimate using lumped parameter circuit model, which is caused by the spreading resistance; when a current flows from a narrower leg to a wider leg. Thus, the width of the p- and n-type legs in the bileg-TEG at the μm-scale should be carefully selected.

2:30 PM - 2:45 PM

[C-9-04] Impact of grain-boundary on thermal conductivity in environmentally friendly thermoelectric sulphide Cu_2ZnSnS_4

○Katsuma Nagatomo[1], Akira Nagaoka[1], Kouichi Okamoto[1], Kenji Yoshino[1], Kensuke Nishioka[1] (1. University of Miyazaki (Japan))

Cu2ZnSnS4 (CZTS) single crystal is a high-performance thermoelectric material while using environmentally friendly materials, and its ZT shows 1.6 at 800K. In this study, we investigated the impact of grain-boundary on thermal conductivity in CZTS by the combination of experimental and theoretical results. It was confirmed that the value of thermal conductivity with 0.1 μm grain was 0.9 at 800 K, which is almost the half value of single crystal.

2:45 PM - 3:00 PM

[C-9-05] Thermoelectric characterization of multinary compound $(Cu_{1-x}Ag_x)_2ZnSnS_4$

○Kouichi Okamoto[1], Akira Nagaoka[1], Katsuma Nagatomo[1], Kenji Yoshino[1], Kensuke Nishioka[1] (1. Univ. of Miyazaki (Japan))

Cu2ZnSnS4 (CZTS), a quaternary material with a kesterite structure, is one of the thermoelectric materials with high performance. In this study, we investigated the crystal growth, thermoelectric properties and electrical properties of n-type (Cu1-xAgx)2ZnSnS4 (CAZTS) by substituting Ag for CZTS. The Seebeck coefficient of CAZTS (x = 0.1-0.5) at 373-723 K was a negative value of ~100 μV/K at x = 0.4, confirming a conduction type. Similarly, the Hall coefficient was negative value with the carrier concentration of 10^16 /cm^3.

3:00 PM - 3:15 PM

[C-9-06] Design of Planar-type Thermoelectric Generator with Polycrystalline Silicon Thin Film

○Ryoto Yanagisawa[1], Masahiro Nomura[1] (1. Univ. of Tokyo (Japan))

We simulated the performance of a planar-type thermoelectric generator with different thicknesses of silicon thin-film device layer. We introduced a variety of thermal conductivity depending on the thickness of silicon thin-film for both single-crystalline and polycrystalline in the simulation and found optimal dimensions of device design. We clarified that different dependence on thick-ness for thermal conductivity between single- and poly-crystalline silicon leads to a different optimal thickness of silicon device layer.

3:15 PM - 3:30 PM

[C-9-07] Grain Shape Dependence of Thermal Conductivity of Silicon Polycrystalline Nanostructure

○Riku Tomabechi[1], Ryusei Taniguchi[1], Takuma Hori[1] (1. Tokyo Univ. of Agriculture and Tech. (Japan))

Thermoelectric device can convert thermal energy into electrical one. Decreasing thermal conductivity of the material is theoretically known to be necessary for improving the conversion efficiency. Nanostructuring of materials can impede lattice vibration (phonon) transport and thus it is effective for decreasing thermal conductivity of semiconductors. In this study, the influence of grain shape of polycrystalline nanostructure on its thermal conductivity is evaluated by numerical analysis. Our phonon transport simulations reveal that the mean free path of phonons in nanostructures of uniform grain shape has correlation with ratio of the grain volume to its surface area. This tendency is reasonable since scattering frequency between phonons and grain boundaries decreases with smaller surface area.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

09: Novel Functional / Quantum / Spintronic Devices and Materials

[C-10] Spintronics 2

Thu. Sep 29, 2022 4:00 PM - 5:30 PM 103 (1F)

Session Chair: Ken-ichi Aoshima (NHK STRL), Ken Morita (Chiba Univ.)

4:00 PM - 4:15 PM

[C-10-01] Operating characteristics of domain walls in perpendicular magnetized ferrimagnetic nano-pillar for three-dimensional magnetic memory

○Yuichiro Kurokawa[1], Hiromi Yuasa[1] (1. Kyushu University (Japan))

4:15 PM - 4:30 PM

[C-10-02] Superconducting Diode Effect in Ferromagnet-inserted Noncentrosymmetric Superconducting Multilayers

○Hideki Narita[1], Jun Ishizuka[2], Ryo Kawarazki[1], Daisuke Kan[1,3], Yoichi Shiota[1,3], Takahiro Moriyama[1,3], Yuichi Shimakawa[1,3], Ognev V. Alexey[4], Samardak S. Alexander[4], Youichi Yanase[5,6], Teruo Ono[1,3,4,7]
(1. ICR, Kyoto Univ. (Japan), 2. ETH Zurich (Switzerland), 3. CSRN, Kyoto Univ. (Japan), 4. Far Eastern Federal Univ. (Russia), 5. Dept. of Phys. , Kyoto Univ. (Japan), 6. IMS (Japan), 7. CSRN, Osaka Univ. (Japan))

The diode effect in superconductors, called the superconducting diode effect (SDE), implies a superconducting state in one direction and a normal-conducting state in the other direction. Recently, the SDE has been discovered in the Nb/V/Ta superlattice with a polar structure. However, the SDE requires an external magnetic field, which limits its practical application. We present an SDE in a zero-field using noncentrosymmetric [Nb/V/Co/V/Ta]20 multilayers. The polarity of the SDE is controlled by the magnetization direction of the ferromagnetic layer. These findings enable the development of novel non-volatile memories and logic circuits with ultralow power consumption using such SDEs.

4:30 PM - 4:45 PM

[C-10-03] THz Ferrimagnetic Oscillation Based on the Atomistic Model

○Xue Zhang[1], Baofang Cai[2], Jie Ren[1], Zhengping Yuan[1], Yumeng Yang[1], Gengchiau Liang[2], Zhifeng Zhu[1]
(1. Univ.of ShanghaiTech (China), 2. National Univ.of Singapore (Singapore))

The magnetization oscillation of ferrimagnets, (FeCo)1-xGdx, driven by the spin transfer torque is studied using the two-dimensional atomistic model. Two oscillation modes are observed, i.e., the exchange mode and the flipped exchange mode, where the former only exists at small Gd composition. The frequency ranges from 300 GHz to 4.3 THz, and it can be controlled in a wide current range from 3×10^11 A/m^2 to 1.9×10^12 A/m^2. The high frequency is mainly occurred in the flipped exchange mode. The frequency increases when the Gd composition is increased. A spatial nonuniform oscillation is also observed when the sample is small. The effect of the Gd composition and the sample size cannot be captured using the macrospin model. Our study helps to understand the THz oscillation generated in ferrimagnets.

4:45 PM - 5:00 PM

[C-10-04] Investigation of Multileveled Spin Orbit Torque Magnetization Switching for High Density Magnetic Memory

○uraku kamihoki[1], Yuichiro Kurokawa[1], Masahiro Fujimoto[1], Masahiro Itoh[1], Hiromi Yuasa[1] (1. Kyushu Univ. (Japan))

5:00 PM - 5:15 PM

[C-10-05] Impact of Grain Boundaries in MgO Layer on Data Retention Performance of STT-MRAM

○Keisuke Morishita[1], Yosuke Harashima[2], Masaaki Araidai[1,3], Tetsuo Endoh[4,5,6], Kenji Shiraishi[1,3,4]
(1. Univ. of Nagoya (Japan), 2. NAIST (Japan), 3. Inst. of Materials and Systems for Sustainablity (Japan), 4. Center for Innovative Intergrated Electronic Systems (Japan), 5. Univ. of Tohoku (Japan), 6. Research Inst. Electrical Communiaction (Japan))

We have theoretically investigated the influence of grain boundary in MgO layer for data retention in STT-MRAM. We have found that grain boundary decreases interfacial perpendicular magnetic anisotropy based on the first principles calculations.
This is because the peak of minority spin d_xz/d_yz DOS decreased near fermi energy by the existence of grain boundary.

5:15 PM - 5:30 PM

[C-10-06 (Late News)] Highly Efficient Spin Current Source Using BiSb Topological Insulator / NiO Bilayers

○Julian Sasaki[1], Shigeki Takahashi[2], Yoshiyuki Hirayama[2], Pham Nam Hai[1]
(1. Tokyo Institute of Technology (Japan), 2. Samsung R&D Institute Japan (Japan))

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

07: Organic / Molecular / Bio-electronics

[D-8] Optoelectronics and thermoelectronic devices

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 104 (1F)

Session Chair: Hiroaki Iino (Tokyo Tech), Masaki Murata (Sony Semiconductor Solutions Corp.)

10:45 AM - 11:00 AM

[D-8-01] Study of Near-infrared Organic Photodetectors with Octa-substituted Alkyl and Alkoxy Phthalocyanine Derivatives

○Shahriar Kabir[1], Yukiko Takayashiki[1], Jun-ichi Hanna[1], Hiroaki Iino[1] (1. Tokyo Tech. (Japan))

In this study, near-infrared photodetectors with octa-substituted alkyl and alkoxy phthalocyanine derivatives were realized and compared. The photodetectors were prepared with a bulk heterojunction active layer where each of the phthalocyanine derivatives acted as the donor and phe-nyl-C61-butyric-acid-methyl-ester (PCBM) acted as the acceptor. By varying the blend ratio of the donor and acceptor materials, the photo current output was improved and maximum responsivity of 0.7 A/W and 0.0092 A/W were achieved for the alkyl phthalocyanine:PCBM and alkoxy phthalocyanine:PCBM devices, respectively, at 740 nm with -1 V bias. The superior performance was attributed to the better intermixed condition of the bulk heterojunction active layer due to the weak intermolecular interactions of the alkyl phthalocyanine material. High responsivity of the demonstrated organic photodetector makes it suitable for practical applications.

11:00 AM - 11:15 AM

[D-8-02] Improved Operational Stability of Perovskite Solar Cells at High Temperature

○Yuki Fujita[1], Ganbaatar Tumen Ulzii[2], Toshinori Matsushima[1], Chihaya Adachi[1]
(1. Univ. of Kyushu (Japan), 2. Univ. of Cambridge (UK))

Metal halide hybrid perovskites are promising be-cause of the efficient harvesting of solar energy into electricity. However, the degradation of perovskite solar cells (PSCs), especially at high temperature, is still problematic for future commercialization. In this study, we show that volatilization of 4-tert-butylpyridine (4-tBP) from an organic hole transport layer is the main degradation mechanism of PSCs at high temperature. We demonstrate that this 4-tBP volatilization can be suppressed by covering PSCs with a fluoro-polymer CYTOP layer, greatly improving the high-temperature stability of PSCs.

11:15 AM - 11:30 AM

[D-8-03] Lasing and optical waveguide characteristics in one-dimensional crystals of thiophene/phenylene co-oligomers

○Takumi Matsuo[1,2], Shotaro Hayashi[1], Fumio Sasaki[2], Hisao Yanagi[3]
(1. School of Environmental Sci. and Eng., Kochi Univ. of Tech. (Japan), 2. Res. Inst. for Advanced Electronics and Photonics (RIAEP), National Inst. of Advanced Indus. Sci. and Tech. (AIST) (Japan), 3. Graduate School of Sci. and Tech., Nara Inst. of Sci. and Tech. (NAIST) (Japan))

One-dimensional (1D) organic microstructures are important for lasers, optical waveguides, and photonic circuits. Among various organic compounds, thiophene/phenylene co-oligomers (TPCOs) are promising materials as laser media in single crystal state owing to their high photoluminescence (PL) quantum efficiency, robustness, and high carrier mobilities. However, their potentials for transporting photons are still unrevealed.
We report here the characterization of lasing behaviors in 1D TPCO crystals along with their optical waveguide characteristics. As the target materials, a series of TPCOs, 2,5-bis(4′-cyanobiphenyl-4-yl)thiophene (BP1T-CN) and 5,5′-bis(4′-cyano-biphenyl-4-yl)-2,2′-bithiophene (BP2T-CN) are obtained in solution phase. Apart from the lasing in the naturally formed crystal edges, the low values of attenuation coefficient estimated through the spatially-resolved PL measurements suggest that the obtained 1D TPCOs are superior materials for photonic applications.

11:30 AM - 11:45 AM

[D-8-04] Excited-state quenching and laser properties of 1-naphthylmethylamine-based quasi-2D perovskite films

○Ryotaro Nasu[1,2,3], Chathuranganie A. M. Senevirathne[3], Toshinori Matsushima[2], Chihaya Adachi[2,3]
(1. Dept. Appl. Chem., Kyushu University (Japan), 2. International Institute for Carbon-Neutral Energy Research (WPI-I2CNER) (Japan), 3. Center for Organic Photonics and Electronics Research (OPERA) (Japan))

A metal halide perovskite (MHP) film is an excellent gain medium for optically pumped lasing. Although high hole and electron mobilities of MHP films would be useful for realizing electrically pumped laser devices, in which high current operation is required, electrical las-ing has never been demonstrated. For future electrical lasing, in this study, we investigated excited-state quenching and lasing behaviors of 1-naphthylmethlamine (NMA)-based MHP films. We found that NMA-based MHP films have less excit-ed-state quenching and, therefore, exhibit a relatively low laser threshold under optical pumping.

11:45 AM - 12:00 PM

[D-8-05] Mechanism of N-type doping of CNT yarn using tetrabutylammonium halide (TBAX, X= Cl, Br, and I) for efficient flexible thermoelectric generators.

○Aghnia Dinan Maulani Heriyanto[1], Yongyoon Cho[1], Naofumi Okamoto[1], Ryo Abe[1], Manish Pandey[1], Hiroaki Benten[1], Masakazu Nakamura[1] (1. Nara Institute of Science and technology (NAIST) (Japan))

Carbon nanotubes (CNTs) are a promising candidate for thermoelectric (TE) materials owing to their excellent electrical and mechanical properties. By doping the CNT, it is possible to control the carrier concentration, which can modulate the Seebeck coefficient and electrical conductivity which are strongly dependent upon each other. In this work, a series of halide dopants to obtain flexible n-type CNT-based TE CNT yarn are reported. By using tetrabutylammonium halide (TBAX, X= Cl, Br, or I) of which introduction is confirmed by Electron Probe Microanalyzer (EPMA), CNTs are successfully doped to n-type keeping Seebeck coefficient and enhancing electrical conductivity. The optimal n-type CNT yarn was found in TBAI/CNT composition, showing a power factor of 351.15 μW/mK2. This work sheds light on the interaction between organic halide compound and CNT to improve the TE performance

Session information

Oral Presentation

03: Interconnect / 3D Integrations / MEMS

[E-7] MEMS and Advanced Metallization II

Thu. Sep 29, 2022 9:00 AM - 10:45 AM 105 (1F)

Session Chair: Akinobu Yamaguchi (Univ. of Hyogo), Takeo Minari (NIMS)

9:00 AM - 9:30 AM

[E-7-01 (Invited)] TBD

○Tadashi Inoue[1] (1. MMI Semiconductor Co., Ltd. (Japan))

9:30 AM - 9:45 AM

[E-7-02] Fabrication and Characterization of Through-X Via (TXV) for Smart Skin Display

○Tadaaki Hoshi[1], Yuki Susumago[1], Liu Chang[1], Atsushi Shinoda[2], Hisashi Kino[3], Tetsu Tanaka[1,3], Takafumi Fukushima[1,3]
(1. Dept. of Mechanical Systems Engineering, Graduate School of Engineering, Univ. of Tohoku (Japan), 2. Dept. of Mechanical and Aerospace Engineering, School of Engineering, Univ of Tohoku (Japan), 3. Dept. of Biomedical Engineering, Graduate School of Biomedical Engineering, Univ. of Tohoku (Japan))

9:45 AM - 10:00 AM

[E-7-03] Piezoresistive Strain Sensors Based On Gold Nanoparticle Deposits On PDMS Substrates For Highly Sensitive Human Pulse Sensing

○Wei-Rong Yang[1], Yu-Shun Su[1], Jenn-Ming Song[1], Watson Kuo[1], Shien-Der Tzeng[2], Kiyokazu Yasuda[3]
(1. National Chung Hsing University (Taiwan), 2. National Dong Hwa University (Taiwan), 3. Osaka University (Japan))

In this study, highly-sensitive piezoresistive strain sen-sors based on gold nanoparticle thin films deposited on a stretchable PDMS substrate by centrifugation were de-veloped to measure arterial pulse waveform. The gauge factors of nanoparticle thin film sensors can be opti-mized up to 419 in tensile mode and 260 in compressive mode. It has been demonstrated that nanoparticle thin film sensors on PDMS substrates were successfully ap-plied to sense arterial pulses at human body.

10:00 AM - 10:15 AM

[E-7-04 (Late News)] Study on Microfluidic analysis system with molecular sensing based on Surface-enhanced Raman Scattering

○Akinobu Yamaguchi[1], Taku Tanaka[1], Shunya Saegusa[1], Masayuki Naya[2,1], Takao Fukuoka[3], Sho Amano[1], Yuichi Utsumi[1]
(1. Univ. of Hyogo (Japan), 2. Keio Univ. (Japan), 3. Kyoto Univ. (Japan))

10:15 AM - 10:30 AM

[E-7-05 (Late News)] Assessment for Moisture Resistance Reliability of Graphene-Capped Copper Structures by Spectroscopic Ellipsometry

○Shun Nakajima[1], Yoko Wasai[2], Kenji Kawahara[3], Nataliya Nabatova-Gabain[2], Hiroki Ago[3], Hiroyuki Akinaga[4], Kazuyoshi Ueno[1]
(1. Shibaura Inst. Tech. (Japan), 2. Horiba Techno Service Co. Ltd. (Japan), 3. Kyushu Univ. (Japan), 4. Nat. Inst. Adv. Indus. Sci. Tech. (Japan))

10:30 AM - 10:45 AM

[E-7-06 (Late News)] Control of Surface Oxidation and Stress by Additives in Ni Electrodeposition

○Takeyasu Saito[1], Kohei Yamada[1], Ryosuke Komoda[1], Naoki Okamoto[1] (1. Osaka Metropolitan University (Japan))

2022 International Conference on
ssdm Solid State Devices and Materials
2022 September 26-29, 2022

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-7] In-Memory and Unconventional Computing

Thu. Sep 29, 2022 9:00 AM - 10:15 AM 201 (2F)

Session Chair: Halid Mulaosmanovic (GlobalFoundries), Hiroki Sasaki (MIRISE Technologies Corp.)

9:00 AM - 9:30 AM

[F-7-01 (Invited)] Neuromorphic computing with diffusive memristors

Ye Zhuo[1], Wenhao Song[1], Ruoyu Zhao[1], ○Jianhua Yang Yang[1] (1. University of Southern California (United States of America))

9:30 AM - 9:45 AM

[F-7-02] Tiny and Error Torrent Convolutional LSTM for Event-based Vision Sensor with ReRAM Computation-in-Memory

○Tomoki Kobayashi[1], Kazuhide Higuchi[1], Naoko Misawa[1], Chihiro Matsui[1], Ken Takeuchi[1] (1. Univ. of Tokyo (Japan))

This paper proposes tiny and error tolerant Convolu-tional LSTM (ConvLSTM) for event-based vision sensor (EVS) data processing with ReRAM Computa-tion-in-Memory (CiM). To realize tiny ConvLSTM CiM, reduction of the bit precision of each ConvLSTM layer and weight is considered. On the other hand, reducing the bit precision degrades inference accuracy and error tolerance. ReRAM has low switching current and high scalability, but ReRAM has non-ideality such as conductance variation due to program/read disturb. Thus, the bit precision of the weight is optimized to accept bit error rate of 0.1%. Therefore, the proposed tiny ConvLSTM can reduce the size of memory by 91% compared with conventional ConvLSTM.

9:45 AM - 10:00 AM

[F-7-03] FeFET Reservoir with Four-Terminal Operation for Efficient and Flexible Reservoir Computing Hardware

○Kasidit Toprasertpong[1,2], Eishin Nako[1], Zeyu Wang[1], Ryosho Nakane[1], Mitsuru Takenaka[1], Shinichi Takagi[1]
(1. Univ. of Tokyo (Japan), 2. Stanford Univ. (United States of America))

We explore the potential of the four-terminal operation scheme of the FeFET reservoir in FeFET-based reservoir computing. By reading out the current waveforms from the drain, source, and substrate to form the reservoir state, the computing performance is significantly improved compared to the previous operation scheme using only the drain current. This reservoir computing scheme can well predict the output sequence of the second-order nonlinear dynamical system with a low prediction error. The four-terminal feature of FeFETs also provides the capability to fine-tune the reservoir state for flexible reservoir computing hardware.

10:00 AM - 10:15 AM

[F-7-04] A High-Efficiency, Reliable Multilevel Hardware-Accelerated Annealer with In-Memory Spin Coupling and Complementary Read Algorithm

○Yun-Yuan Wang[1], Yu-Hsuan Lin[1], Dai-Ying Lee[1], Ming-Liang Wei[1], Cheng-Hsien Lu[1], Po-Hao Tseng[1], Ming-Hsiu Lee[1], Kuang-Yeu Hsieh[1], Keh-Chung Wang[1], Chih-Yuan Lu[1] (1. Macronix Int'l Corp., Ltd. (Taiwan))

The cost-effective, high-density, and robust floating-gate (FG) spin coupler based on the NOR flash technology is proposed for the first time to overcome the challenges of convergence speed and the capacity limitation in the conventional SRAM-based simulated annealing (SA) machines. In addition, the novel complementary read algorithm can further increase the tolerance on threshold voltage (Vth) variation by 60%. Demonstrations show that the proposed in-memory spin coupling architecture provides high efficiency and scalability in solving the combinatorial problems regardless of the problem size.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[F-8] Memory Devices for New Applications

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 201 (2F)

Session Chair: Keiji Hosotani (KIOXIA Corp.), Xu Bai (NanoBridge Semiconductor, Inc.)

10:45 AM - 11:00 AM

[F-8-01] Heater Size Dependence of Mismatch in Intermediate States of Mushroom PCM Cells for Analog AI Hardware

○Jin-Ping Han[1], Arthur R Gasasira[2], Victor Chan[2], Yoo-Mi Lee[1], Timothy M Philip[2], Injo Ok[2], Iqbal Saraf[2], Kevin W Brew[2], Juntao Li[2], Ning Li[1], Nicole A Saulnier[2], Sean Teehan[2], Vijay Narayanan[1]
(1. IBM T. J. Watson Res. Center (United States of America), 2. IBM Res. - Albany Nano Tech. (United States of America))

We characterized mismatch (MM) behaviors of Ge2Sb2Te5 (GST) based mushroom phase change memory (PCM) cells and explored intermediates states MM by introducing rampup and rampdown pulses to achieve gradual reset and gradual set. We evaluated heater size dependency on device MM figure of merit (FOM) in different PCM states. We found that MM FOM in intermediate states is worse than full set and reset states, smaller heater shows better MM than bigger heater in intermediate states.

11:00 AM - 11:15 AM

[F-8-02] Multilevel In-Memory-Searching in 3D NAND-Flash Memory

○Po Hao Tseng[1], Feng Ming Lee[1], Yung Chun Li[1], Yu Hsuan Lin[1], Chih Wei Hu[1], Chih Chang Hsieh[1], Ming Hsiu Lee[1], Kuang Yeu Hsieh[1], Keh Chung Wang[1], Chih Yuan Lu[1] (1. Macronix International Co., Ltd. (Taiwan))

We propose a novel method of multilevel in-memory-searching (IMS) using 3D NAND-flash memory. The approach provides ultra-high parallel searching capability with the database stored in high-density 3D NAND-flash IMS chip(s), with the power similar to a typical NAND flash read operation. Fail bit issue caused from retention loss, program/read disturbance are evaluated and solutions are provided. An example on applying the MLC NAND-IMS accelerator in deoxyribonucleic acid (DNA) read mapping is described. The multilevel IMS is promising for data-intensive applications including big data searching and future memory-centric computing systems.

11:15 AM - 11:30 AM

[F-8-03] Split-Gate Ferroelectric Field-Effect Transistor for Reconfigurable Logic-in-Memory

○Junghyeon Hwang[1], Giuk Kim[1], Sanghun Jeon[1] (1. Korea Advanced Institute of Science and Technology (Korea))

Conventional semiconductor technology needs several devices to compose the majority logic. We present the majority logic operation with a single split-gate FeFET for non-volatile logic-in-memory (NV-LiM) technology. By using a novel write method, we found low voltage and high-speed operation were possible in split-gate FeFET, as well as improved endurance characteristics. In this presentation, we will demonstrate majority logic based reconfigurable computing using split-gate FeFET by controlling multiple inputs or stored ferroelectric polar-ization

11:30 AM - 11:45 AM

[F-8-04] Current-Divider-Via Assisted Metal-Fuse OTP Memory in FinFET CMOS Technologies

I-HSIN YANG[1], ○LI-YU YEH[1], CHRONG-JUNG LIN[1], YA-CHIN KING[1] (1. Univ. of National Tsing Hua (Taiwan))

11:45 AM - 12:00 PM

[F-8-05] The Demonstration of a Physical Unclonable Function (PUF) on a Resistive-Gate FinFET Memory

M. Y. Lee[1], Y. J. Li[2], T. C. Kao[3], C. F. Huang[4], Y. S. Wu[5], Y. H. Ye[6], M. L. Miu[7], ○E Ray Hsieh Hsieh[8], J. C. Guo[9], S. S. Chung[10]
(1. National Yang Ming Chiao Tung Univ. (Taiwan), 2. National Yang Ming Chiao Tung Univ. (Taiwan), 3. National Yang Ming Chiao Tung Univ. (Taiwan), 4. National Central Univ. (Taiwan), 5. National Central Univ. (Taiwan), 6. National Central Univ. (Taiwan), 7. National Central Univ. (Taiwan), 8. National Central Univ. (Taiwan), 9. National Yang Ming Chiao Tung Univ. (Taiwan), 10. National Yang Ming Chiao Tung Univ. (Taiwan))

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

Focus Session 2 (Area1&2&8)

[F-9] CMOS and Memory Applications of Low Dimensional Materials I

Thu. Sep 29, 2022 1:30 PM - 3:15 PM 201 (2F)

Session Chair: Toshifumi Irisawa (AIST), Hiroshi Naganuma (Tohoku Univ.)

1:30 PM - 2:00 PM

[F-9-01 (Invited)] Novel high-k insulator deposition on 2D materials for future electronics

○Kosuke Nagashio[1] (1. Univ. of Tokyo (Japan))

2:00 PM - 2:15 PM

[F-9-02] Realization of P-type MoTe2-TFET Via Laser-induced Doping Technique

○Tianshun Xie[1], Kazuki Fukuda[1], Mengnan Ke[1], Nobuyuki Aoki[1] (1. Chiba University (Japan))

The fabrication of p-type tunnel field effect transistor (TFET) composed of a transition metal dichalcogenide has great challenges due to the difficulty of n-type heavy doping. In this study, a p-type TFET has been successfully fabricated by using laser-induced doping technique to modulate the MoTe2 crystalline to n-type and p-type heavily doped regions to form a p+/i/n+ or i /n+ in-plane heterojunction.

2:15 PM - 2:30 PM

[F-9-03] Machine Learning Attack Resilient MoS_2 Fe-FET True Random Number Generator for Hardware Security in IoT: 0.7 pJ/bit Writing Energy, Self-Correction Function, and 1250 bit/s Seed Throughput

○Yu-Chieh Chien[1], Heng Xiang[1], Jianze Wang[1], Yufei Shi[1], Xuanyao Fong[1], Kah-Wee Ang[1,2]
(1. National Univ. of Singapore (Singapore), 2. Inst. of Materials Res. and Eng., A*STAR (Singapore))

We demonstrate a machine learning attack resilient true random number generator (TRNG) based on MoS2 Fe-FET. The probabilistic nature of the ferroelectric-accelerated charge trapping/de-trapping mechanism is exploited as the entropy source to achieve (i) a significantly reduced operation voltage to trigger the stochastic process by introducing a ferroelectric HZO layer with a writing energy (Ewrite) of ~0.7 pJ/bit; (ii) a physically unclonable Fe-TRNG with a near-ideal entropy of 0.99; (iii) a designed self-correction circuitry that further improves its randomness with no observable degradation after 3×106 endurance cycles. Additionally, we demonstrate the random quick response (QR) passwords as a protection layer for enhancing the hardware security in IoT. A seed throughput of 1250 bit/s and an estimated circuit power consumption of ~0.37 mW are featured in the Fe-TRNG array.

2:30 PM - 2:45 PM

[F-9-04] Moire Schottky Barriers for Lower Contact Resistances on layered MoS_2

○John Robertson[1], Zhaofu Zhang[1], Yuzheng Guo[2] (1. Cambridge University (UK), 2. Wuhan University (China))

We show how rotational Moire interfaces for electri-cal contacts between metals and monolayer MoS2 can be used to explain the metal dependence of physisorptive sites with weaker Fermi level pinning. This creates the smallest n-type Schottky barrier heights, giving the lowest contact resistances for physisorptive sites of In and noble metal Ag, as seen experimentally, but previously unexplained. They arise from a combination of low metal work function and physisorptive bonding at these sites.

2:45 PM - 3:15 PM

[F-9-05 (Invited)] Comparing h-BN and MgO as Tunnel Barriers in scaled Magnetic Tunnel Junctions

○John Robertson[1] (1. Cambridge Univ. (UK))

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

Focus Session 2 (Area1&2&8)

[F-10] CMOS and Memory Applications of Low Dimensional Materials II

Thu. Sep 29, 2022 4:00 PM - 5:45 PM 201 (2F)

Session Chair: Takamasa Kawanago (Tokyo Tech), Sakura Takeda (NAIST)

4:00 PM - 4:30 PM

[F-10-01 (Invited)] Hybrid 2D/CMOS microchips for memristive technologies

○Mario Lanza[1] (1. KAUST (Saudi Arabia))

4:30 PM - 4:45 PM

[F-10-02] Neural Network Hardware Accelerator using Memristive Crossbar Array based on Wafer-Scale 2D HfSe2

○Sifan Li[1], Samarth Jain[1], Mei-Er Pam[1], Li Chen[1], Yu-Chieh Chien[1], Xuanyao Fong[1], Dongzhi Chi[2], Kah-Wee Ang[1,2]
(1. National Univ. of Singapore (Singapore), 2. Inst. of Material Res. and Engineering (Singapore))

For the first time, hardware acceleration of neural network calculations is demonstrated using large memristive crossbar arrays (CBAs) based on two-dimensional (2D) hafnium diselenide (HfSe2). Growth of wafer-scale polycrystalline HfSe2 thin film and metal-assisted van der Waals (vdW) transfer method are developed. The memristor exhibits a small switching voltage (0.6 V) with low switching energy (0.82 pJ) and achieves synaptic long-term potentiation/depression (LTP/D) with high offline classification accuracy (93.34%) in modeled artificial neural network (ANN). Furthermore, the CBA integrates custom-designed periphery circuits to implement full-hardware convolutional image processing, achieving large-scale image edge detection, soft and inverse functions with a tight current distribution of σ = 0.25 %. This work opens a potential route to the development of large-scale and energy-efficient neuromorphic computing systems.

4:45 PM - 5:00 PM

[F-10-03] Self-selective Monolayer MoS_2 Memtransistor Crossbar Array for In-memory Computing Applications

○Xuewei Feng[1], Kah-Wee Ang[2] (1. Shanghai Jiao Tong Univ. (China), 2. National Univ. of Singapore (Singapore))

We demonstrate a CVD grown monolayer MoS2 memtransistor crossbar array capable of performing neuromorphic functionalities. The three terminal MoS2 memtransistor allows for highly controlled conductance tuning of more than 3 orders of magnitude. Moreover, sneak path current can be eliminated with the use of individual gate terminal to turn off the unselected cells. This shows the feasibility to eliminate the crosstalk issues of a typical 1R array. Building on this architecture, a 3 by 3 memtransistor crossbar array is experimentally demonstrated, paving the way for large scale implementation in neuromorphic computing.

5:00 PM - 5:15 PM

[F-10-04] Demonstration of Single-gate MoS2 Tunnel FET with Natural In-plane Heterojunction

○Tomohiro Fukui[1], Tomonori Nishimura[1], Takashi Taniguchi[2], Kenji Watanabe[2], Kosuke Nagashio[1]
(1. Univ. of Tokyo (Japan), 2. Inst. for Materials Science (Japan))

In this work, Nb-doped p+-MoS2 Tunnel FET was fabricated and demonstrated by single gate operation. It was clarified that type-III band alignment was formed at natural in-plane heterojunction. Furthermore, the additional test device revealed the two kinds current paths in the natural in-plane heterojunction device.

5:15 PM - 5:45 PM

[F-10-05 (Invited)] 2D transistor top and bottom gate stack scaling in 300mm pilot line

○Quentin Smets[1], Tom Schram[1], Daire Cott[1], Anish Dangol[1], Dennis Lin[1], Souvik Ghosh[1], Rudy Verheyen[1], Steven Brems[1], Benjamin Groven[1], Pierre Morin[1], Inge Asselberghs[1], Gouri Sankar Kar[1] (1. imec (Belgium))

2022 International Conference on
ssdm Solid State Devices and Materials
2022 September 26-29, 2022

Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[G-7] Advanced CMOS: Device Technology

Thu. Sep 29, 2022 9:00 AM - 10:15 AM 301 (3F)

Session Chair: Keisuke Yamamoto (Kyushu Univ.), Anabela Veloso (imec)

9:00 AM - 9:30 AM

[G-7-01 (Invited)] CMOS Technology Beyond FINFET : Challenges and Opportunities

○Kai Zhao[1], Julien Frougier[1], Nicolas Loubet[1], Hemanth Jagannathan[1], Brent Anderson[1], Gen Tsutsui[1], Liqiao Qin[1], Jingyun Zhang[1], Shogo Mochizuki[1], Teresa Wu[1], Dechao Guo[1], Huiming Bu[1] (1. IBM (United States of America))

9:30 AM - 9:45 AM

[G-7-02] Mobility Enhancement in Extremely-Thin Body (110) SiGe-on-insulator pMOSFETs using Starting Substrates with Thin SiGe Layers

○Chia-Tsong Chen[1], Xueyang Han[1], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1] (1. Univ. of Tokyo (Japan))

9:45 AM - 10:00 AM

[G-7-03] Atomic-Layer Deposited Tantalum-based Metal Gates (TaN, TaAlC, TaAlN, TaCoN) for Multiple VTH Modulation

○Moounsuk Choi[1], Boncheol Ku[1], Yu-Rim Jeon[1], Chulwon Chung[1], Changhwan Choi[1] (1. Hanyang university (Korea))

We demonstrated threshold voltage (VTH) modulation by various ALD TaN-based metals gates of TaN, TaAlC, TaAlN, and TaCoN. To achieve tunability of VTH, we in-cluded thickness modulation, binary or ternary metal doping, and dipole formation. By changing process pa-rameters of metal precursors, ALD process sequence, post heat treatment, dipole capping, we successfully controlled the wide range of VFB (Al¬2O3: 190 mV, La2O3: 460 mV), VTH (0.6~1.38 V) and eWF (4.09 ~ 5.43 eV), which are suitable for advanced logic device applications.

10:00 AM - 10:15 AM

[G-7-04] Mobile-Ionic FETs Based on Amorphous Dielectric with Steep Subthreshold Swing

○Huan Liu[1], Lulu Chou[2], Chengji Jin[1], Jiajia Chen[1], Xiao Yu[1], Yan Liu[2], Genquan Han[2]
(1. Zhejiang Lab (China), 2. Xidian University (China))

Thanks to the surface potential amplification effect induced by ions movement in the dielectric, the steep subthreshold swing (SS) of 25 and 19 mV/decade over 2 decades has been realized at forward and reverse sweep-ing, respectively, in mobile-ionic FETs (MIFET) with 3.5 nm amorphous (a-) ZrO2. The negative differential re-sistance (NDR) phenomenon can be observed in devices. MIFET exhibits a stable ferroelectric-type hysteresis at the wide temperature range from room temperature to 77K, with temperature-independent SS, indicating the possible low power utilization in cryogenic.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[G-8] Ferroelectric Material and Process

Thu. Sep 29, 2022 10:45 AM - 11:45 AM 301 (3F)

Session Chair: Tsuda Shibun (Renesas Electronics Corp.), Genji Nakamura (Tokyo Electron Ltd.)

10:45 AM - 11:00 AM

[G-8-01] Investigation of NH_3 Plasma Nitridation on Reliability of Gate-All-Around Stacked Poly-Si Nanosheet Channel Ferroelectric $Hf_xZr_{1-x}O_2$ FETs

Dong Ru Hsieh[1], Chia Chin Lee[1], ○Wei Ju Yeh[1], Cheng En Hsieh[1], Huai En Luo[1], Tien Sheng Chao[1]
(1. National Yang Ming Chiao Tung Univ. (Taiwan))

In this study, double-layer gate-all-around stacked poly-Si nanosheet channel ferroelectric HfxZr1–xO2 FETs with NH3 plasma at both the ZrO2/TiN and TiN/HZO in-terfaces were successfully fabricated and their reliability was investigated and discussed for the first time. By NH3 plasma at both the metal/oxide interfaces to suppress the generation of oxygen vacancies (Vo), the devices exhibit an excellent SS of 51.4 mV/dec., a high driving current of 49.5 μA/μm, and a better positive gate bias stress (PGBS) immunity for monolithic 3-D integrated circuits.

11:00 AM - 11:15 AM

[G-8-02] Effects of $Hf_xZr_{1-x}O_2$ Ferroelectrics/Ge MFIS Interfaces on Polarization Reversal Behavior

○Koichiro Iwashige[1], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1] (1. Univ. of Tokyo (Japan))

We report on the effect of interface properties on the polarization reversal behavior in HZO/Ge MFIS capacitors on Ge substrates with low doping concentrations. It is found that, when the interface properties are poor and the Fermi-level pinning occurs, the polarization reversal behavior can be observed even for MFIS capacitors with low doping concentrations at the measurement frequency where the interface states can respond.

11:15 AM - 11:30 AM

[G-8-03] A Comprehensive Study on the Ferroelectric HfO_2-ZrO_2-HfO_2 and ZrO_2-HfO_2-ZrO_2 Nanolaminates

○Kaixuan Li[1], Yue Peng[1], Wenwu Xiao[2], Yan Liu[1], Genquan Han[1,3], Yue Hao[1]
(1. Wide Bandgap Semiconductor Technology Disciplines State Key Laboratory, School of Microelectronics, Xidian University (China), 2. Xi'an UniIC Semiconductors Company Ltd. (China), 3. Hangzhou Institute of Technology, Xidian University (China))

In this paper, the effect of starting layer on the ferroelectric properties and reliability of Zr-doped HfO2 ferroelectric (FE) thin films was studied. The HfO2-ZrO2-HfO2 (HZH) and ZrO2-HfO2-ZrO2 (ZHZ) nanolaminates metal-FE-metal (MFM) capacitors were fabricated. Compared with the ZHZ device, a higher value of 2Pr for the HZH device was achieved. However, the ZHZ structure shows a better wake-up performance and frequency stability than HZH, which is due to the HfO2 initial layer introduces more oxygen into FE film than ZrO2 during FE film deposition. The study is helpful for understanding and optimizing the HfO2-based FE films for non-volatile memory applications.

11:30 AM - 11:45 AM

[G-8-04] Improved Ferroelectric Memory Characteristics by Using TiN_x in Novel $Ru/TiN_x/Hf_{0.5}Zr_{0.5}O_2/TiN$ Capacitor

○Asim Senapati[1], Siddheswar Maikap[1,2], Chen- Ying Lin[3], Chun- Yu Liao[3], Min- Hung Lee[3]
(1. Chang Gung University (CGU) (Taiwan), 2. Keelung Chang Gung Memorial Hospital (CGMH) (Taiwan), 3. National Taiwan Normal University (NTNU) (Taiwan))

A thin TiNx layer in novel Ru/TiNx/Hf0.5Zr0.5O2/TiN capacitor shows improved 2Pr value of 14.5%, 22.4 μC/cm2 after 1010 cycles, and 27.1 μC/cm2 after 10 years retention with respect to without TiNx in Ru/Hf0.5Zr0.5O2/TiN. This is owing to higher ratio of o-phase from HRTEM, higher permittivity, and TiNx consumes limited oxygen to have lower barrier height by F-N tunneling.

2022 International Conference on
ssdm Solid State Devices and Materials
2022 September 26-29, 2022

Session information

Oral Presentation

01: Advanced CMOS: Material Fundamentals / Process Science / Device Physics

[G-10] Advanced CMOS: Device, Process and Material

Thu. Sep 29, 2022 4:00 PM - 6:00 PM 301 (3F)

Session Chair: Nobuyuki Mise (Hitachi High-Tech Corp.), Keisuke Yamamoto (Kyushu Univ.)

4:00 PM - 4:30 PM

[G-10-01 (Invited)] Design-Technology Co-Optimization for Future CMOS: from finFET to CFETs and Backside Power

Geert Hellings[1], Pieter Schuddinck[1], Samantha Liu[1], Shairfe Muhammad Salahuddin[1], Gioele Mirabelli[1], Rongmei Chen[1], Anabela Veloso[1], Anne Jourdain[1], ○Gaspard Hiblot[1], Naoto Horiguchi[1], Julien Ryckaert[1] (1. imec (Belgium))

4:30 PM - 4:45 PM

[G-10-02] Impact of Back-side Power Delivery Network Layout on the FinFET Device Performance

○Goutham Arutchelvan[1], Thomas Chiarella[1], Hiroaki Arimura[1], Anabela Veloso[1], Anne Jourdain[1], Eugenio Dentoni Litta[1], Naoto Horiguchi[1], Jerome Mitard[1] (1. imec (Belgium))

Backside power delivery (BSPDN) with Buried Power Rail (BPR) is an essential enabler for CMOS scaling beyond the 5nm node. In this work, we show that integrating BPR and Nano-Through Silicon Via (n-TSV) close to the active channel does not degrade the device performance, thus, confirming that the stress transfer from BSPDN elements is rather weak. Design guidelines with respect to n-TSV proximity and number of VBPR vias for optimized device performance and reduced footprint is discussed.

4:45 PM - 5:00 PM

[G-10-03] Investigation of access resistance components in Si-channel p-FinFET using cascaded devices.

○Pierre Eyben[1], Goutham Arutchelvan[1], Thomas Chiarella[1], Hiroaki Arimura[1], Romain Ritzenthaler[1], Jérome Mitard[1], Eugenio Dentoni Litta [1], Naoto Horiguchi[1], Ludovic Goux[1] (1. Imec (Belgium))

Within this work, a new procedure is proposed to split and analyze the different access resistance compo-nents for Si-channel p-FinFET devices. This is realized combining a dedicated cascaded FET test-structure and advanced data filtering procedures. This is allowing us to identify the relative weight of contact, epi, interface and channel resistance components and hence to propose strategies to minimize the total access resistance such as the introduction of graded SiGe source-drain epi.

5:00 PM - 5:15 PM

[G-10-04] Impacts of Annealing Temperature and Atmosphere on (111) and (100) n-Ge MOS Interface Properties with Plasma Oxidation GeO_x and ALD Al_2O_3

○Xueyang Han[1], Chia-Tsong Chen[1], Mengnan Ke[2], Ziqiang Zhao[1], Kasidit Toprasertpong[1], Mitsuru Takenaka[1], Shinichi Takagi[1] (1. Univ. of Tokyo (Japan), 2. Chiba Univ. (Japan))

5:15 PM - 5:30 PM

[G-10-05] Low Temperature Selective Growth of Ga-Doped Germanium Source / Drain for pMOS Devices

○Clement Porret[1], Gianluca Rengo[1,2,3], Mustafa Ayyad[1], Andriy Hikavyy[1], Erik Rosseel[1], Robert Langer[1], Roger Loo[1] (1. imec vzw (Belgium), 2. Quantum Solid State Physics, KU Leuven (Belgium), 3. FWO - Vlaanderen (Belgium))

The properties of Ge:Ga epilayers, grown selectively at low temperature using a cyclic deposition and etch chemical vapor deposition process, are investigated and benchmarked against their Ge:B counterpart. Ti / Ge:Ga contacts are evaluated with the aim of providing new solutions for advanced Ge-based devices.

5:30 PM - 5:45 PM

[G-10-06] Atomic Layer Etching of Ti-Compounds: Mechanism and Etch Selectivity Control for Advanced Device Fabrication

○Bablu Mukherjee[1,2], René H.J. Vervuurt[3], Airah Peraro Osonio[2], Takayoshi Tsutsumi[2], Masaru Hori[2], Nobuyoshi Kobayashi[2] (1. ASM Japan K.K. (Japan), 2. Nagoya Univ. (Japan), 3. ASM Belgium (Belgium))

5:45 PM - 6:00 PM

[G-10-07] Super-conformal CVD Ruthenium with 1 Angstrom Liner in Advanced MOL Local Interconnect

○Maryamsadat Hosseini[1], Alicja Leśniewska[1], Gyana Pattanaik[2], Robert Clark[2], Anish Dangol[1], Marleen H van der Veen[1], Nicolas Jourdan[1], Gert Leusink[2], Hunter Frost[2], Cory Wajda[2], Eugenio Dentoni Litta[1], Naoto Horiguchi[1]

(1. imec (Belgium), 2. TEL (United States of America))

Ruthenium is a prime candidate to replace Tungsten and Cobalt in MOL local interconnects. In this paper we demonstrate for the first time a seamless and barrierless narrow trench filling using super-conformal CVD Ru with ultra-thin liners (1 Å thick TiN or 2 Å thick TaN). We also report reliability studies that indicate Ruthenium does not drift into the oxide dielectric.

2022 International Conference on
ssdm Solid State Devices and Materials
2022 September 26-29, 2022

Session information

Oral Presentation

08: Low Dimensional Devices and Materials

[H-8] Device Application III: Low Dimensional Devices and Materials

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 302 (3F)

Session Chair: Yusuke Hoshi (Tokyo City Univ.), Taishi Takenobu (Nagoya Univ.)

10:45 AM - 11:15 AM

[H-8-01 (Invited)] Upconversion Optoelectronic Phenomena in van Der Waals Heterostructures

○Goki Eda[1] (1. National Univ. of Singapore (Singapore))

11:15 AM - 11:30 AM

[H-8-02] Ohmic current injection into single-crystal carbon-doped *h*-BN toward two-dimensional power device application

○Supawan Ngamprapawat[1], Tomonori Nishimura[1], Kenji Watanabe[2], Takashi Taniguchi[2], Kosuke Nagashio[1]
(1. Univ. of Tokyo (Japan), 2. NIMS (Japan))

Current injection into two types of C-doped single-crystal h-BN prepared by in-situ C doping and C diffusion was investigated. The in-situ C-doped h-BN with a higher C density shows an ohmic conduction, while the C-diffused h-BN exhibits a nonohmic conduction. Both current injections show totally different behavior from the transverse dielectric breakdown. The detailed analysis suggests that the dominant mechanism for current injection in the in-situ C-doped and C-diffused h-BN is tunneling through defect states and tunneling-assisted Poole-Frenkel (PF) conduction, respectively.

11:30 AM - 11:45 AM

[H-8-03] PCz sorted SWCNTs-TFT "Electronic Hourglass" and its Recovery Behavior

○Yang Xu[1], Qinyu Hu[1,2], Yi Zhou[1,2], Jiayi Wang[1], Qi Huang[3], Jie Zhao[3], Xuelei Liang[3], Shengkai Wang[1,2]
(1. Inst. of Microelectronics of Chinese Academy of Sci. (China), 2. Univ. of Chinese Academy of Sci. (China), 3. Key Lab. for the Physics and Chemistry of New Device, Peking Univ. (China))

11:45 AM - 12:00 PM

[H-8-04] Accuracy of Equivalent Model in Band-to-band Tunneling Simulation of Semiconductor Nanowires

○Jo Okada[1], Nobuya Mori[1], Gennady Mil'nikov[1] (1. Osaka Univ. (Japan))

Accuracy of the equivalent model in the band-to-band tunneling simulation of semiconductor nanowires is investigated by constructing equivalent models for various semiconductor nanowires and calculating the tunneling probability with non-equilibrium Green's function method. As the transport window is widened, the equivalent model accurately reproduces not only the traveling states but also the evanescent states. The relative error of the tunneling probability is found to decrease exponentially as the transport window width. In addition, the direct-gap semiconductor nanowire case is found to be more accurate than the indirect-gap case.

2022 International Conference on
ssdm 2022 Solid State Devices and Materials
September 26-29, 2022

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-8] Si and SiC Power Devices

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 303 (3F)

Session Chair: Tetsuya Nitta (Mitsubishi Electric Corp.), Tomoaki Hatayama (Sumitomo Electric Industries, Ltd.)

10:45 AM - 11:15 AM

[J-8-01 (Invited)] Progress of Low-Voltage Si-Power MOSFETs

○Wataru Saito[1] (1. Kyushu Univ. (Japan))

11:15 AM - 11:30 AM

[J-8-02] Poly Back Seal Effect on Platinum Solid Phase Diffusion in High Speed Switching Diodes

○Yuhki Fujino[1], Shotaro Baba[1], Hiroaki Kato[1], Shingo Sato[1], Katsura Miyashita[1]
(1. Toshiba Electric Devices & Storage Corp. (Japan))

We evaluated poly back seal (PBS) effect on platinum concentration profile during platinum solid phase diffusion in high speed switching diodes. We confirmed that the platinum concentration in PBS is kept constant and by far higher than that in silicon wafers. We also confirmed that the thicker the PBS, the more platinum is accumulated. It is also confirmed that PBS has no effects on the platinum concentration profile of the front side of the wafer after platinum solid phase diffusion, which is also verified in Qrr measurement.

11:30 AM - 11:45 AM

[J-8-03] Experimental Demonstration of the Surge Current Capability of Embedded SBDs in 1.2-kV SiC SBD-integrated Trench MOSFETs with Ti and Ni as Schottky Metals

○Yudai Kitamura[1], Takeshi Tawara[2], Shinsuke Harada[2], Hiroshi Yano[1], Noriyuki Iwamuro[1]
(1. Univ. of Tsukuba (Japan), 2. National Inst. of Advanced Indus. Sci. and Tech. (Japan))

This study investigates, for the first time, the surge current capabilities of embedded Schottky Barrier Diodes (SBDs) in a 1.2-kV SiC SBD-integrated trench MOSFET (SWITCH-MOS) with Ti and Ni, as Schottky metals, and demonstrates sufficiently high SBD surge current capabilities when a higher Schottky barrier height of Ni was used.

11:45 AM - 12:00 PM

[J-8-04] Experimental and Numerical Investigations of the Electrical Characteristics of SiC SBD-Integrated MOSFETs by Varying the Area Occupied by Embedded SBDs

○Keisuke Kashiwa[1], Mitsuki Takahashi[1], Hiroshi Yano[1], Noriyuki Iwamuro[1] (1. Univ. of Tsukuba (Japan))

This study describes the static and dynamic char-acteristics and withstanding capabilities of two types of 1.2-kV SiC SBD-integrated MOSFET, which have different SBD areas, using experimental validation and numerical simulations. In the MOSFETs with a larger SBD area, unipolar operation in the SBD during diode forward operation was maintained at higher forward currents; as a result, the MOSFETs show lower re-verse recovery and turn-on losses. However, the MOSFETs with a larger SBD area showed higher leakage current through the SBD during short-circuit transients owing to a higher electric field at the SBD, resulting in less short-circuit withstanding capability.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

04: Power / High-speed Devices and Materials

[J-9] GaN Power Devices

Thu. Sep 29, 2022 1:30 PM - 3:00 PM 303 (3F)

Session Chair: Toru Sugiyama (Toshiba Device & Strage Corp.), Heiji Watanabe (Osaka Univ.)

1:30 PM - 2:00 PM

[J-9-01 (Invited)] Non-destructive Breakdown in GaN/SiC-based Hybrid HEMT

○Akira Nakajima[1], Hirohisa Hirai[1], Yoshinao Miura[1], Shinsuke Harada[1] (1. AIST (Japan))

2:00 PM - 2:15 PM

[J-9-02] Two-dimensional characterization of the edge structure of Ni/n-GaN Schottky contacts under applied voltage by scanning internal photoemission microscopy

○Hiroki Imabayashi[1], Fumimasa Horikiri[2], Yoshinobu Narita[2], Noboru Fukuhara[2], Tomoyoshi Mishima[3], Kenji Shiojima[1]
(1. Univ. of Fukui (Japan), 2. SCIOCS (Japan), 3. Hosei Univ. (Japan))

We report the experimental results on mapping characterization of the edge structure of Ni/n-GaN Schottky contacts formed with a metal-shadow-mask by scanning internal photoemission microscopy (SIPM). The high breakdown-voltage and uniform SIPM signals under ap-plied voltage were obtained for the fresh sample. On the other hand, SIPM signals increased significantly at the electrode edge for the aged sample compared with the electrode center. It is considered that the influence of the electric field concentration on the electrode periphery was detected as a photocurrent. We found that SIPM is available to clarify the relationship between the difference in the structure and electric field concentration at the edge of electrode.

2:15 PM - 2:30 PM

[J-9-03] Theoretical Analysis of Tunneling Current in 4H-SiC Schottky Barrier Diodes Under Reverse-biased Condition Based on Complex Band Structure

○Yutoku Murakami[1], Sachika Nagamizo[1], Hajime Tanaka[1], Nobuya Mori[1] (1. Osaka Univ. (Japan))

The tunneling current in heavily doped 4H-SiC Schottky barrier diodes under reverse-biased condition is calculated based on the complex band structure. Considering the nonparabolicity of the complex band, the experimental result of tunneling current is well reproduced by the calculation.

2:30 PM - 2:45 PM

[J-9-04] Stability of Monolithically Integrated Power devices for 200V GaN-on-SOI power circuits platform

○Deepthi Cingu[1], Olga Syshchyk[1], Dirk Wellekens[1], Thibault Cosnier[1], Matteo Borga[1], Urmimala Chatterjee [1], Benoit Bakeroot[2], Niels Posthuma[1], Stefaan Decoutere[1] (1. Imec (Belgium), 2. Center for Microsystems Technology (Belgium))

The stability of the monolithically integrated Enhance-ment-mode p-GaN HEMTs, Depletion Mode MIS HEMTs and Schottky Barrier diodes in a 200 V GaN-on-SOI technology is studied for two different dielectric options. This paper focuses mainly on wafer-level High Temper-ature Reverse Bias (HTRB), High Temperature Gate Bias (HTGB) and High Temperature Forward Bias (HTFB) experiments. The results display that the addition of the integral components has shown no impact on the stability of the baseline p-GaN HEMTs.

2:45 PM - 3:00 PM

[J-9-05] Vertical Current Temperature Analysis of GaN-on-Si Epitaxy through Analytical Modelling

○Florian Rigaud-Minet[1,2], Julien Buckley[1], William Vandendaele[1], Stéphane Bécu[1], Matthew Charles[1], Jérôme Biscarrat[1], Romain Gwoziecki[1], Charlotte Gillot[1], Veronique Sousa[1], Hervé Morel[2], Dominique Planson[2]
(1. CEA, LETI and Univ. Grenoble Alpes (France), 2. Univ. Lyon, INSA Lyon, Ampère Lab. (France))

The current temperature dependence of a 3.9 µm GaN-on-Silicon epitaxy at temperatures ranging from 25 °C to 200 °C and for voltages beneath the plateau limited by the carrier generation in the p-doped substrate is analyzed. Based upon a fit with analytical transport models, the vertical current is reported for the first time to be the superposition of three different transport mechanisms: Recombination limited at low and middle voltages for low temperatures, Ohmic at low and middle voltages for high temperatures and Nearest Neighbor Hopping (NNH) at high voltages. Thanks to their temperature dependences and therefore to their energy, the transports can be related to either point defects clustered around threading dislocations or to interstitial nitrogen.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

02: Advanced and Emerging Memories / New Applications

[J-10] DRAM, SRAM, and 3D NAND

Thu. Sep 29, 2022 4:00 PM - 5:45 PM 303 (3F)

Session Chair: Norikatsu Takaura (Hitachi, Ltd.), Soichi Sugiura (Micron Technology Inc.)

4:00 PM - 4:15 PM

[J-10-01] Evaluating Pillar Capacitor Profile and Material Property Effects on Advanced DRAM Device Performance

○Ye Xiao Yu[1], Zhong Ming Liu[1], Guo Bao Xiong[1] (1. Changxin corporate (China))

4:15 PM - 4:30 PM

[J-10-02] What are the Constraints for 1T-DRAM Operation via Reconfigurable Transistor?

○Rohit Kumar Nirala[1], Sandeep Semwal[2], Nivedita Rai[3], Abhinav Kranti[4]
(1. Indian Institute of Technology Indore (India), 2. Indian Institute of Technology Indore (India), 3. Indian Institute of Technology Indore (India), 4. Indian Institute of Technology Indore (India))

4:30 PM - 4:45 PM

[J-10-03] Evaluate the Impact of Process Variations on Storage Node Contact Area Under Different Etching Models

○Ye Xiao Yu[1], Zhong Ming Liu[1], Jing Si Cui[1] (1. Changxin corporate (China))

4:45 PM - 5:00 PM

[J-10-04] A Loadless 4T SRAM Cell Powered by Gate Leakage Current and Tolerant of Random Dopant Fluctuation and Surface Roughness at Si-SiO_2 Interface

○Yihan Zhu[1], Takashi Ohsawa[1] (1. Waseda Univ. (Japan))

Monte Carlo simulations under Vth fluctuation and gate leakage current variation due to random dopant fluctuation (RDF) and surface roughness at Si-SiO2 interface are conducted for a new loadless 4T SRAM cell in 32nm whose data is held by gate leakage current of the access PFETs with EOTp less than EOPn. Read and write SNMs are shown larger than 6TSRAM. Though the hold SNM is smaller than 6TSRAM, its -5 sigma value is extrapolated to 60mV at VDD=1V and T=25 deg. C

5:00 PM - 5:15 PM

[J-10-05] Improvement of Cell Characteristics using Controlling the Current Path in 3D NAND Flash

Daewoong Kang[1], ○Hyojin Park[2], Inyoung Lee[2], Hyowon Kang[3], Hyoungsoo Kim[4]
(1. Korea National University of Transportation (Korea), 2. Myongji Univ. (Korea), 3. Korea Int'l School (Korea), 4. California State Polytechnics Univ. (United States of America))

In Vertical NAND (V-NAND) flash memory, the effect of current path change according to the program state was analyzed. Also, the method to control it was confirmed through simulation. Electrical properties such as S.S and short channel effect were improved by adding a separately doped poly silicon channel under the poly silicon channel.

5:15 PM - 5:30 PM

[J-10-06] Analytical Modeling of Intrinsic Threshold Voltage and Subthreshold Slope for 3D NAND Flash Memory with a Gaussian Doping Profile

○Amit Kumar[1], Shubham Sahay[1] (1. Indian Inst. of Tech., Kanpur (India))

In this work, we formulate an analytical model for the intrinsic threshold voltage and the subthreshold slope of 3D NAND flash cells with uniform threshold voltage distribution across different word line (WL) layers along the string. The results obtained using the analytical model are in close agreement with the TCAD simulations validating the accuracy of the developed model. We also utilize the analytical model to provide insights and necessary design guidelines for further optimizing the performance.

5:30 PM - 5:45 PM

[J-10-07] Dually Functional Wide Bandgap Oxides Bilayer SiO_2/Al_2O_3 Based Memristor for Nonvolatile Memory and Photo Sensing

○Dayanand Kumar[1], Lana Joharji[1], Nazek El Atab[1] (1. King Abdullah University of Science and Technology (Saudi Arabia))

In this work, we investigate bilayer SiO2/Al2O3-based memristor for nonvolatile memory and photo sensing application. The current opto-electronic ITO/SiO2/Al2O3/Pt device exhibits good photo sensing features in terms of electrical SET and optical RESET endurance of at least 100 cycles for blue light without any disruption. Furthermore, the device shows highly stable retention (104 s) without any degradation and excellent device-to-device uniformity. This work not only enables us to use our device in memory capabilities but also provides a significant advantage for photo sensing.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

12: Advanced Circuits / Systems Interacting with Innovative Devices and Materials

[K-7] Advanced Systems with Innovative Devices

Thu. Sep 29, 2022 9:00 AM - 10:15 AM 304 (3F)

Session Chair: Daisuke Kanemoto (Osaka Univ.), Yasuhiro Ogasahara (AIST)

9:00 AM - 9:30 AM

[K-7-01 (Invited)] Mixed-Signal Circuit Design for the Data-Driven World

○Boris Murmann[1] (1. Stanford Univ. (United States of America))

9:30 AM - 9:45 AM

[K-7-02] Crystalline Oxide Semiconductor FET-based Analog Neural Network for Intelligent IoT Sensor

○Hidefumi Rikimaru[1], Satoru Ohshita[1], Yoshiyuki Kurokawa[1], Toshihiko Takeuchi[1], Shunpei Yamazaki[1]
(1. Semiconductor Energy Laboratory Co., Ltd. (Japan))

This paper proposes an intelligent Internet of Things (IoT) sensor including an analog neural network (NN) constructed using a crystalline oxide semiconductor field-effect transistor (OSFET). An analog multiply-accumulate (MAC) cell array composed of only OSFETs corresponds to a synapse circuit of each layer in the NN, and monolithically stacked OSFET layers are applicable to a multilayer NN. MAC cells execute MAC operation with current input of the order of picoamperes. Stacking a photoelectric conversion layer on the NN should achieve a low-power intelligent IoT sensor.

9:45 AM - 10:00 AM

[K-7-03] Feasibility Study for 32-level cell using Memory with 13.5-V 0.5-um OSFET Monolithically Stacked on 13.5-V 1.6-um CMOSFET

○Hiroki Inoue[1], Shoki Miyata[1], Yusuke Komura[1], Yuki Okamoto[1], Takanori Matsuzaki[1], Hidetomo Kobayashi[1], Yoshinori Ando[1], Hitoshi Kunitake[1], Yoshiyuki Kurokawa[1], Shunpei Yamazaki[1] (1. Semiconductor Energy Laboratory Co., Ltd. (Japan))

We found a possibility to achieve a 32-level cell using a 16-level-cell memory test chip in which a 13.5-V 0.5-um crystalline oxide semiconductor field-effect transistor (OSFET) was monolithically stacked on a 13.5-V 1.6-um CMOSFET. The variation in a read 16-level analog voltage, the +/-3 sigma range, was 0.202 V at a maximum. With regard to retention characteristics, 16-level data was retained for three hours at room temperature, and the voltage change was 0.038 V at a maximum. The narrowest difference between distributions was 0.253 V. The maximum +/-3 sigma range was smaller than the narrowest difference between distributions, which shows a possibility that one more piece data is able to be retained between pieces of data.

10:00 AM - 10:15 AM

[K-7-04] Design and fabrication of low-power sensing circuits based on carbon nanotube thin-film transistors for self-powered flexible sensors

○Naohiro Mitsuzawa[1], Taiga Kashima[1], Hiromichi Kataura[2], Yutaka Ohno[3]
(1. Nagoya Univ. (Japan), 2. Nanomaterials Research Institute, National Institute of Advanced Industrial Science and Technology (Japan), 3. Inst. of Material and Systems for Sustainability, Nagoya Univ. (Japan))

2022 International Conference on
Solid State Devices and Materials
2022 September 26-29, 2022

Session information

Oral Presentation

Joint Session (Area1&12)

[K-8] Innovative Devices and Systems for Advanced Imaging and Sensing

Thu. Sep 29, 2022 10:45 AM - 12:00 PM 304 (3F)

Session Chair: Keita Yasutomi (Shizuoka Univ.), Hidetoshi Oishi (Sony Semiconductor Solutions Corp.)

10:45 AM - 11:00 AM

[K-8-01] Electro-optic imaging system using a CMOS image sensor with a dual-layer on-pixel polarizer

○Ryoma Okada[1], Kiyotaka Sasagawa[1], Maya Mizuno[2], Hironari Takehara[1], Makito Haruta[1], Hiroyuki Tashiro[1,3], Jun Ohta[1]
(1. Nara Institute of Science and Technology (Japan), 2. National Institute of Information and Communications Technology (Japan), 3. Kyushu Univ. (Japan))

In this study, we demonstrate an electro-optic (EO) imaging system using an image sensor with dual-layer on-pixel polarizers composed of metal wire grids. The line and space of the dual-layer polarizer are both set to 0.7 μm. The extinction ratio at a wavelength of 780 nm is 3.49, which is considerably higher than that of a sin-gle-layer polarizer with identical line and space dimen-sions. The system improves signal detection performance by more than seven times in the EO imaging of a high-frequency electric field of 100 MHz.

11:00 AM - 11:15 AM

[K-8-02] A high-NIR sensitivity SOI-gate lock-in pixel with improved modulation contrast

○Tatsuya Kobayashi[1], Keita Yasutomi[1], Naoki Takada[1], Shoji Kawahito[1] (1. Shizuoka Univ. (Japan))

11:15 AM - 11:30 AM

[K-8-03] Double Modulation Lock-in Based Stimulated Raman Scattering Detection Method Using a Charge Modulator CMOS Image Sensor

○Shukri Bin Korakkottil Kunhi Mohd[1], De Xing Lioe[2], Keita Yasutomi[3], Keiichiro Kagawa[4], Mamoru Hashimoto[5], Shoji Kawahito[6]
(1. Shizuoka University (Japan), 2. Shizuoka University (Japan), 3. Shizuoka University (Japan), 4. Shizuoka University (Japan), 5. Hokkaido University (Japan), 6. Shizuoka University (Japan))

This paper reports a design of the Stimulated Raman Scattering (SRS) detection method using a high-speed lock-in CMOS image sensor. Since the SRS signal is very weak, a two-stage fully-differential switched-capacitor integrator is designed to cancel offset light and amplify the SRS signal. The sensitivity of the proposed method is shown based on the relative intensity of up to ΔISRS / Ioffset = 10-6. The two-stage readout mechanism reduces the circuit's low-frequency noise by approximately 1-decade, which improves the dynamic range. The advantage of the double-modulation technique is that the system's low-frequency noise is reduced, where the first modulation is for laser intensity noise and the second is for circuit noise.

11:30 AM - 11:45 AM

[K-8-04] Development of Thin Film Retinal Prosthesis with CMOS Smart Electrode Array

○Kaige Pan[1], Ronnakorn Siwadamrongpong[1], Takanori Hagiwara[1], Makito Haruta[1], Yukari Nakano[2], Takurou Kouno[2], Yasuo Terasawa[2], Hironari Takehara[1], Hiroyuki Tashiro[1,3], Kiyotaka Sasagawa[1], Jun Ohta[1]
(1. Nara Institute of Science and Technology (Japan), 2. Nidek Corp., Ltd. (Japan), 3. Kyushu Univ. (Japan))

Retinal prosthesis reconstructs vision by electrically stimulating the remaining normal retinal cells of patients with age-related macular degeneration and retinitis pigmentosa. The purpose of this study is to develop a device that can be safely implanted into patients for a long period. We successfully develop a flexible retinal prosthesis with the CMOS smart electrode array. By mounting CMOS chips in the device, the device can work with only four wirings. Simulating the in-vivo environment using a rat, a biphasic stimulation current waveform is confirmed with our device.

11:45 AM - 12:00 PM

[K-8-05] Self-Sensitivity Amplifiable Dual-gate Ion-Sensitive Field-Effect Transistor Based on High-*k* Engineered Dielectric Layer

○Yeong-Ung Kim[1], Won-Ju Cho[1] (1. Kwangwoon Univ. (Korea))

In this study, we propose a self-sensitivity amplifiable pH sensor platform based on a double gate (DG) ion sensing field effect transistor (ISFET) by applying a high-k engineered dielectric layer. The amplification ca-pacity was ensured through the capacitive coupling effect using the DG structure to overcome the limitations of the conventional ISFET (~59 mV/pH @300K). The imple-mented ISFET exhibited sensitivity far exceeding the Nernst limit depending on the capacitance ratio of the top gate dielectric to the bottom gate dielectric, as well as excellent linearity and stability under exposure to pH buffer solution. In addition, the amount of change ac-cording to pH was maximized by extracting the current change based on the reference voltage. Therefore, the proposed ISFET is expected to be a promising technology that can be utilized as a biosensor platform for detecting micropotential analytes.

2022 International Conference on
Solid State Devices and Materials
SSDM 2022 September 26-29, 2022

Session information

Oral Presentation

12: Advanced Circuits / Systems Interacting with Innovative Devices and Materials

[K-9] Advanced Device-based Circuits and Power Management Systems

Thu. Sep 29, 2022 1:30 PM - 3:15 PM 304 (3F)

Session Chair: Kousuke Miyaji (Shinshu Univ.), Kiichi Niitsu (Nagoya Univ.)

1:30 PM - 1:45 PM

[K-9-01] Wide temperature- and voltage-range temperature sensing utilizing statistical property of sub-threshold MOSFET current

○Shinichi Ota[1], Mahfuzul Islam[1], Takashi Hisakado[1], Osami Wada[1] (1. Graduate School of Engineering, Kyoto Univ. (Japan))

CMOS temperature sensors are attractive for their low-power operation. However, they suffer from narrow temperature range operation due to the complex relationship between the drain current and temperature. This paper proposes a CMOS based temperature sensor that utilizes the statistical properties of sub-threshold MOSFET current to suppress several error sources. The sensor operates under a supply voltage of 0.8 V to 1.2 V and achieves an error of −0.53/+0.43 °C across a range of −20 °C to 120 °C after a two-point calibration.

1:45 PM - 2:00 PM

[K-9-02] CMOS Inverter-Base Ring Oscillator Design and Evaluation Against g-ray Total Ionizing Dose Effect

○Arisa Kimura[1], Kaito Kuroki[1], Ryoichiro Yoshida[1], Kenji Hirakawa[1], Masayuki Iwase[1], Munehiro Ogasawara[1], Takashi Yoda[1], Noboru Ishihara[1], Hiroyuki Ito[1] (1. Tokyo Institute of Technology (Japan))

The gamma ray Total Ionizing Dose (TID) effect up to 10 Mrad on 0.18-um MOSFET is modeled and a radiation-hard design method for stabilizing oscillation frequency of CMOS inverter base ring oscillators have been devised. The TID effect on MOSFET is modeled using a function of the two exponential sums to express combination phenomena of two kinds of charge trapping for the threshold voltage and leakages current variations, respectively. By using this model, the TID effect to CMOS inverter circuit was analyzed, and it was clarified that the oscillation frequency of the CMOS ring IC can be stabilized against the TID effect by optimizing the size ratio of p-type and n-type MOSFETs. This was successfully confirmed by fabricating and evaluating CMOS oscillator ICs with the 0.18-um technology. These results are useful design guideline for CMOS ICs for systems in radiation-irradiated environments.

2:00 PM - 2:15 PM

[K-9-03] A Sub-10nW Temperature-to-Digital-Converter for Thermopile Temperature Sensors

Mao-Wei Lee[1], ○Hongchin Lin[1], Po-Wei Lai[1] (1. National Chung Hsing Univ. (Taiwan))

A 6.29nW temperature-to-digital converter (TDC) at VDD = 0.7 V for thermopile temperature sensors was designed and fabricated on 0.068mm^2 using the 90 nm CMOS technology. The small output voltages of a few mV produced by thermopile sensors is proportional to the frequency ratios in the TDC. The average resolution is 0.11ºC with the conversion time of 348 ms. Its inaccuracy is +0.18/-0.98ºC for the object temperatures from -10ºC to 100ºC at the ambient temperature of 25ºC.

2:15 PM - 2:30 PM

[K-9-04] A 24V-to-1V On-Chip Switch Dual-Charging Path Dual-Inductor Hybrid Converter Achieving Improved Load Transient Response

○Kazuya Nishijima[1], Toma Umeki[1], Kousuke Miyaji[1] (1. Shinshu University (Japan))

This paper proposes a dual-charging path dual-inductor hybrid (DCP-DIH) converter that can charge two inductors simultaneously to improve load transient response. The proposed scheme only introduces a single additional switch and capacitor to form dual charging paths during load transient response. All power switches are integrated using 5V transistors with 0.25μm HV BCD process. Simulation results show that the proposed circuit achieves 8.7% recovery time and 12.9% voltage drop reduction compared to the conventional DIH converter at 20mA to 4A load transient step.

2:30 PM - 2:45 PM

[K-9-05] Low-Jitter CMOS Inverter-Based RC Oscillator with Voltage-Integration Feedback for Sensor Interface

○ZIXUAN LI[1], Sangyeop Lee[1], Noboru Ishihara[1], Hiroyuki Ito [1] (1. Tokyo Inst. of Tech. (Japan))

In this work, we proposed a low-power high-resolution sensor interface circuit based on a range improved feedback RC oscillator, which could be applied for various kinds of sensing. The sensor prototype circuit is fabricated in 0.18μm standard CMOS process, achieving period jitter of 50ppm while the cycle is 55 μs, and the power consumption is 7.5 μW with 1-V power supply.

2:45 PM - 3:00 PM

[K-9-06] Fully Integrated Switched-Capacitor Buck Converter with Variable Ratio and Frequency Controllers for Ultra-Low Power LSI Systems

○Ryo Matsuzuka[1], Tetsuya Hirose[1], Shuto Kanzaki[2], Kaori Matsumoto[1], Nobutaka Kuroki[2], Masahiro Numa[2], Daisuke Kanemoto[1] (1. Osaka Univ. (Japan), 2. Kobe Univ. (Japan))

This paper presents a switched-capacitor (SC) buck converter with a variable ratio and frequency controllers. The variable ratio controller monitors an input voltage and then changes the step-down ratio of the SC converter, enabling the converter to operate with a wide range of input voltage. The frequency controller changes a frequency in accordance with the load current for highly efficient power conversion. Measurements of a prototype chip demonstrated that our SC buck converter achieved a high efficiency of 84%.

3:00 PM - 3:15 PM

[K-9-07] Switched-Capacitor Voltage Boost Converter with Digital Maximum Power Point Tracking for Low-Voltage Energy Harvesting

○Kaori Matsumoto[1,2], Ryuki Ikeda[2], Hikaru Sebe[2], Nobutaka Kuroki[1], Masahiro Numa[1], Daisuke Kanemoto[2], Tetsuya Hirose[2] (1. Kobe Univ. (Japan), 2. Osaka Univ. (Japan))

This paper presents an ultra-low-power switched-capacitor (SC) voltage boost converter (VBC) with a digital maximum power point tracking (MPPT) control circuit for low-voltage energy harvesting. The proposed digital MPPT control circuit converts analog voltage information of the PV cell into digital values and extracts the maximum power regardless of the harvester’s conditions and load current. Measurement results demonstrated that our proposed digital MPPT control circuit can track the maximum power point of the PV cell successfully. The proposed PMS generated a 2.58-V output voltage from a 0.46-V input voltage. The maxi-mum power conversion efficiency was 63%.